

## 512 X 8 Electrically Erasable PROM

### FEATURES

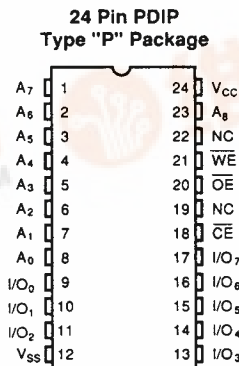
- **Fast Read Access Times**  
— 250ns, 300ns, 350ns, 450ns
- **5 Volt-only Operation**  
— Including Write
- **Fast Nonvolatile Write Cycle**  
— Internally Latched Data and Address  
— 10ms Nonvolatile Write Cycle
- **Automatic Erase Before Write**
- **Automatic Write Timeout**
- **On-chip Inadvertent Write Protection**
- **Unlimited Read Cycle Endurance**
- **10,000 Rewrites per Byte**
- **10 Year Secure Data Retention**
- **TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Memory Pinout**

### OVERVIEW

The XL2804A is a full-featured, 512 x 8 bit E<sup>2</sup>PROM (Electrically Erasable Programmable Read Only Memory). Read access times are as low as 250ns; standby current, less than 40mA. The device is fully functional with a single 5V power supply, and the XL2804A is manufactured with EXEL's 2.5μ NMOS E<sup>2</sup>PROM process.

The sophisticated architecture of this device provides complete and automatic control of the nonvolatile write cycle eliminating the need for external timers, latches, high voltage generators and inadvertent write protection circuitry. It fits into a standard SRAM socket and responds to typical SRAM write commands.

### PIN CONFIGURATION



PARALLEL  
**3**  
 P.DCTS

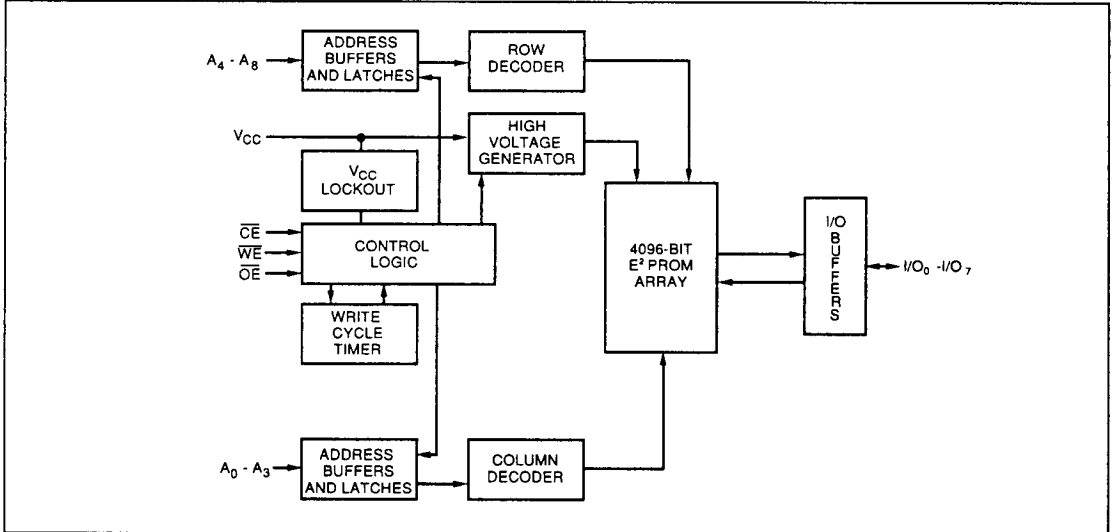
### PIN NAMES

A <sub>0</sub> -A <sub>8</sub>	Address Inputs
I/O <sub>0</sub> -I/O <sub>7</sub>	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V <sub>cc</sub>	Supply Voltage
V <sub>ss</sub>	Power and Signal Ground
NC	No Connect

The XL2804A features  $\overline{OE}$  write inhibit logic and noise protected  $\overline{WE}$ , to inhibit inadvertent writes.

The XL2804A is compatible with industrial standard 512 x 8 E<sup>2</sup>PROMS — its pinouts and operating modes conform to established standards. This compatibility extends to higher and lower density EXEL E<sup>2</sup>PROMS as well.

## BLOCK DIAGRAM



## APPLICATIONS

The XL2804A provides secure and reliable data storage throughout your system's lifetime both during periods of power on and power off. It may be written to through standard microprocessor protocols as if it were a Static RAM, yet it retains its data in the absence of system power for at least 10 years after the data is written. This flexibility has resulted in a wide variety of digital system applications.

The nonvolatile storage in the XL2804A replaces dip switches as a means of storing configuration data. It delivers firmware for booting up systems, and for operating industrial and process controllers, traffic controllers, robotics and telemetry, measuring instruments and appliance controls. It retains phone numbers and messages in facsimile machines. The XL2804A is ideal in applications that are self-adapting such as video games and systems that require automatic re-calibration, as well as those that are subject to power failures.

## ENDURANCE and DATA RETENTION

The XL2804A is designed for applications requiring up to 10,000 data changes per E<sup>2</sup>PROM byte ensuring a guaranteed endurance of 20 million data changes per device. It provides 10 years of secure data retention, with or without power applied after the data is written.

## DEVICE OPERATION-STANDARD MODES

Three control pins ( $\overline{CE}$ ,  $\overline{OE}$  and  $\overline{WE}$ ) select all standard, user operating modes for the XL2804A. Chip erase (typically executed during test procedures) requires a higher supply voltage on one input pin. This conforms with existing E<sup>2</sup>PROM standards.

### Read Mode

Data is read from the XL2804A by bringing both  $\overline{CE}$  and  $\overline{OE}$  LOW while keeping  $\overline{WE}$  HIGH. With the read mode selected, address lines can be changed at any time, in any order to read data at various locations in the E<sup>2</sup>PROM array. Read access time is measured from the time when the final controlling line ( $\overline{CE}$  or  $\overline{OE}$ ) goes LOW, or the time when the address is established.

The device can be read an unlimited number of times, because the stored charge that defines the bit state is not affected by a read cycle. (See Figure 2.)

### Write Mode

In the XL2804A the write cycle is initiated by applying a logical "0" to both  $\overline{WE}$  and  $\overline{CE}$  while  $\overline{OE}$  is logical "1." The address inputs are latched into the device on the falling edge of  $\overline{WE}$  or  $\overline{CE}$  (whichever is last) to specify the address that is to be written. Data on the I/O pins is then latched into the device by bringing either  $\overline{WE}$  or  $\overline{CE}$  HIGH. Both addresses and data are latched in a brief 200ns interval using a 5V supply and TTL write signals. Once the data is latched, the XL2804A will automatically erase the selected byte and write the new data in less than 10ms. The system is therefore freed to proceed with other operations while the XL2804A autonomously executes its internal write cycle. The I/O pins will be in a high impedance state while the write operation is in progress. (See Figures 3 and 4.)

### Output Disable Mode

If, while in the read mode,  $\overline{OE}$  is brought HIGH, the device remains in the read mode, but with the outputs disabled. (I/O pins are in a HIGH impedance state.)

### Standby Mode

Whenever  $\overline{CE}$  is brought HIGH, the device is set into its standby mode, placing the I/O pins in a HIGH impedance state. Standby power dissipation is less than 40mA with TTL level inputs. While  $\overline{CE}$  remains HIGH, all other input pins are disabled, insulating the device from activity on the system busses.

### Chip Erase — High Voltage Mode

The chip erase mode allows the user to erase the entire E<sup>2</sup>PROM array with a single command. The method requires the application of high voltage ( $V_H$ ) on the  $\overline{OE}$  pin, with  $\overline{CE}$  at a logical "0." Chip erase is initiated by a standard byte write command while holding the data on the I/O pins HIGH. A byte containing all "1's" is automatically written to all locations in the E<sup>2</sup>PROM array. (Refer to Mode Selection chart.)

### WRITE PROTECT MECHANISMS

The XL2804A features several integrated mechanisms to protect it from inadvertent writes that might occur during system power supply transitions or periods of system noise. In addition to the user-controlled protection mechanisms, the following specialized circuits are built in.

#### $\overline{OE}$ Write Disable

If  $\overline{OE}$  is brought LOW before the  $\overline{CE}$  and  $\overline{WE}$  write command sequence, the internal nonvolatile write cycle will not occur. See the Mode Selection Table below.

#### Noise Protection

Write pulses of less than 20ns duration on the  $\overline{WE}$  pin will not initiate nonvolatile write cycles.



### MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O	POWER
$V_{IH}$	X	X	Standby	HIGH Z	Standby
$V_{IL}$	$V_{IL}$	$V_{IH}$	Read	DOUT	Active
$V_{IL}$	$V_{IH}$		Byte Write ( $\overline{WE}$ Controlled)	DIN	Active
	$V_{IH}$	$V_{IL}$	Byte Write ( $\overline{CE}$ Controlled)	DIN	Active
$V_{IL}$	$V_H$	$V_{IH}$	Chip Erase*	Data In= $V_{IH}$	Active
X	$V_{IL}$	X	Write Inhibit	—	—

\*Contact EXEL for details.

**ABSOLUTE MAXIMUM RATINGS**

Temperature Under Bias .....	-10°C to +85°C
Storage Temperature .....	-65°C to +120°C
Lead Soldering Temperature (less than 10 seconds) .....	300°C
Supply Voltage .....	0 to 6.5V
Voltage on Any Pin* .....	-0.5V to V <sub>CC</sub> + 0.3V
ESD Rating .....	2000V
DC Output Current .....	5mA

\*With respect to ground

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Although this product includes specific circuitry to protect it from electrostatic discharge, conventional precautions should be taken to protect it from any voltages higher than the rated maxima.

**DC CHARACTERISTICS**

T<sub>A</sub> = 0°C to +70°C, V<sub>CC</sub> = 5V±5% unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Max.	Units
I <sub>CC</sub>	V <sub>CC</sub> Current-Active (TTL)	CE = OE = V <sub>IL</sub> I/O's = open Other Inputs = 5.25V		80	mA
I <sub>SB</sub>	V <sub>CC</sub> Current-Standby (TTL)	CE = V <sub>IH</sub> OE = V <sub>IL</sub> I/O's = open Other Inputs = 5.25V		40	mA
I <sub>LI</sub>	Input Leakage Current	V <sub>IN</sub> = 0 to 5.25V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>OUT</sub> = 0 to 5.25V		±10	μA
V <sub>IL</sub>	Input Low Voltage			0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1mA		0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400μA	2.4		V
V <sub>H</sub>	High Voltage for Chip Erase		15	18	V

**CAPACITANCE**

T<sub>A</sub> = +25°C, f = 1.0 MHz

Symbol	Test	Test Conditions	Max.	Units
C <sub>I/O</sub>	Input/Output Capacitance	V <sub>I/O</sub> = 0V	10	pF
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 0V	6	pF

## AC OPERATING CHARACTERISTICS

### READ CYCLE (See Figure 2)

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$ , unless otherwise specified.

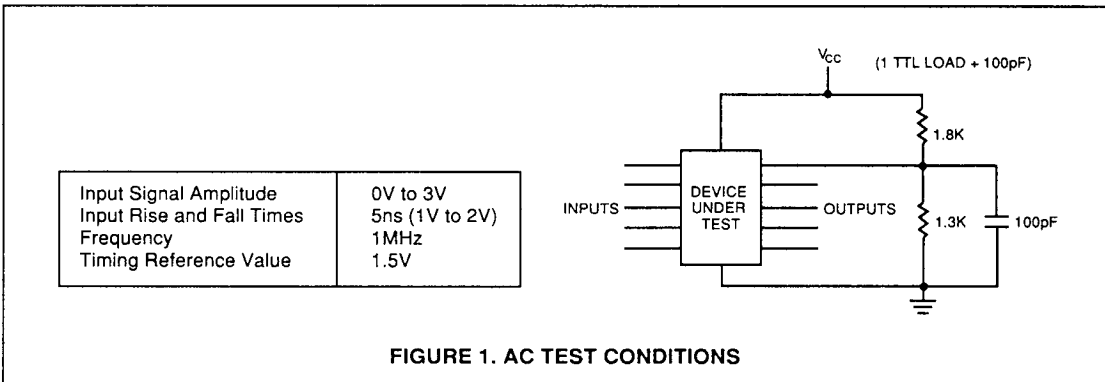
Symbol	Parameter	XL2804A-250 Limits		XL2804A-300 Limits		XL2804A-350 Limits		XL2804A-450 Limits		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
$t_{RC}$	Read Cycle Time	250		300		350		450		ns
$t_{AA}$	Address Access Time		250		300		350		450	ns
$t_{CE}$	Chip Enable Access Time		250		300		350		450	ns
$t_{OE}$	Output Enable Access Time		100		120		135		150	ns
$t_{LZ}$	Chip Enable to Output in Low Z	10		10		10		10		ns
$t_{HZ}$	Chip Disable to Output in High Z	10	100	10	100	10	100	10	100	ns
$t_{OLZ}$	Output Enable to Output in Low Z	10		10		10		10		ns
$t_{OHZ}$	Output Disable to Output in High Z	10	70	10	80	10	100	10	100	ns
$t_{OH}$	Output Hold from Address Change	20		20		20		20		ns

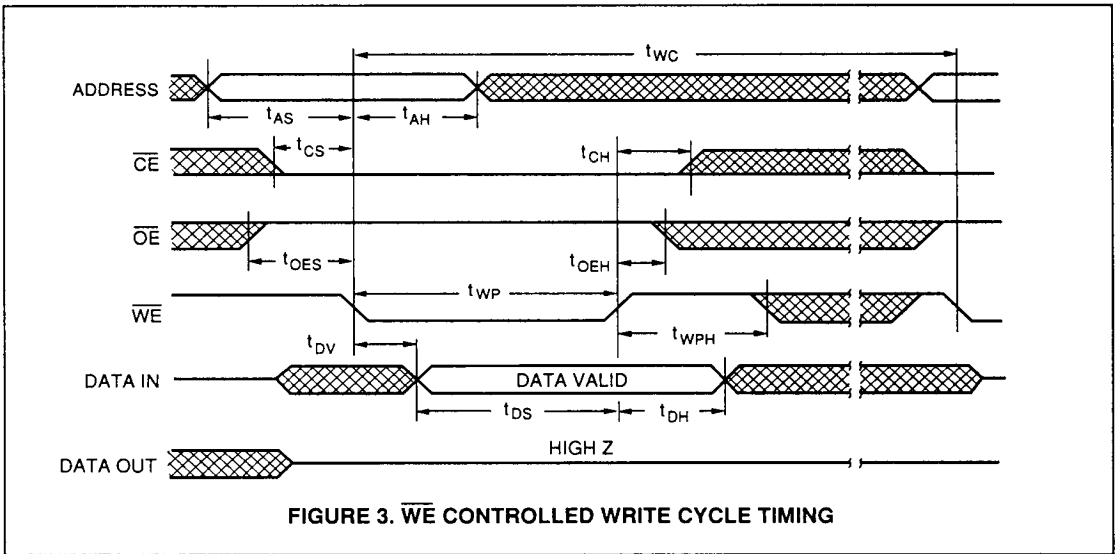
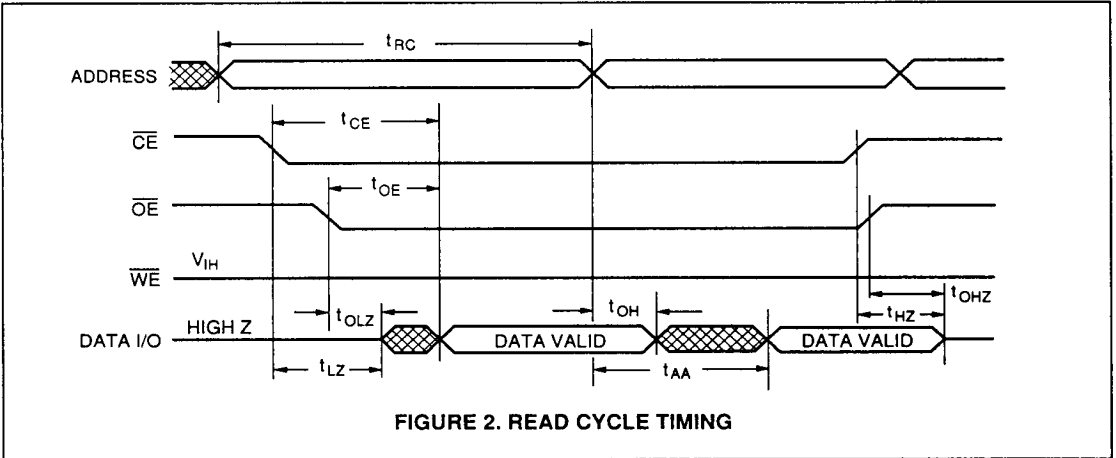
PARALLEL  
**3**  
PODTS

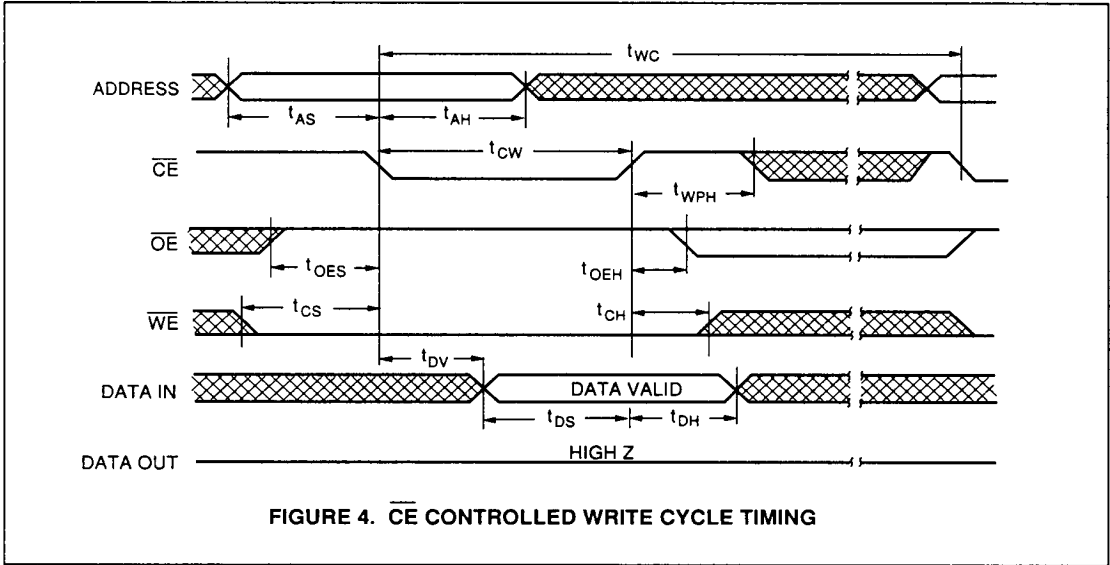
### WRITE CYCLE (See Figures 3 and 4)

$T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 5V \pm 5\%$

Symbol	Parameter	Min.	Max.	Units
$t_{WC}$	Nonvolatile Write Cycle Time		10	ms
$t_{AS}$	Address Setup Time	10		ns
$t_{AH}$	Address Hold Time	70		ns
$t_{CS}$	Chip Enable or Write Setup Time	0		ns
$t_{CH}$	Chip Enable or Write Hold Time	0		ns
$t_{CW}$	Chip Enable to End of Write Input	150		ns
$t_{OES}$	Output Enable Setup Time	10		ns
$t_{OEH}$	Output Enable Hold Time	10		ns
$t_{WPH}$	Write Enable Pulse Width	150		ns
$t_{WPH}$	Write Pulse Recovery	50		ns
$t_{DV}$	Data Valid Time		1	$\mu\text{s}$
$t_{DS}$	Data Setup Time	50		ns
$t_{DH}$	Data Hold Time	10		ns
$t_{INIT}$	Power-up Initialization Period		20	ms







PARALLEL  
**3**  
P DCTS