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MC88200

Technical Summary

16-Kbyte Cache/Memory Management Unit (CMMU)

The MC88200 CMMU is a high-performance, HCMOS VLSI device providing zero-wait-state memory management and data caching. The memory management unit (MMU) efficiently supports a demand-paged virtual memory environment with two logical address ranges (user/supervisor) of 4 Gbytes each. Translated addresses are provided by one of two address translation caches (ATCs), providing address translation in one clock cycle for most memory accesses. The page address translation cache (PATC) is a 56-entry, fully associative cache containing recently used translations for 4-Kbyte memory pages and is maintained by MC88200 hardware. The block address translation cache (BATC) is a 10-entry cache, loaded by software, containing translations for 512-Kbyte memory blocks. The BATC translations are used for operating system software or other memory-resident instructions and data. In addition, the MMU provides access control for the two logical address spaces. The CMMU data cache is a 16-Kbyte, four-way, set-associative cache for instruction or data storage. The cache incorporates memory-update policies and cache-coherency mechanisms that support multiprocessor applications. The MC88200 CMMU also includes an MC88100-compatible processor bus (P-bus) interface and a memory bus (M-bus) interface.

A processor may use two or more CMMUs for increased data cache and ATC sizes.

Features of the MMU portion of the MC88200 include:

- Two Logical Address Spaces of 4 Gbytes Each (User/Supervisor)
- Automatically Maintained PATC and Software-Maintained BATC
- Write Protection for User and Supervisor Accesses
- Used and Modified Flags Maintained in Page Translation Tables
- Probe Capability for Testing the Status of a Memory Location

Features of the cache portion of the MC88200 include:

- 16-Kbyte, Four-Way, Set-Associative Physical Cache
- Zero-Wait-State Physical Cache Accesses — Address Translation in Parallel with Cache Access
- LRU (Least Recently Used) Replacement Algorithm for Each Cache Set
- Cache Entries Allocated with Copyback or Writethrough Policies

Multiprocessor support features include:

- Bus Snoop Protocol Keeps the Cache Consistent with Other Caches and with Main Memory
- Cache Flush and Invalidate Initiated Selectively by Software and Executed Automatically by Hardware
- Cache Inhibit Flags on Area, Segment, Page, and Block Basis
- Cache Writethrough or Copyback Selectable on Area, Segment, Page, and Block Basis
- Semaphores for Efficient Multiprocessor Synchronization (In Memory and Cached)
- Data Cache and ATCs Can Be Flushed by Any Processor or I/O Device

Fault-Tolerance application support features include:

- Checker Mode Fault Detection (Functional Redundancy)
- Parity-Protected Memory Bus
- Cache Line Disable Flags

MC88200 OVERVIEW

The MC88200 incorporates 16 Kbytes of cache memory plus cache control, memory management, and bus control logic into a single component with over 750,000 transistors. This integration allows the MC88200 to provide data or instructions at the peak capacity of the system processor. In addition, the integration lowers system cost and increases reliability. The MC88200 is a fully synchronous component for the MC88100 processor.

The small footprint of the MC88100/MC88200 configuration permits large amounts of memory to be included on the same board, eliminating memory delays across backplane buses. It also allows multiple processing nodes on a single printed circuit board. The memory-update policies and the cache-coherency mechanism enhance multiprocessing capabilities by minimizing memory bus traffic; even when multiple processors access a shared-memory system. These capabilities, coupled with remote cache flushing, in-cache semaphores, and full separation of instructions and data, maximize the memory bus throughput and make the MC88100/MC88200 combination ideal for multiprocessing environments.

The MC88200 has been designed so that multiple CMMUs can be used in parallel, further increasing the ATC and data cache hit rates. In a multiple CMMU configuration, translation cache hit rates also increase since there are more ATC entries. Figure 1 shows an example MC88100/MC88200 system.

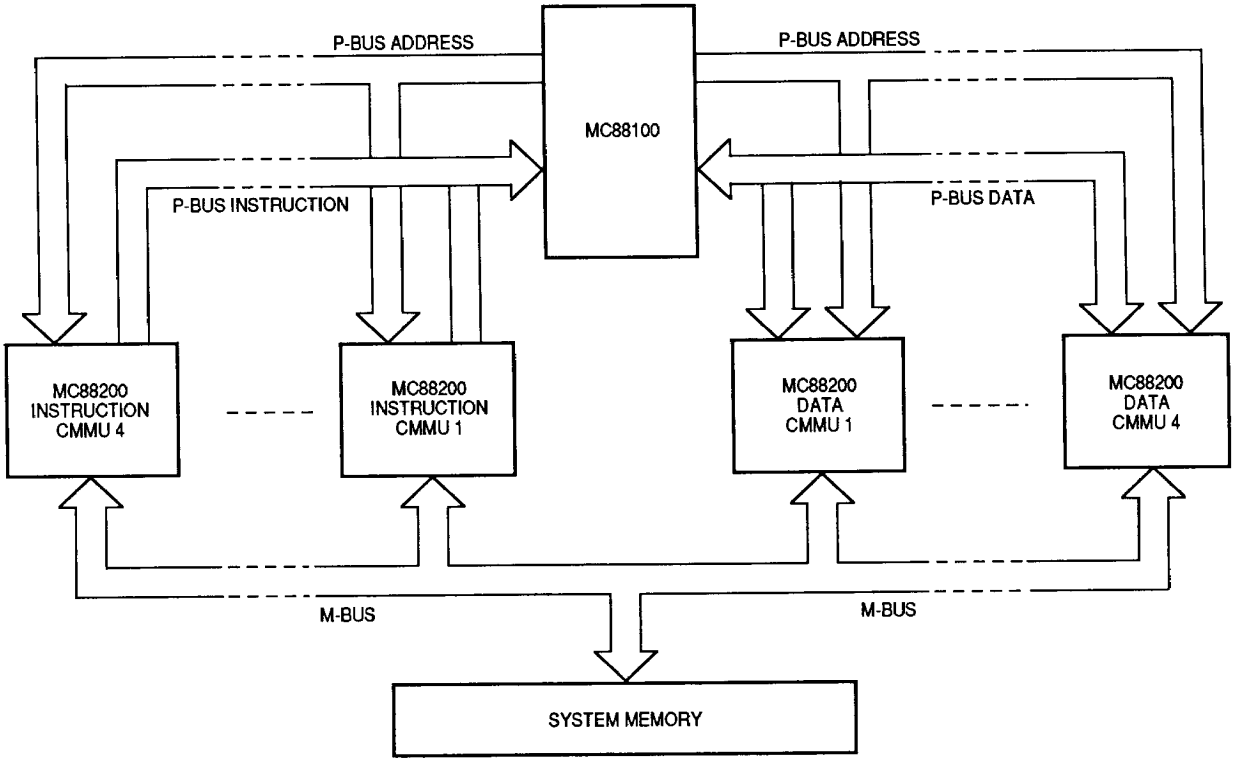


Figure 1. MC88100/MC88200 Example System Diagram

SYSTEM CONFIGURATION

High-performance microprocessor systems require specialized circuitry and/or software to support complex system and application software. These systems require facilities implementing multitasking (the execution of multiple tasks concurrently) and protection (preventing one task from corrupting the memory and resources allocated to another task). If virtual addressing capabilities are needed, large amounts of complex hardware and software are normally required to implement a demand-paged virtual memory system.

The MC88200 provides the mapping and protection facilities needed to construct a multitasking, demand-paged virtual memory system. The MC88200 resides logically between the processor and the physical memory as shown in Figure 2. The "logical" address output by the processor is received by the MC88200 on its P-bus address inputs. The MC88200 performs translation and privilege checking for the logical address and, if the logical address is valid, outputs the translated "physical" address on the memory bus (M-bus). This physical address is used to access memory or other physical devices. At the same time that it performs the translation, the MC88200 checks the on-chip data cache. If the data requested by the processor is in the cache, then the MC88200 returns the cached data to the processor instead of accessing physical memory. This reduces the processor's memory access time to a single clock cycle.

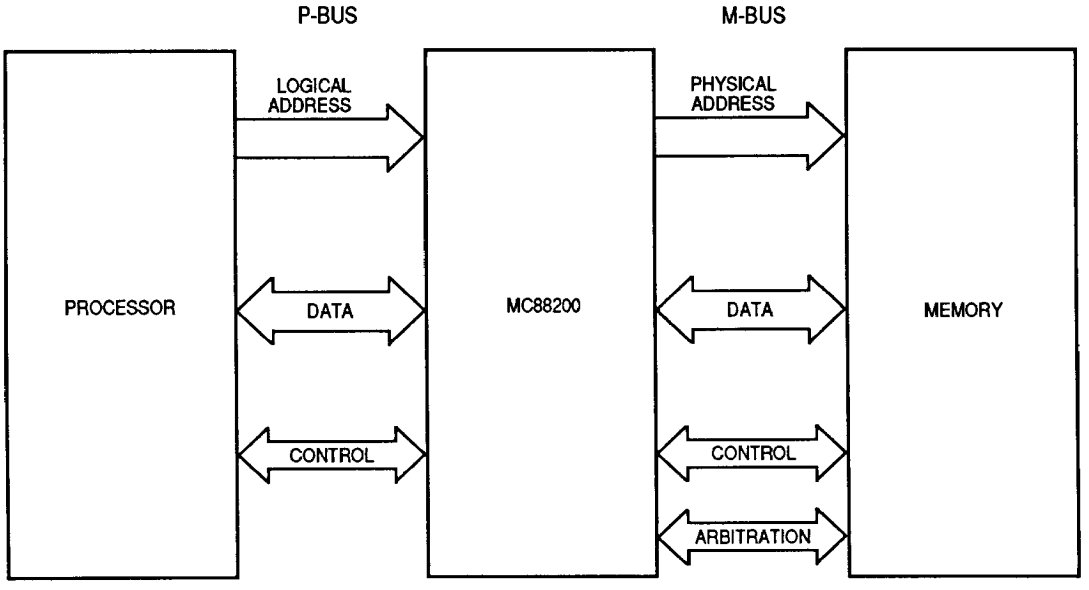


Figure 2. MC88200 Logical Block Diagram

In this configuration, the MC88200 controls all accesses to physical devices; tasks can be prevented from accessing the resources owned by other tasks. Under control of an operating system with virtual memory capabilities, the logical-to-physical mapping functions allow tasks to utilize the entire address space of the CPU without detailed knowledge of the system.

MEMORY MANAGEMENT UNIT

The MMU translates logical addresses into physical addresses. The memory management scheme allows the processor to use two logical address ranges (user/supervisor) of 4 Gbytes each without requiring physical memory of that size. Two ATCs provide high-speed, logical-to-physical address translation. The PATC is a 56-entry, fully associative cache containing descriptors for 4-Kbyte pages in memory. The BATC is a 10-entry cache containing memory block descriptors (512-Kbyte blocks in memory).

When the processor initiates a memory access that does not have a corresponding translation resident in either ATC, the MC88200 automatically loads the translation for the memory access into the PATC. The MC88200 locates the address translation for the new PATC entry by searching address translation tables resident in physical memory. These tables partition memory into discrete units and contain the physical addresses for the 4-Kbyte memory pages. These tables also include protection and control information for the representative memory sections; this information is accumulated and incorporated into the new PATC entry. Once a PATC entry is allocated, the address translation is repeated through the PATC.

Most address translations are performed in a single clock cycle; the remaining translations (requiring access to external translation tables) are located automatically by the CMMU hardware. This translation mechanism provides the highest memory management performance without additional hardware or intervening software.

ADDRESS TRANSLATION CACHES

Each ATC is fully associative; ATC entries contain the logical address, the corresponding physical translation, and status and protection information. When a bus cycle is initiated by the processor, the logical address (received over the P-bus) is input to the ATCs where it is simultaneously compared to all current entries. If the

logical address matches one of the ATC entries (there is a "hit"), the MC88200 concatenates the stored physical base address with the low-order word-offset from the logical address to form the complete physical address. If there is a hit in both ATCs, the BATC translation takes precedence. Figure 3 shows the ATC organization.

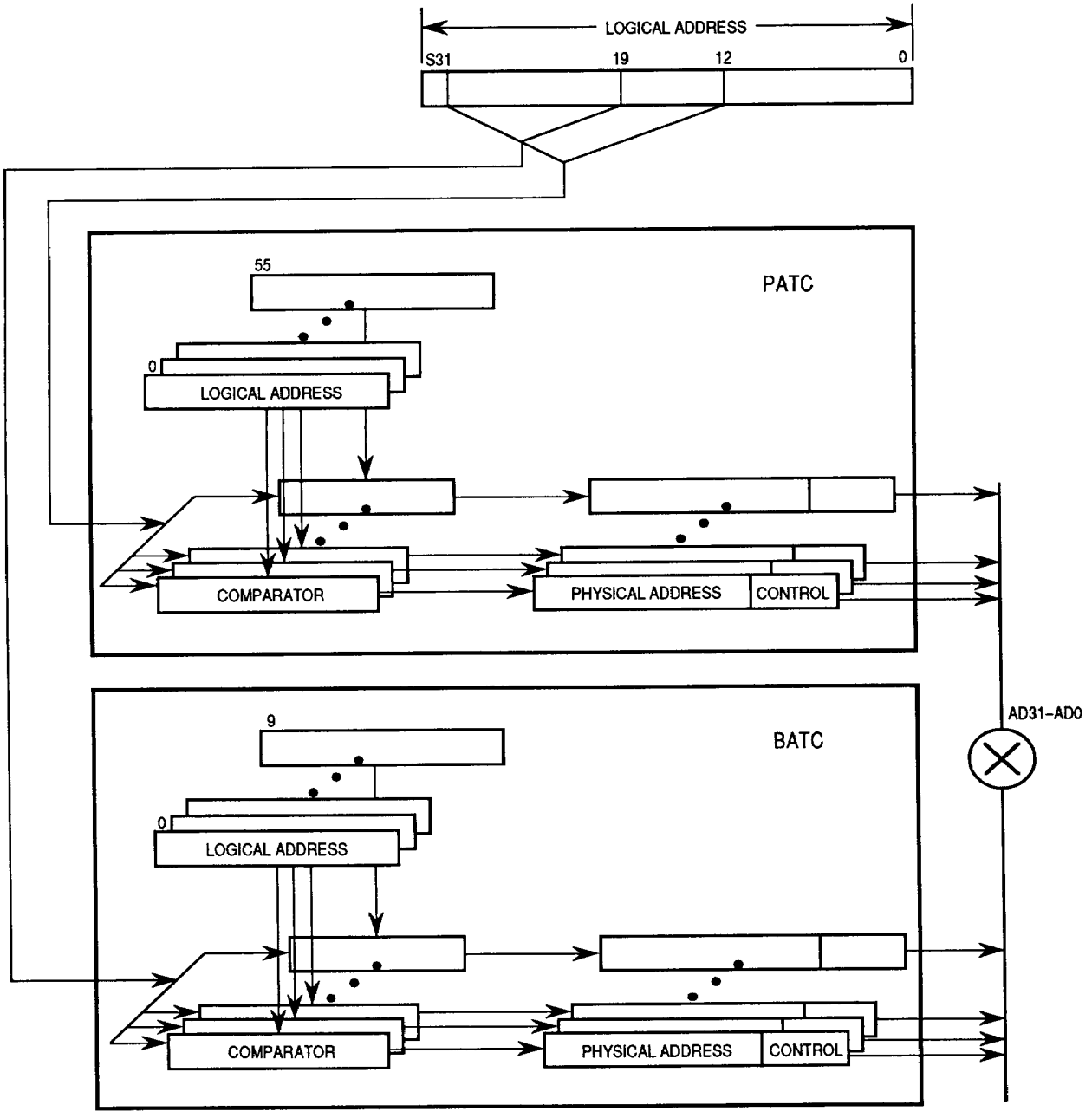


Figure 3. ATC Organization

The status and protection information includes the protection attributes for that mapping (e.g., write and/or supervisor protected), a data cache inhibit indicator, and other protection and control information. Before an address is translated through the ATC, the MC88200 checks the protection information. If the transaction

conflicts with the protection (e.g., write to write-protected memory), the memory transaction is aborted with a fault, and the translation is not performed. The address and status registers are updated with information concerning the fault.

The ATCs eliminate many of the memory accesses required for translation table searches. This significantly improves the performance of the CMMU and reduces memory bus bandwidth requirements.

Block Address Translation Cache (BATC)

The BATC provides translations for ten 512-Kbyte blocks of memory. System software loads eight of the ten BATC entries with the logical and physical addresses of the memory blocks. Normally, these blocks contain the operating system kernel or other high-use software. Since these are high-use blocks, performance is optimized because ATC misses and translation table searches are eliminated for a large number of memory accesses. The two remaining BATC entries are hardwired providing a one-to-one (identity) mapping in the upper 1 Mbyte of physical memory. This 1 Mbyte of memory, called the control memory space, is reserved for memory-mapped peripherals and I/O devices.

Page Address Translation Cache (PATC)

The PATC is a fully associative cache containing translations for 56 4-Kbyte pages. The PATC is automatically maintained by the MC88200. If a memory access misses in both ATCs, then a PATC entry is created by a translation table search. Once a PATC entry is created, all translations for that page are performed by the PATC until the entry is replaced or invalidated.

ADDRESS TRANSLATION TABLES

When the processor initiates a memory access that does not have a corresponding translation resident in either ATC, the MC88200 loads the translation for that access into the PATC. The MC88200 automatically searches address translation tables resident in physical memory to locate the address translation. No software assistance or external hardware is required to perform the table search.

When the MC88200 performs a translation table search, it simultaneously delays the processor's memory transaction (P-bus "wait" reply) and requests ownership of the M-bus. When the M-bus is available, the MC88200 completes the bus arbitration sequence, assumes M-bus ownership, and searches the translation tables. If no exception conditions occur, the required translation descriptor is loaded into the PATC. The MC88200 then completes the memory access, using the physical address translated through the PATC. When the memory access is complete, the MC88200 signals the processor that the memory transaction was successful (P-bus "success" reply).

The translation tables describe the logical-to-physical mappings to the MC88200. These tables are organized into a tree structure in the physical address space (see Figure 4). The operating system initializes the tables; the MC88200 accesses the tables to obtain translation information and maintain status information. The tree structure supported by the MC88200 contains two distinct levels in the supervisor and user address space:

1. The segment level divides each of the two 4-Gbyte logical address spaces (supervisor/user) into 1024 equivalent 4-Mbyte segments.
2. The page level divides each segment into 1024 equivalent page frames, each 4 Kbytes in size.

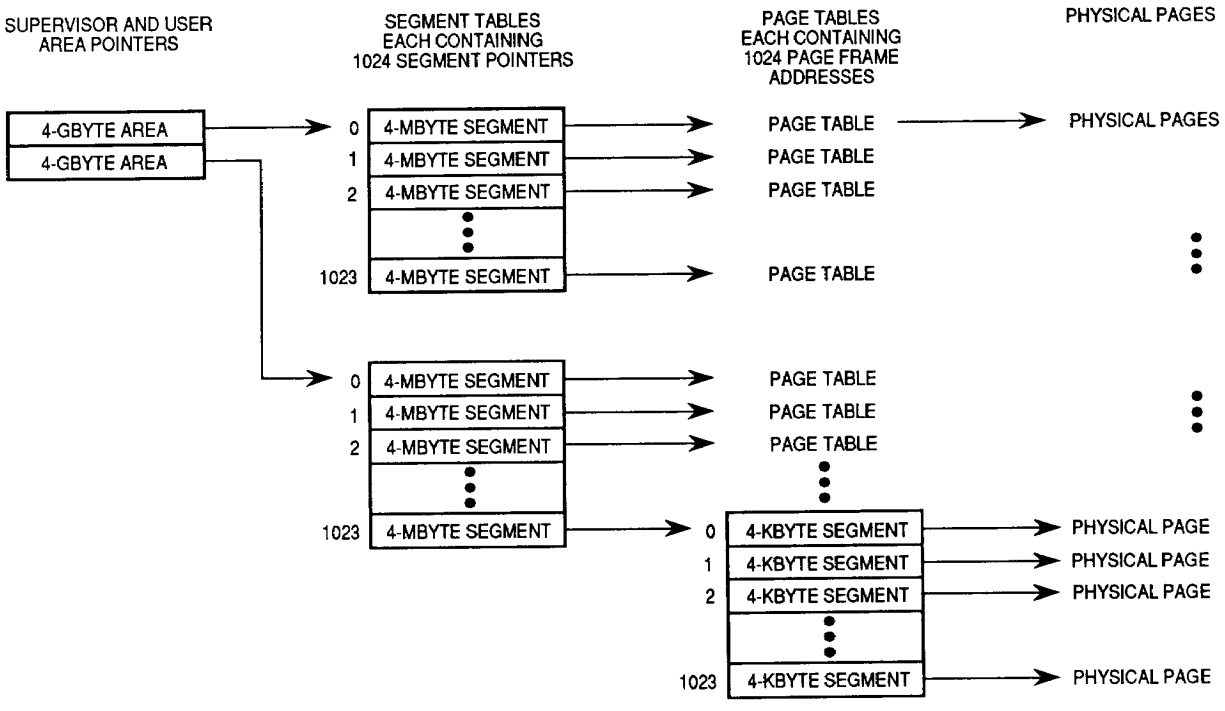


Figure 4. Translation Table Organization

The tree structure allows the MC88200 to maintain only the required working set of translation tables; physical memory does not have to be allocated to tables corresponding to unused portions of the logical address space. The tables and entries can be dynamically configured to meet the requirements of the operating system and the availability of physical memory.

Translation Descriptors

The translation descriptors contain a pointer to the next level in the translation hierarchy, either another translation table or a physical page. They also contain control and protection information for the corresponding portions of memory. System software initializes the descriptors as required (i.e., at system initialization or on demand) with appropriate addresses and information. The software can modify the descriptors as needed during operation.

The area descriptors contain the base address of the segment tables. The MC88200 contains the user and the supervisor area descriptors in the two area pointer registers. The descriptors also contain the area control information, which includes the translation enable bits (set when the area descriptors are located to enable address translation for that area).

Each segment descriptor contains the base address of a page table. In addition, each segment descriptor contains segment-level protection and control information.

Each page descriptor contains the address of a physical page frame into which 4 Kbytes of logical addresses are mapped. In addition, each descriptor contains page-level protection and control information.

Table Search Algorithm

In response to a PATC miss, the MC88200 searches the address translation tables to locate the appropriate logical-to-physical mapping. Control and protection information is accumulated from each descriptor for inclusion in the PATC entry. After the new PATC entry is allocated, the MC88200 translates the address through the PATC.

During the table search operation, several fault conditions can occur; invalid segment descriptor (segment fault), invalid page descriptor (page fault), supervisor protection violation, write protection violation, or bus error. When any of these conditions occur, the MC88200 terminates the table search and reports the fault to the processor. The address and status registers are updated with information pertaining to the fault.

ACCESS PROTECTION

The MC88200 protection mechanism provides privilege and write protection for the physical address space. The logical address space is partitioned into supervisor and user spaces; the supervisor address space is privileged and user address space is unprivileged. The privilege levels allow a system to be built with protection from accidental or malicious corruption. The processor accesses either supervisor or user memory according to its current operating state (reflected by the P-bus S/U signal); the MC88200 automatically enforces the proper access rights. Any segment, page, or block may be write-protected or declared supervisor only.

The descriptors in the address translation tables contain information that indicates the protection at each particular level of the table structure. During a table search operation, the protection attributes at each level of the table structure are logically ORed to form the protection for the physical address. For example, if a segment or a page descriptor indicates write protection, then the physical address mapped by those descriptors is write-protected. When the MC88200 detects a write transaction to a write-protected address, it aborts the transaction and signals a fault to the processor (write-protection violation). Similarly, when the MC88200 detects a user access to a supervisor-protected address, it signals a privilege-violation fault to the processor. Whenever a fault occurs, address and status registers are updated with information pertaining to the fault.

DATA CACHE

Due to locality of reference, instructions and data that are used in a program have a high probability of being reused within a short time. Additionally, instructions and data that reside in proximity to the instructions and data currently in use have a high probability of being used within a short period of time. To exploit these locality characteristics, the MC88200 contains a 16-Kbyte cache.

The cache improves the overall system performance by reducing average memory access time, by reducing the number of M-bus cycles required to access memory, and by increasing the bus bandwidth available to other M-bus masters. The MC88200 data cache includes the ability to designate certain parts of memory as uncachable and a choice of memory-update mechanisms. In the copyback mode, memory is updated only when a cache line is replaced by other data. In the writethrough mode, memory is updated whenever the cache is updated by a write transaction. The MC88200 can be programmed to monitor M-bus transactions performed by other M-bus masters. If another bus master accesses data cached by the MC88200, the MC88200 pre-empts the transaction, takes control of the M-bus, and then updates memory with the cached data. After external memory is updated, the other M-bus device retries its transaction, now accessing the correct data.

Figure 5 shows the organization of the MC88200 cache. The four-way set-associative cache is configured as 256 sets of four lines each. Each line contains four 32-bit words. When the processor initiates a memory

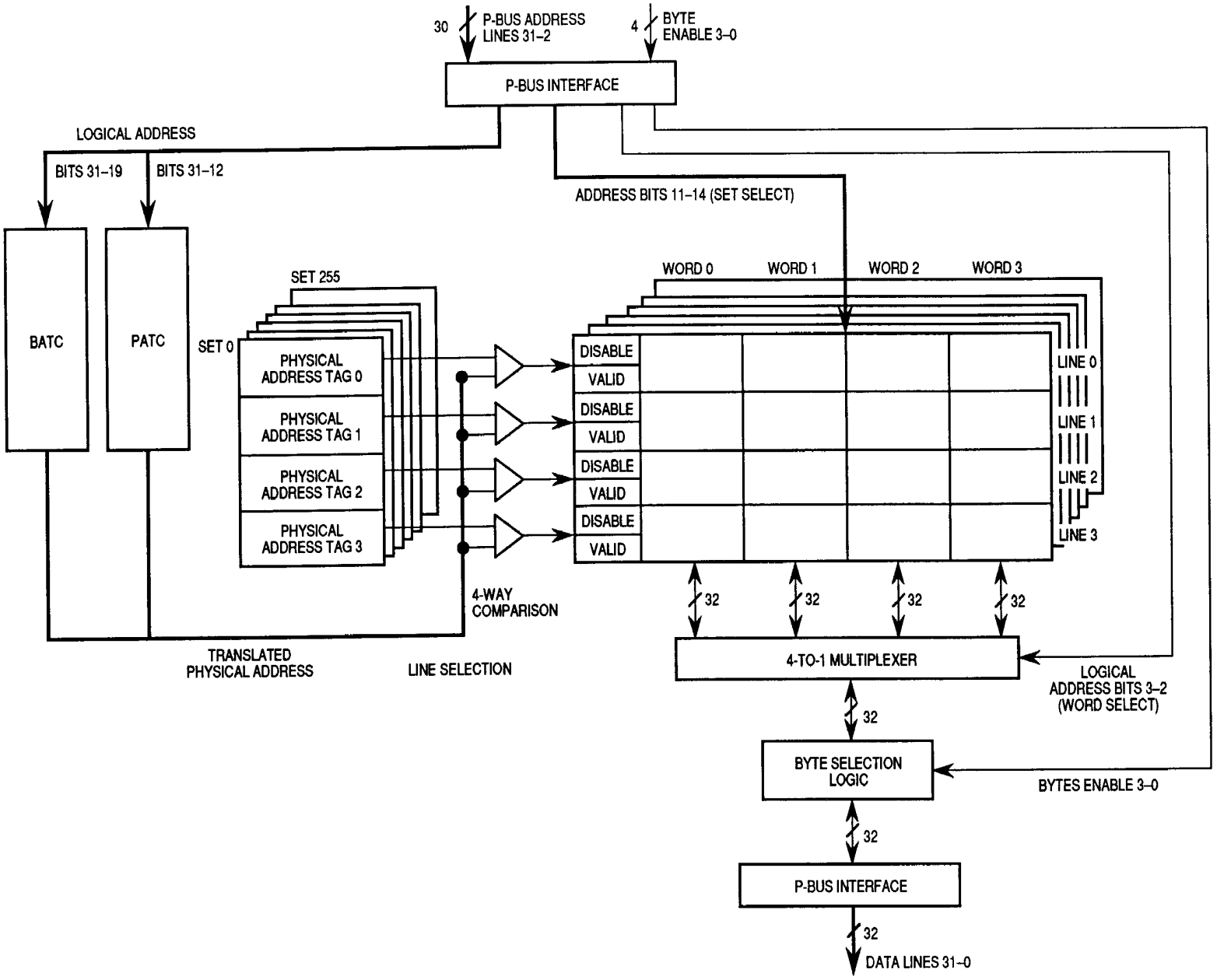


Figure 5. Data Cache

access, the MC88200 selects a cache set using the low-order bits of the logical address. Simultaneously, the MC88200 translates the logical address into a physical address. The physical address is compared to the four address tags in the cache set; if there is a match, the memory access is completed using the corresponding cached data. If there is no match, the MC88200 performs a memory access and loads the data into the cache (unless the address is cache inhibited). The MC88200 selects a line in the set for replacement that is unused or least recently used (LRU replacement algorithm). The selected line is loaded with the data read from physical memory; if the memory transaction was a write transaction, then the cached data is updated. The MC88200 fills an entire cache line using a four-word burst-mode transaction. The burst mode of operation not only fills the cache efficiently, but also captures adjacent instructions or data that are likely to be used in the near future due to locality of reference.

CACHE MEMORY ORGANIZATION

A cache line contains four contiguous words from memory. Cache loads are always performed on a line basis to/from a modulo 4 address. This load scheme optimizes the cache hit rate and bus utilization. Processor accesses to the cached data are designed to match the data types supported by the MC88100 processor; byte (8 bits), half-word (16 bits), word (32 bits), and double word (64 bits).

The status information indicates whether the data is valid or invalid, whether the data is exclusive to the MC88200 cache or resides in other caches, and whether or not the data is modified with respect to memory.

Each line in the cache has an associated address tag. The tag contains a 20-bit physical address that corresponds to the data/instruction address in physical memory. When a memory location is accessed, the tag is used to determine if there is cached data corresponding to the memory location.

When the MC88200 performs a memory access, it loads the cache line (unless the address used is cache inhibited) containing the data that was accessed. At the same time, it loads the cache tag with the upper 20 bits of the translated physical address. If the physical address was translated through the BATC, the address tag contains the 13-bit physical block address with the upper 7 bits of the block offset concatenated. If the physical address was translated through the PATC, the address tag contains the 20-bit page-frame address. If the cache set is full when the MC88200 loads a line, the MC88200 selects the least recently used line for replacement (LRU algorithm).

The disable bit is used for cache-line fault tolerance. The MC88200 provides facilities for testing each line of the cache and determining if it is operational. If a cache line causes errors, then software disables the line by setting the disable bit. The rest of the cache is unaffected.

MEMORY-UPDATE POLICY

The MC88200 provides two methods of updating memory: copyback and writethrough. Each policy provides particular advantages. In the copyback mode, cache writes are written to memory the first time the cached data is written; then updates are not written to memory until the cache line is flushed (write-once). This mode reduces M-bus traffic and increases the speed of write transactions. The disadvantage of copyback mode is that memory data is not always updated, implying that if snooping is disabled, another M-bus device might access old data. In writethrough mode, a cache line is written to memory whenever it is modified. With this mode, the memory data is always valid, so that other M-bus devices can access the data and be assured of accessing correct data.

The memory-update policy is controlled by a flag in the BATC or PATC entry used to translate the physical address.

CACHE ACCESS

Each time the processor performs a P-bus transaction with the MC88200, the MC88200 initiates a data cache operation. The MC88200 performs the cache operation at the same time that it performs the address translation. To achieve this concurrency, the MC88200 exploits the fact that the low-order 12 bits of an address are the same for both the logical and physical address. Eight of these bits select the cache set. Since these bits do not have to be translated, set selection occurs in parallel with the address translation (done by the MMU).

Once the physical address is available, the upper 20 bits are compared to the four address tags in the selected set. If there is a match, the processor's transaction accesses the cache. If there is a miss, the MC88200 accesses physical memory to load a cache line. When the line is loaded, the processor's transaction accesses the cache.

Certain addresses can be designated as cache inhibited. If a P-bus address is cache inhibited and a cache hit occurs, then the cached data is invalidated without a copyback. The MC88200 performs an M-bus transaction to fulfill the processor request, and the accessed data is not loaded into the cache.

LINE REPLACEMENT ALGORITHM

The data cache is equipped with an LRU register for each of its 256 sets. When a cache miss occurs, the cache replacement algorithm first determines if any of the lines in the selected set contain invalid data. If so, those lines are loaded first. Otherwise, the least recently used line is selected and is examined to determine if it contains modified data. After writing back the modified data to memory (if required), the line is updated with the new data.

CACHE COHERENCY

The MC88200 provides the capability to monitor or "snoop" the M-bus transactions of other devices in order to provide cache coherency in a multiprocessing environment. When the MC88200 is not the M-bus master, it monitors all global transactions of other M-bus masters to ensure that cached data remains consistent with main memory. When an M-bus device accesses information that is resident in the MC88200 cache, the MC88200 pre-empts the access and updates its cache and main memory as appropriate to ensure data consistency.

PROGRAMMING MODEL

The MC88200 contains four types of registers:

1. The local registers provide exception information to the local (P-bus) processor. These registers are local because the exception information pertains strictly to the local processor. These exceptions result from the MC88100 processor executing an **ld** (load) **st** (store), or **xmem** (exchange memory) instruction.
2. The system interface registers provide command entry and status registers for various MC88200 operations (probe memory location, flush cache, etc.). In addition, they include the two area pointers which define the supervisor and user memory areas.
3. The BATC write ports provide the address load ports for the block address translation cache.
4. The cache diagnostic ports provide data exchange points and status information about the data cache sets.

The MC88200 registers reside in one page (4 Kbytes) in the control memory address space. The register base address includes an 8-bit device ID field that is programmed into the CMMU ID register. Since the

device ID is programmable, MC88200s can be dynamically reconfigured by either P-bus or M-bus masters. Figure 6 shows the MC88200 programming model; Table 1 summarizes the register functions.

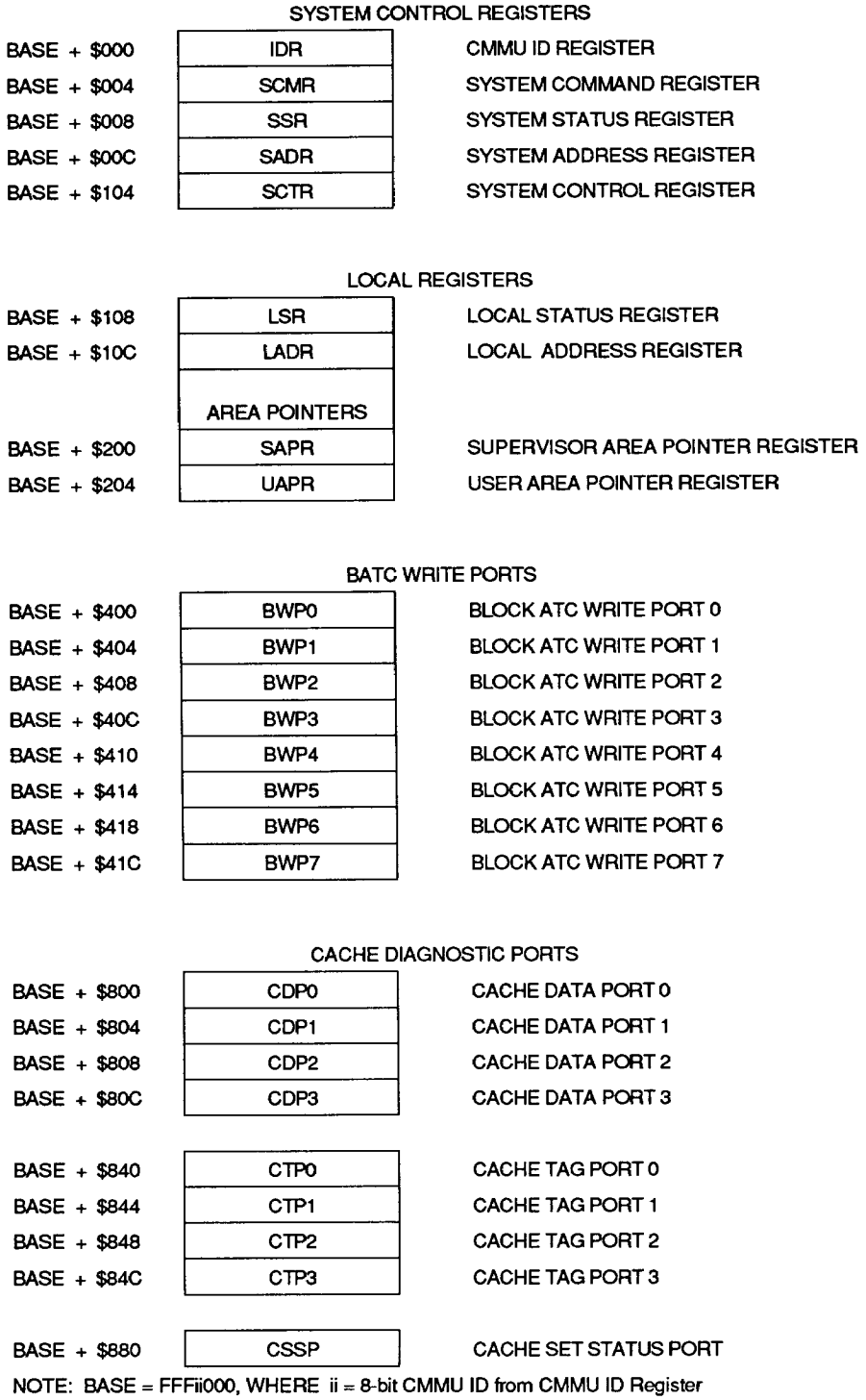


Figure 6. MC88200 Programming Model

Table 1. MC88200 Register Summary

Register	Title	Function	Access
IDR	ID Register	Contains the device type code and defines the MC88200 device address in the control memory space	Read Only
LSR	Local Status Register	Indicates P-bus exception or results of a probe transaction	Read Only
LAR	Local Address	Indicates the physical address of a P-bus exception	Read Only
SCMR	System Command Register	Programmed with MC88200 commands for probe transactions, ATC flushes, and cache flushes	Write Only
SSR	System Status Register	Indicates probe results, M-bus error, data copyback error, and data cache flush error	Read Only
SADR	System Address Register	Written to pass addresses for MC88200 commands; read to obtain address where an M-bus error occurred	Read/Write
SCTR	System Control Register	Programmed with parity enable, memory coherence policy, and bus arbitration scheme	Write Only
SAPR	Supervisor Area Pointer Register	Written with area pointer and control/ protection information for supervisor address space	Write Only
UAPR	User Area Pointer Register	Written with area pointer and control/ protection information for user address space	Write Only
BWP0–BWP7	BATC Write Ports	Written to load address translations into the BATC	Write Only
CTP0–CTP3	Cache Tag Ports	Provide access to the cache tags of a set for diagnostic purposes	Read/Write
CDP0–CDP3	Cache Data Ports	Provide access to the words in a cache set for diagnostic purposes	Read/Write
CSSP	Cache Set	Provide access to the LRU information, disable bits, and line status of a cache set for diagnostic purposes	Read/Write

CMMU P-BUS INTERFACE

The processor bus (P-bus) is a synchronous bus with dedicated address and data buses.

The processor bus (P-bus) is the dedicated communication link between a single MC88100 processor and either a single or a parallel cluster of MC88200 CMMUs. The bus protocol is pipelined and optimized to provide the processor with either code or data at a peak rate of one word per cycle (80 Mbytes/sec at 20 MHz). Full 32-bit addressing and 32-bit data transfers are supported.

CMMU M-BUS INTERFACE

The M-bus (memory bus) is a synchronous 32-bit bus with multiplexed address and data. The CMMU M-bus interface maintains sufficient control signals to specify read and write operations, to establish exclusive resource usage (locks), to inhibit external caching, to signal bus errors, and to provide initialization. In addition, the CMMU can function as a master or a slave device. The CMMU acts as a slave when the CMMU control registers are being read or written via M-bus transactions. The CMMU acts as a bus master when accessing memory.

CMMU FAULT DETECTION

Every output signal on the MC88100 processor and the MC88200 CMMU has a comparator circuit to check that the signal on the output pin is the same as the input signal to the driver. An ERR (error detect) signal is asserted when any of the circuits finds a mismatch. ERR is valid one clock after the mismatch occurs.

In addition, each bus on the CMMU has a checker mode input that disables the device from driving output signals. This allows a configuration (such as that shown in Figure 7) in which the active (master) component is coupled to one or more checker components. The checker components have access to the input code and data stream, and execute concurrently in lock step to compare output results. Checker components check every output signal but do not drive the signals. If the checker component detects a difference between the master component's results and its own results, it asserts the ERR signal to indicate that an error has been detected.

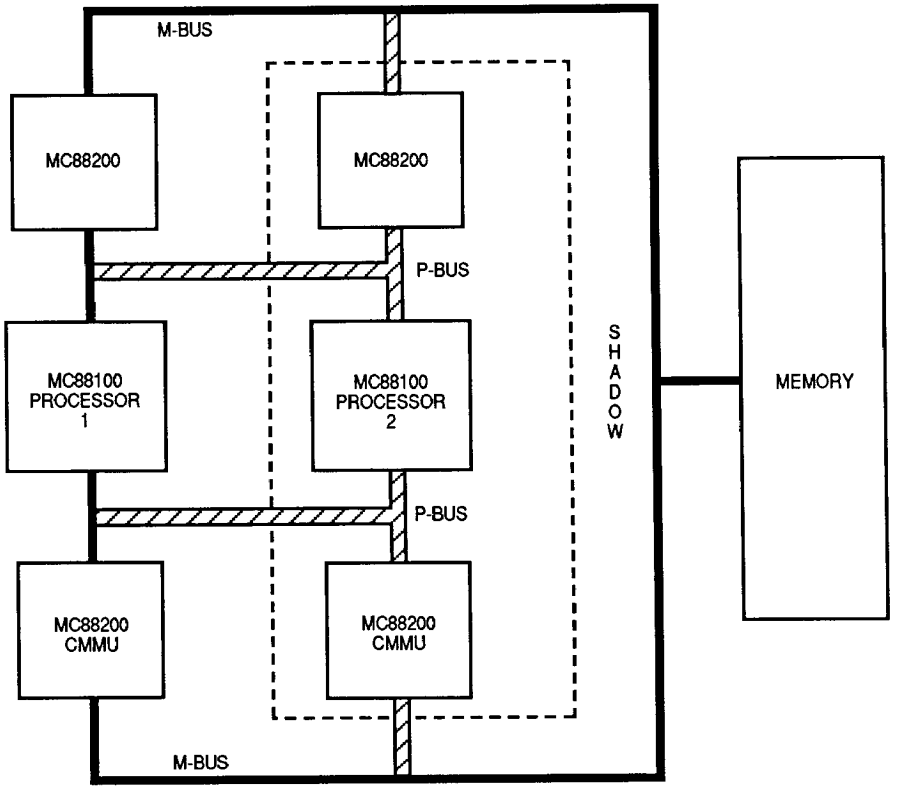


Figure 7. Example Fault-Detection Configuration—M-bus Shadowing

SIGNAL DESCRIPTION

Table 2 lists the MC88200 signals. Figure 8 shows the functional organization of these signals.

Table 2. MC88200 Signal Summary

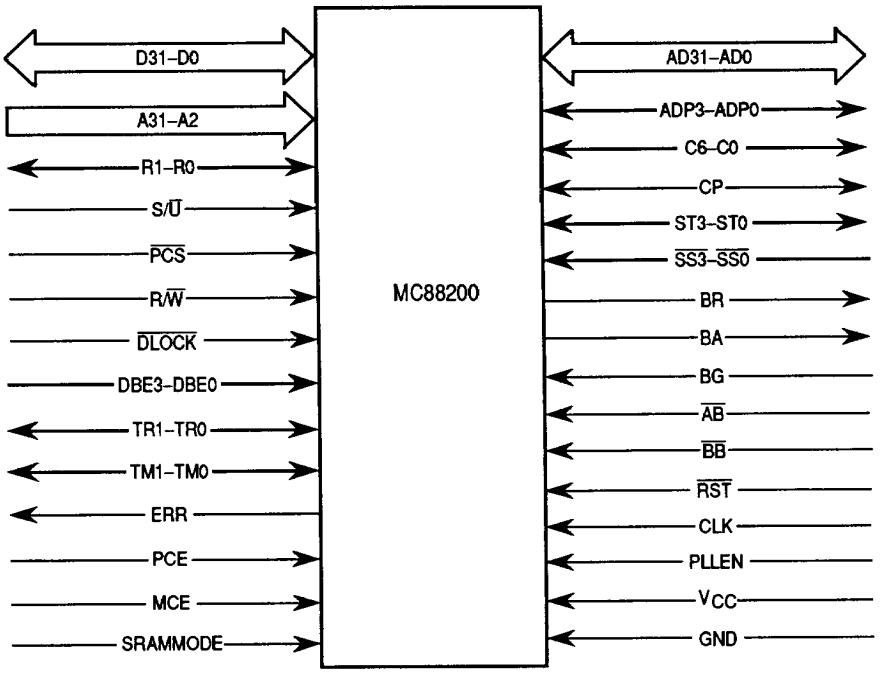
Signal Name	Mnemonic	Function
P-bus Data	D31–D0	These bidirectional three-state signals provide the data or instruction transfer paths between the processor and the MC88200.
P-bus Address	A31–A2	These inputs provide the 30-bit word address for memory accesses. Since MC88100 instructions are word aligned, the two least significant bits of the address are not needed for instruction fetches. For data accesses, the data byte enable signals specify the required byte or half-word.
P-bus Reply	R1–R0	These three-state outputs provide the status of the P-bus transaction to the processor. These signals are encoded to indicate responses of success (transaction complete), wait (transaction delayed), and fault (transaction aborted).
P-bus Supervisor/User	S/$\overline{U}$	The S/$\overline{U}$ input selects the supervisor or user address space. The MC88200 uses this signal to determine which memory area the P-bus (logical) access pertains to, or to select the supervisor or user area pointer at the beginning of a translation table search.
P-bus Chip Select	$\overline{PCS}$	This active-low input selects the MC88200 as a P-bus slave. When multiple MC88200s reside on the P-bus, external circuitry is needed to decode the chip select signal from the P-bus address lines.
P-bus Read/Write	R/$\overline{W}$	The read/write input indicates the type of memory transaction. If the MC88200 is used as an instruction memory controller, this signal can be tied high since all memory accesses are reads (instruction fetches).
P-bus Lock	$\overline{DLOCK}$	The P-bus lock input is the transaction lock signal. When $\overline{DLOCK}$ is asserted, the MC88200 retains M-bus ownership and bypasses the data cache. $\overline{DLOCK}$ prevents the data access from being interrupted, which guarantees that the memory location will not be changed between the load and store parts of the **xmem** instruction.
P-bus Data Byte Enable	DBE3–DBE0	These active-high inputs indicate which bytes of an addressed location are used during the memory access. If one signal is active, a single byte is used; if two signals are active, a half-word is used. When all four signals are active, the transaction is a word transaction.
M-bus Address/Data	AD31–AD0	These bidirectional three-state signals form the multiplexed address/data bus. The function of these signals depends on the M-bus transaction phase (defined by the M-bus control signals). During the request phase, the MC88200 drives the 30 most significant bits of the physical address onto AD31–AD2 (AD1 and AD0 are not used). During the data phase, AD31–AD0 are the data input/output lines.
M-bus Address/Data Parity	ADP3–ADP0	These active-high bidirectional signals indicate the parity of the M-bus address/data lines. The MC88200 always uses even parity, checking parity on reads and generating parity for addresses and memory writes. Each parity signal is associated with one byte of the address/data bus.
M-bus Control	C6–C0	When the MC88200 is the bus master, these active-high outputs define the transaction phase and type of transaction. The C0 signal defines whether the phase is address (address on AD31–AD2) or data (data on AD31–AD0). During the address phase, C1–C5 indicate intent to modify, read/write, M-bus lock, cache inhibit, and global address. During the data phase, C1–C5 indicate end-of-request, read/write, and selected bytes. These signals are inputs during M-bus snooping and when the MC88200 is accessed as a slave device.
M-bus Control Parity	CP	When the MC88200 is the M-bus master, this active-high output indicates the even parity of the M-bus control signals.

Table 2. MC88200 Signal Summary (Continued)

Signal Name	Mnemonic	Function
M-bus Local Status	ST3–ST0	These bidirectional active-high signals indicate the local M-bus status when the MC88200 is being accessed as a slave device (register access), or when the MC88200 is snooping a global M-bus transaction. These signals are inputs during reset and are used to intialize the CMMU ID register.
M-bus System Status	$\overline{SS3}$–$\overline{SS0}$	These active-low inputs are the reply generated by M-bus slaves in response to the MC88200 address and data phases.
M-bus Request	BR	This active-high output is asserted by the MC88200 to request M-bus ownership.
M-bus Grant	BG	The M-bus arbitration logic generates this active-high input in response to a bus request. The MC88200 recognizes this signal only if the M-bus is not busy ($\overline{BB}$ signal negated).
M-bus Acknowledge	BA	Bus acknowledge is an active-high output asserted by the MC88200 when it has received a bus grant in response to a bus request. This signal allows the MC88200 to accept and maintain bus ownership while making memory accesses.
M-bus Busy	$\overline{BB}$	This active-low input indicates that some other M-bus device is currently the bus master; it qualifies the bus grant signal. For an MC88200 to become the bus master, it must receive a bus grant signal from the arbitration logic, and $\overline{BB}$ must be negated (no other device is the M-bus master).
M-bus Arbitration Busy	$\overline{AB}$	This active-low input indicates that one or more M-bus devices are performing a bus request. It is an input to the MC88200 that indicates contention for bus ownership is taking place.
Trace	TR1–TR0	These bidirectional signals perform several functions during MC88200 operation. During normal operation, these signals are output by the MC88200 to indicate which line of a cache set is being accessed. (The tag monitor signals indicate what type of access is being made.) During cache test operations, these signals are MC88200 inputs which select the data line to be tested in a particular cache set. During reset, these signals are MC88200 inputs used to initialize the CMMU ID register.
Tag Monitor	TM1-TM0	These bidirectional active-high outputs provide information about the address tags associated with each line in the cache. The encoded values on these signals indicate when an address tag is loaded, invalidated, etc. TM0-TM1 allow external logic to maintain duplicates of the data cache address tags by indicating when changes are made to the tags.
Error	ERR	This active-high signal is output when a bus comparator error occurs. This signal is asserted by internal bus checking circuitry or by the checker MC88200 in master/checker configurations.
P-bus Checker Enable	PCE	This active-high input determines the operational mode (master/checker) of the MC88200 P-bus. In the checker mode of operation, all P-bus signals are placed in the high-impedance state and all P-bus outputs are monitored as inputs. The master operates normally. The checker compares its internal results with the results read as inputs. If a mismatch occurs, the checker asserts ERR.
M-bus Checker Enable	MCE	This active-high input determines the operational mode (master/checker) of the MC88200 M-bus. In the checker mode of operation, all M-bus signals are placed in the high-impedance state and all M-bus outputs are monitored as inputs. The master operates normally. The checker compares its internal results with the results read as inputs. If a mismatch occurs, the checker asserts ERR.

Table 2. MC88200 Signal Summary (Continued)

Signal Name	Mnemonic	Function
Cache Static RAM Mode	SRAMMODE	SRAMMODE is an active-high input that places the MC88200 into diagnostic mode for checking the data cache. The data cache is accessed with P-bus signals A2–A11, DBE0–DBE3, and TR0–TR1 providing the address. The P-bus master can perform write-read comparisons to check the consistency of the cache lines and to mark faulty lines as invalid.
Reset	$\overline{\text{RST}}$	The $\overline{\text{RST}}$ input initiates an orderly restart of the MC88200, bringing it to a known state. When $\overline{\text{RST}}$ is asserted, the MC88200 halts the current transaction (if any) and functionally removes itself from the M-bus and P-bus. The CMMU ID register is initialized, and the M-bus and P-bus checker enable signals are sampled (MCE and PCE, respectively). Registers are placed in a predefined state and all MMU address translation is disabled.
Clock	CLK	The clock input signal generates the internal timing signals for the MC88200. The MC88200 internal clock is derived from the CLK signal, normally phase locked to minimize the skew between the external and internal signals. Since the CLK signal will be applied to the processor (MC88100) and to other peripherals, exact timing of internal signals is required to properly synchronize the devices to the buses.
Phase Lock Enable	PLLEN	Phase lock enable is an active-high input that controls the internal phase lock circuit that synchronizes the internal clocks to the CLK signal. To enable phase locking, PLLEN must be properly asserted during reset. If PLLEN is not asserted, phase locking does not occur.
Power Supply	V_{CC}	+5-volt power supply.
Ground	GND	Ground connections.



Function	Mnemonic	Type	Active	Count	Reset State
P-Bus					
Address	A31–A2	Input	High	30	Ignored
Supervisor/User	S/U	Input	High	1	Ignored
Chip Select	PCS	Input	Low	1	Ignored
Data Byte Enable	DBE3–DBE0	Input	High	4	Ignored
Data	D31–D0	I/O	High	32	High Imped
Read/Write	R/W	Input	High	1	Ignored
Lock	DLOCK	Input	Low	1	Ignored
Reply	R1–R0	Output	High	2	High Imped
M-Bus					
Request	BR	Output	High	1	Negated
Grant	BG	Input	High	1	Ignored
Acknowledge	BA	Output	High	1	Negated
Arbitration Busy	AB	Input	Low	1	Ignored
Busy	BB	Input	Low	1	Ignored
Address/Data	AD31–AD0	I/O	High	32	High Imped
Address/Data Parity	ADP3–ADP0	I/O	High	4	High Imped
Control	C6–C0	I/O	High	7	High Imped
Control Parity	CP	I/O	High	1	High Imped
Local Status	ST3–ST0	I/O	High	4	Active Input
System Status	SS3–SS0	Input	Low	4	Ignored
Reset	RST	Input	Low	1	Asserted
Clock	CLK	Input	High	1	Active
Phase Lock Enable	PLLEN	Input	Low	1	Active
Tag Monitor	TM1–TM0	I/O	High	2	Active Input
Trace	TR1–TR0	I/O	High	2	Active Input
Cache Static RAM Mode	SRAMMODE	Input	High	1	Active Input
P-Bus Checker Enable	PCE	Input	High	1	Active Input
M-Bus Checker Enable	MCE	Input	High	1	Active Input
Error	ERR	Output	High	1	Low
Power	VCC			18	
Ground	GND			18	

Figure 8. MC88200 Signal Functional Diagram

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to + 7.0	V
Input Voltage	V_{in}	−0.3 to + 7.0	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature Range	T_{stg}	−55 to + 150	°C

This device contains protective circuitry against damage due to high static voltages or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either GND or V_{CC}).

THERMAL CHARACTERISTICS—PGA PACKAGE

Characteristic	Symbol	Value	Rating
Thermal Resistance — Ceramic Junction to Ambient Junction to Case	 θ_{JA} θ_{JC}	 25 10*	°C/W

*Estimated

DC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V_{dc} ± 5%; GND = 0 V_{dc}; T_A = 0 to 70°C)

Characteristic	Symbol	Min	Max	Unit
Clock Low Voltage	V_{CL}	−0.3	0.2 V_{CC}	V
Clock High Voltage	V_{CH}	0.8 V_{CC}	V_{CC} + 0.3	V
Input Low Voltage (All Inputs Except CLK)	V_{IL}	−0.3	0.8	V
Input High Voltage (All Inputs Except CLK)	V_{IH}	2.0	V_{CC} + 0.3	V
Output Low Voltage @ 8 mA I_{OL}	V_{OL}	—	0.5	V
Output High Voltage @ −4 mA I_{OH}	V_{OH}	2.4	—	V
Input Leakage Current	I_{in}	—	10	µA
High-Impedance Leakage Current	I_{TSI}	—	20	µA
Typical Power Dissipation (T_A = 0°C) 16, 20, 25 MHz 33 MHz	P_D	—	1.5 1.8	W
Input Capacitance (V_{in} = 0 V, T_A = 25°C, f = 1 MHz)	C_i	—	15	pF
Output Capacitance (V_{in} = 0 V, T_A = 25°C, f = 1 MHz)	C_o	—	15	pF
Output Load Capacitance All P-bus Outputs All M-bus Outputs	C_L	—	70 130	pF
AC Output Delay Derating (See Note 1)	C_{LD}	—	1	ns/25 pF

NOTE: Only applies when exceeding the specified output load capacitance (C_L). Absolute output load capacitance, per output for correct device operation, must be less than or equal to 120 pF for P-bus and 180 pF for M-bus.

AC ELECTRICAL SPECIFICATIONS — CLOCK INPUT (see Figure 9)

Num	Characteristic	16.67 MHz		20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
	Frequency of Operation (See Note 1)	15.38	16.67	16.67	20	20.0	25	25	33.3	MHz
1	Clock Cycle Time (Measured at 0.5 V_{CC})	60	65	50	60	40	50	30	40	ns
2, 3	Clock Pulse Width (Measured at 0.5 V_{CC})	29	33.5	24	31	19	26	14	21	ns
4	Clock Rise Time (0.2 V_{CC} to 0.8 V_{CC})	—	5	—	5	—	4	—	3	ns
5	Clock Fall Time (0.8 V_{CC} to 0.2 V_{CC})	—	5	—	5	—	4	—	3	ns

NOTE: The PLLEN and RST signals must be asserted as specified (phase-locked operation). Otherwise, correct device operation cannot be guaranteed.

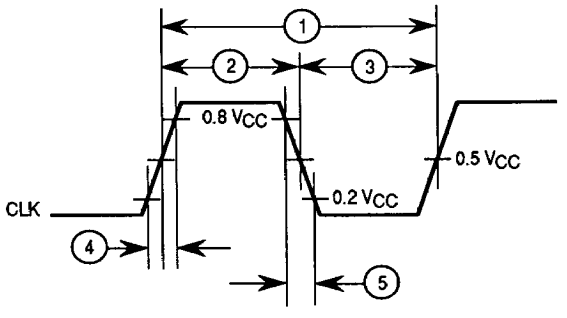


Figure 9. Clock Input Timing Diagram

P-BUS AC SPECIFICATIONS (see Figure 10)

Num	Characteristic	16.67 MHz		20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
7	Address (Axx), S/$\overline{U}$, R/$\overline{W}$, $\overline{DLOCK}$ to CLK Rising (Input Setup)	4	—	3	—	2	—	2	—	ns
8	CLK Falling to Address (Axx), S/$\overline{U}$, R/$\overline{W}$, $\overline{DLOCK}$ Invalid (Input Hold)	2	—	3	—	2	—	1	—	ns
9	Data Byte Enable (DBEx) Valid to CLK Falling (Input Setup)	18	—	15	—	12	—	10	—	ns
10	CLK Falling to Data Byte Enable (DBEx) Invalid (Input Hold)	2	—	3	—	2	—	1	—	ns
11	Chip Select ($\overline{PCS}$) Valid to CLK Falling (Input Setup)	18	—	15	—	12	—	10	—	ns
12	CLK Falling to Chip Select ($\overline{PCS}$) Invalid (Input Hold)	2	—	3	—	2	—	1	—	ns
13	Write Data In (Dxx) Valid (Write to CMMU) to CLK Falling (Input Setup)	4	—	3	—	2	—	2	—	ns
14	CLK Rising to Write Data In (Dxx) Invalid (Write to CMMU) (Input Hold)	2	—	3	—	2	—	1	—	ns
15	CLK Falling to Read Data Out (Dxx) Low-Impedance (Read from CMMU)	10	—	10	—	8	—	6	—	ns
16	CLK Falling to Read Data Out (Dxx) Valid (Read from CMMU)	10	23	10	20	8	16	6	12	ns
17	CLK Rising to Read Data Out (Dxx) Invalid (Output Hold) (Read from CMMU)	4	—	5	—	4	—	3	—	ns
18	CLK Rising to Read Data Out (Dxx) High-Impedance (Read from CMMU)	—	8	—	8	—	6	—	5	ns
19	CLK Falling to Reply (Rx) Low-Impedance	10	—	10	—	8	—	6	—	ns
20	CLK Falling to Reply (Rx) Valid	10	28	10	23	8	18	6	14	ns
21	CLK Falling to Reply (Rx) Invalid (Output Hold)	4	—	5	—	4	—	3	—	ns
22	CLK Falling to Reply (Rx) High-Impedance	—	8	—	8	—	6	—	5	ns
66	CLK Rising To TM1–TM0, TR1–TR0 Valid	—	25	—	20	—	15	—	12	ns
67	CLK Falling to TM1–TM0, TR1–TR0 Invalid (Output Hold)	4	—	5	—	3	—	3	—	ns

NOTE: Termination analysis is required to ensure that V_{IL} and V_{IH} specifications are maintained throughout input setup times.

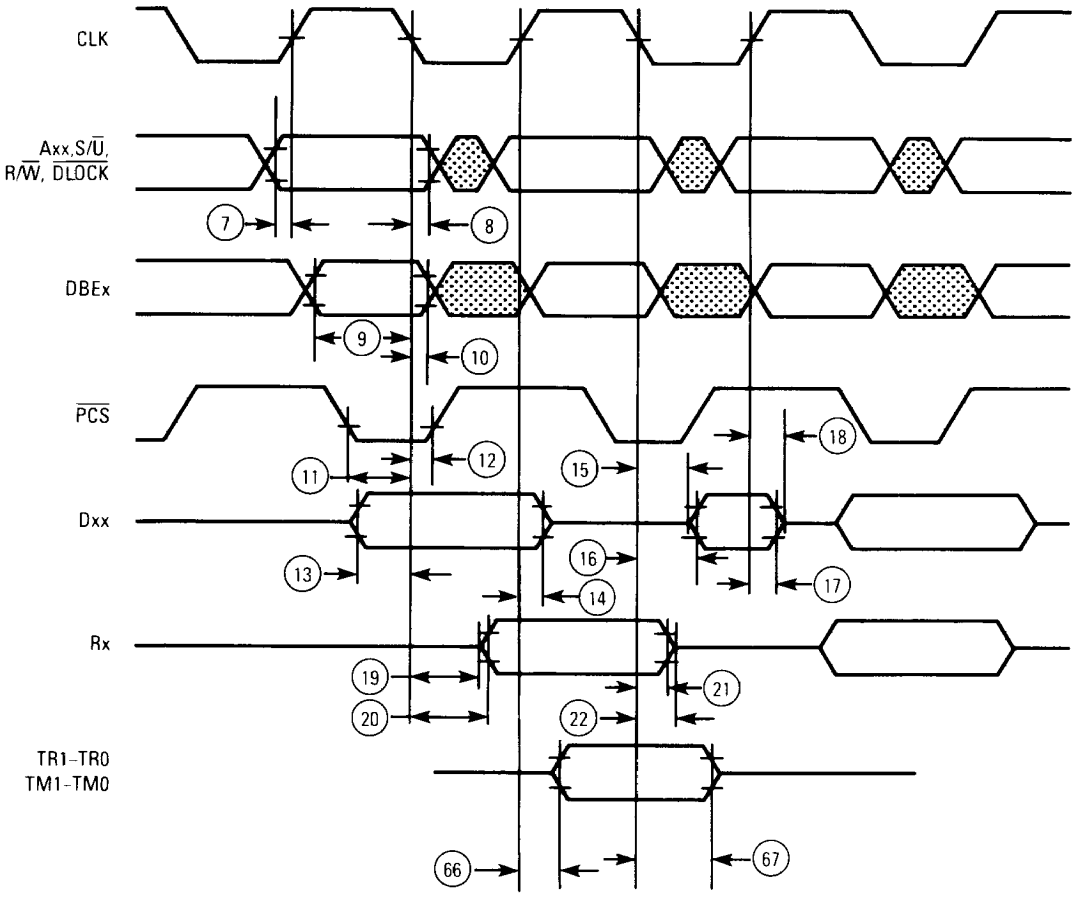


Figure 10. P-bus Timing Diagram

M-BUS AC SPECIFICATIONS: M-BUS ARBITRATION (see Figure 11)

Num	Characteristic	16.67 MHz		20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
23	CLK Rising to BR Valid	—	23	—	20	—	15	—	12	ns
24	CLK Rising to BR Invalid (Output Hold)	4	—	5	—	4	—	3	—	ns
25	BG Valid to Clock Rising (Input Setup)	12	—	10	—	8	—	6	—	ns
26	Clock Rising to BG Invalid (Input Hold)	3	—	3	—	2	—	1	—	ns
27	Clock Rising to BA Valid	—	25	—	20	—	15	—	12	ns
28	Clock Rising to BA Invalid (Output Hold)	4	—	5	—	4	—	3	—	ns
29	$\overline{AB}$ Valid to Clock Rising (Input Setup)	12	—	10	—	8	—	6	—	ns
30	Clock Rising to $\overline{AB}$ Invalid (Input Hold)	3	—	3	—	2	—	1	—	ns
31	$\overline{BB}$ Valid to Clock Rising (Input Setup)	12	—	10	—	8	—	6	—	ns
32	Clock Rising to $\overline{BB}$ Invalid (Input Hold)	3	—	3	—	2	—	1	—	ns
33	BA Valid to $\overline{BB}$ Valid	0	23	0	20	0	15	0	12	ns

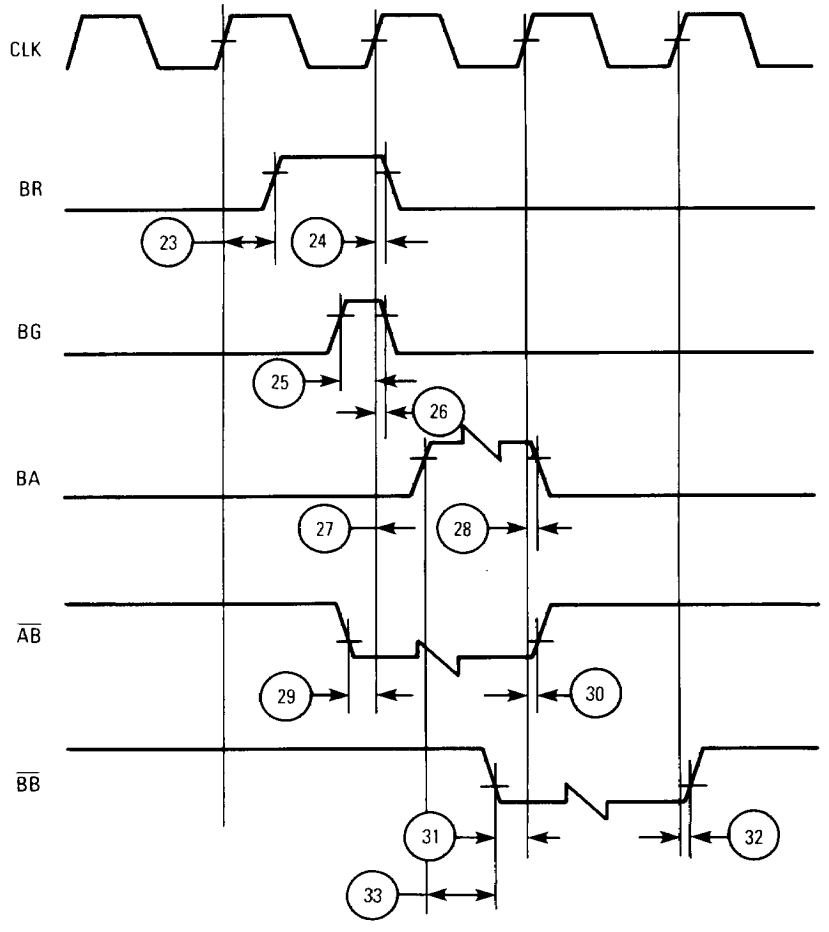


Figure 11. M-bus Arbitration Timing Diagram

M-BUS AC SPECIFICATIONS: M-BUS MASTER (see Figure 12)

Num	Characteristic	16.67 MHz		20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
34	CLK Rising to AD Bus (ADxx, ADPx) Low-Impedance (Address Phase)	10	—	10	—	8	—	6	—	ns
35	CLK Rising to AD Bus (ADxx, ADPx) Valid (Address Phase)	—	25	—	20	—	15	—	12	ns
36	CLK Rising to AD Bus (ADxx, ADPx) Invalid (Output Hold) (Address Phase)	4.5	—	5	—	4	—	3	—	ns
37	CLK Rising to AD Bus (ADxx, ADPx) High-Impedance (Address Phase)	—	8	—	8	—	6	—	5	ns
38	AD Bus (ADxx, ADPx) Valid to CLK Rising (Input Setup) (Data Phase—Read)	12	—	10	—	8	—	6	—	ns
39	CLK Rising to AD Bus (ADxx, ADPx) Invalid (Input Hold) (Data Phase—Read)	2.5	—	3	—	2	—	1	—	ns
40	CLK Rising to AD Bus (ADxx, ADPx) Low-Impedance (Data Phase—Write)	10	—	10	—	8	—	6	—	ns
41	CLK Rising to AD Bus (ADxx, ADPx) Valid (Data Phase—Write)	—	25	—	20	—	15	—	12	ns
42	CLK Rising to AD Bus (ADxx, ADPx) Invalid (Output Hold) (Data Phase—Write)	4.5	—	5	—	4	—	3	—	ns
43	CLK Rising to AD Bus (ADxx, ADPx) High-Impedance (Data Phase—Write)	—	8	—	8	—	6	—	5	ns
44	CLK Rising to Control (Cx, CP) Low-Impedance	8	—	8	—	8	—	6	—	ns
45	CLK Rising to Control (Cx, CP) Valid	—	25	—	20	—	15	—	12	ns
46	CLK Rising to Control (Cx, CP) Invalid (Output Hold)	4.5	—	5	—	4	—	3	—	ns
47	CLK Rising to Control (Cx, CP) High-Impedance	—	8	—	8	—	6	—	5	ns
48	System Status Valid ($\overline{SSx}$) to CLK Rising (Input Setup)	12	—	10	—	8	—	6	—	ns
49	CLK Rising to System Status ($\overline{SSx}$) Invalid (Input Hold)	3	—	3	—	2	—	1	—	ns
66	CLK Rising to TM1–TM0, TR1–TR0 Valid	—	25	—	20	—	15	—	12	ns
67	CLK Falling to TM1–TM0, TR1–TR0 Invalid (Output Hold)	4	—	5	—	3	—	3	—	ns

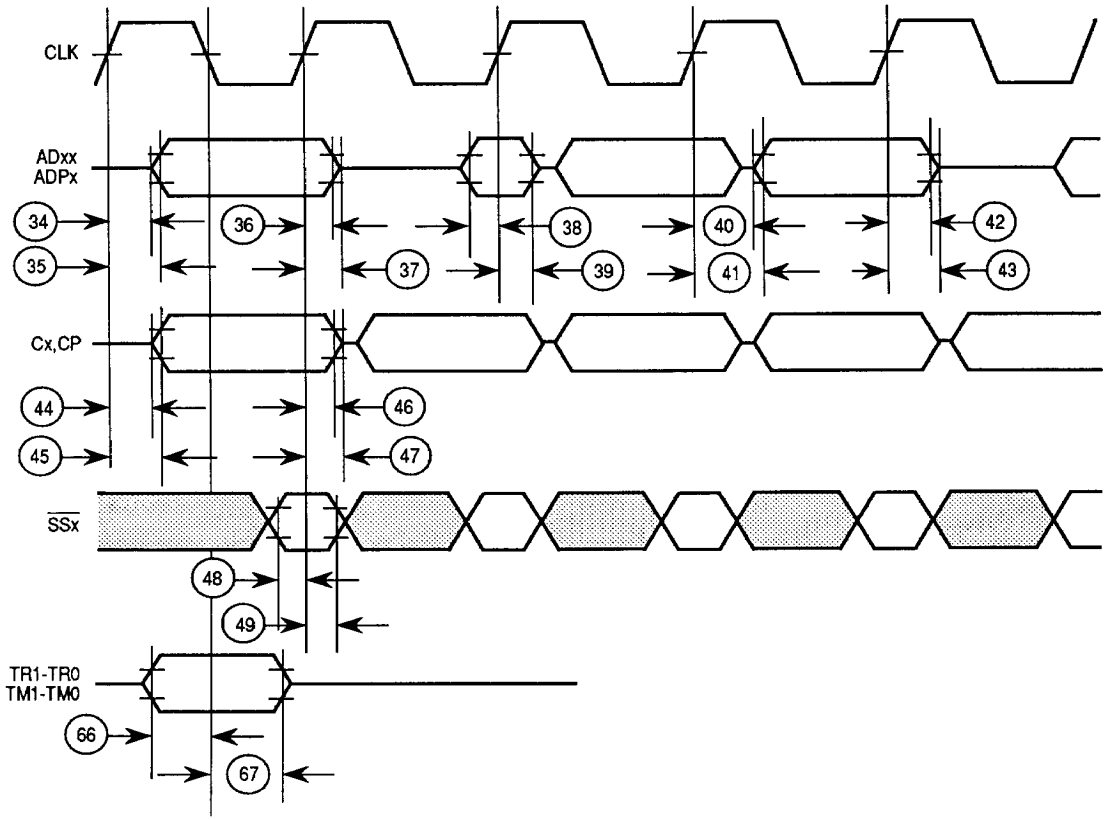


Figure 12. M-bus Master Timing Diagram

M-BUS AC SPECIFICATIONS: M-BUS SLAVE (see Figure 13)

Num	Characteristic	16.67 MHz		20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
50	AD Bus (ADxx, ADPx) Valid to CLK Rising (Input Setup) (Address Phase)	12	—	10	—	8	—	6	—	ns
51	CLK Rising to AD Bus (ADxx, ADPx) Invalid (Input Hold) (Address Phase)	2.5	—	3	—	2	—	1	—	ns
52	CLK Rising to AD Bus (ADxx, ADPx) Low-Impedance (Data Phase—Read from CMMU)	10	—	10	—	8	—	6	—	ns
53	CLK Rising to AD Bus (ADxx, ADPx) Valid (Data Phase—Read from CMMU)	—	25	—	20	—	15	—	12	ns
54	CLK Rising to AD Bus (ADxx, ADPx) Invalid (Output Hold) (Data Phase—Read from CMMU)	4.5	—	5	—	4	—	3	—	ns
55	CLK Rising to AD Bus (ADxx, ADPx) High-Impedance (Data Phase—Read from CMMU)	—	8	—	8	—	6	—	5	ns
56	AD Bus (ADxx, ADPx) Valid to CLK Rising (Input Setup) (Data Phase—Write to CMMU)	12	—	10	—	8	—	6	—	ns
57	CLK Rising to AD Bus (ADxx, ADPx) Invalid (Input Hold) (Data Phase—Write to CMMU)	2.5	—	3	—	2	—	1	—	ns
58	Control (Cxx, CPx) Valid to CLK Rising (Input Setup)	12	—	10	—	8	—	6	—	ns
59	CLK Rising to Control (Cxx, CPx) Invalid (Input Hold)	2.5	—	3	—	2	—	1	—	ns
61	CLK Rising to Local Status (STx) Valid	—	25	—	20	—	15	—	12	ns
62	CLK Rising to Local Status (STx) Invalid (Output Hold)	4	—	5	—	4	—	3	—	ns
64	System Status ($\overline{SSx}$) Valid to CLK Rising (Input Setup)	12	—	10	—	8	—	6	—	ns
65	CLK Rising to System Status ($\overline{SSx}$) Invalid (Input Hold)	3	—	3	—	2	—	1	—	ns

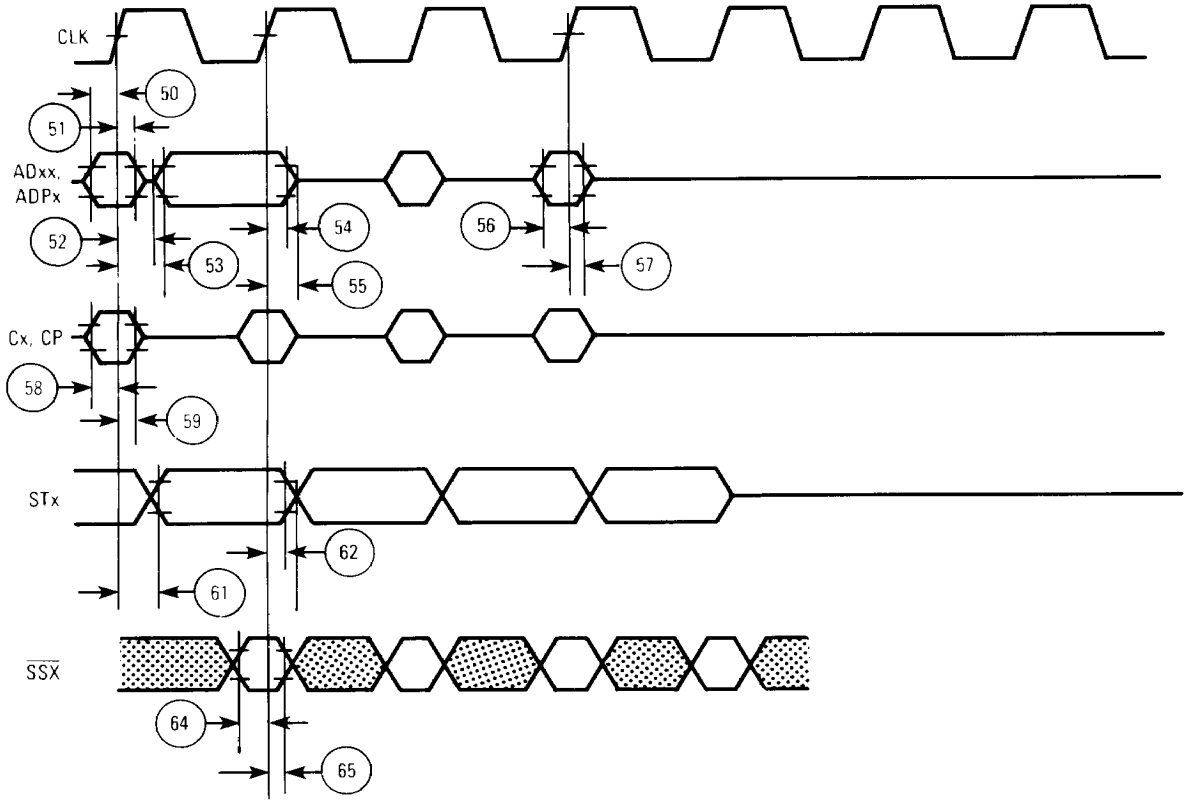


Figure 13. M-bus Slave Timing Diagram

MISCELLANEOUS SIGNAL AC SPECIFICATIONS (see Figures 14 and 15)

Num	Characteristic	16.67 MHz		20 MHz		25 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
68	$\overline{RST}$, PLLEN, Input Transition Time	—	10	—	10	—	10	—	6	ns
69	$\overline{RST}$, PCE, MCE, SRAMMODE Valid to Clock Falling (Input Setup) (see Note)	10	30	10	25	8	20	5	15	ns
70	TR1–TR0, TM0, ST3–ST0 Valid to CLK Falling (Input Setup)	12	—	10	—	8	—	6	—	ns
71	CLK Falling to TR1–TR0, TM0, ST3–ST0 (Input Hold) Invalid	12	—	10	—	8	—	6	—	ns
72	CLK Rising to TR1–TR0, TM0, ST3–ST0 Low Impedance	10	—	—	10	—	8	—	6	ns
73	TR1–TR0 Valid to CLK Falling (Input Setup—SRAMMODE)	12	—	10	—	8	—	6	—	ns
74	CLK Falling to TR1–TR0 Invalid (Input Hold—SRAMMODE)	12	—	10	—	8	—	6	—	ns
75	CLK Falling to ERR Valid	0	12	0	10	0	8	0	6	ns
76	CLK Rising to ERR Negated	4	18	5	15	4	12	3	11	ns

NOTE: This spec must be met for the same clock edge for all M88000 devices operating synchronously. PCE, MCE, and SRAMMODE may only transition during reset.

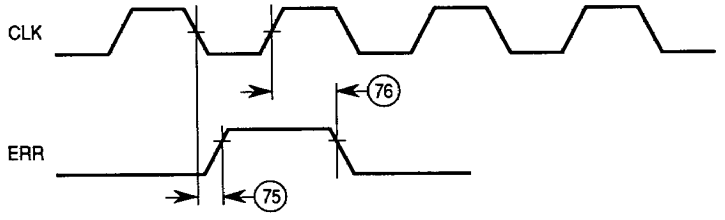
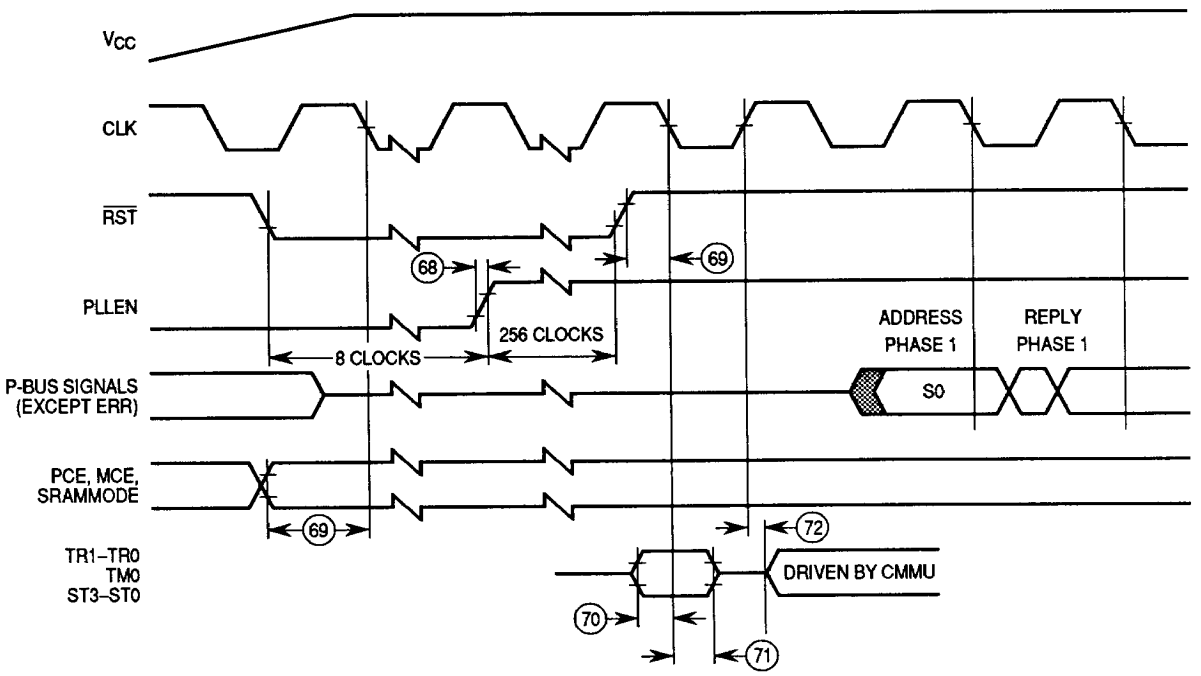
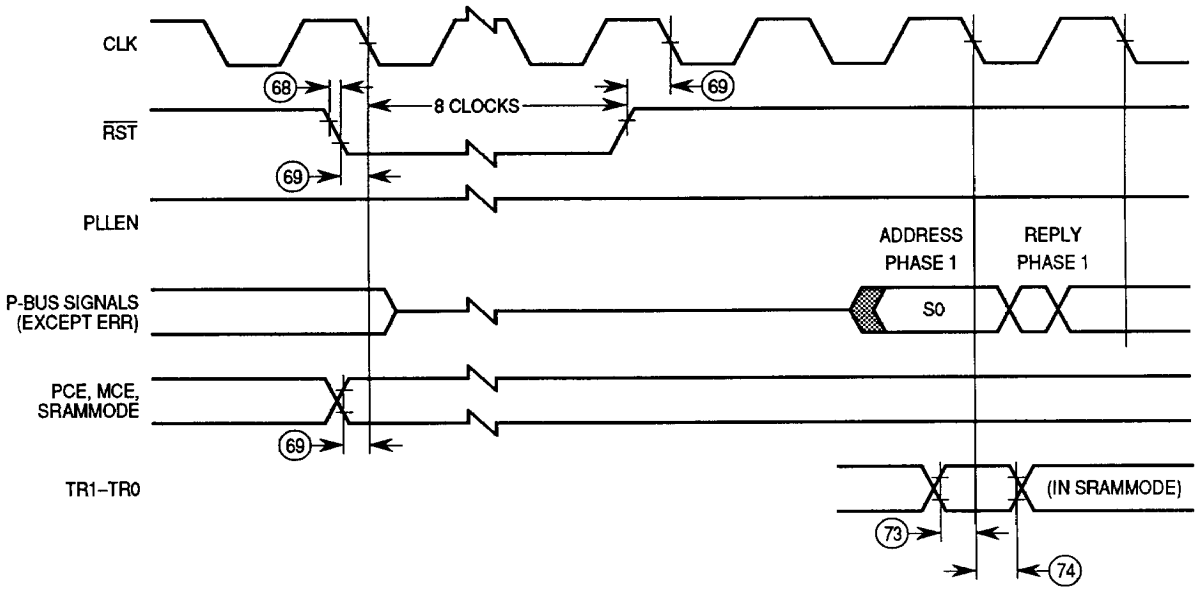


Figure 14. Error Signal Timing Diagram



(a) Power-Up Reset



(b) Warm Reset

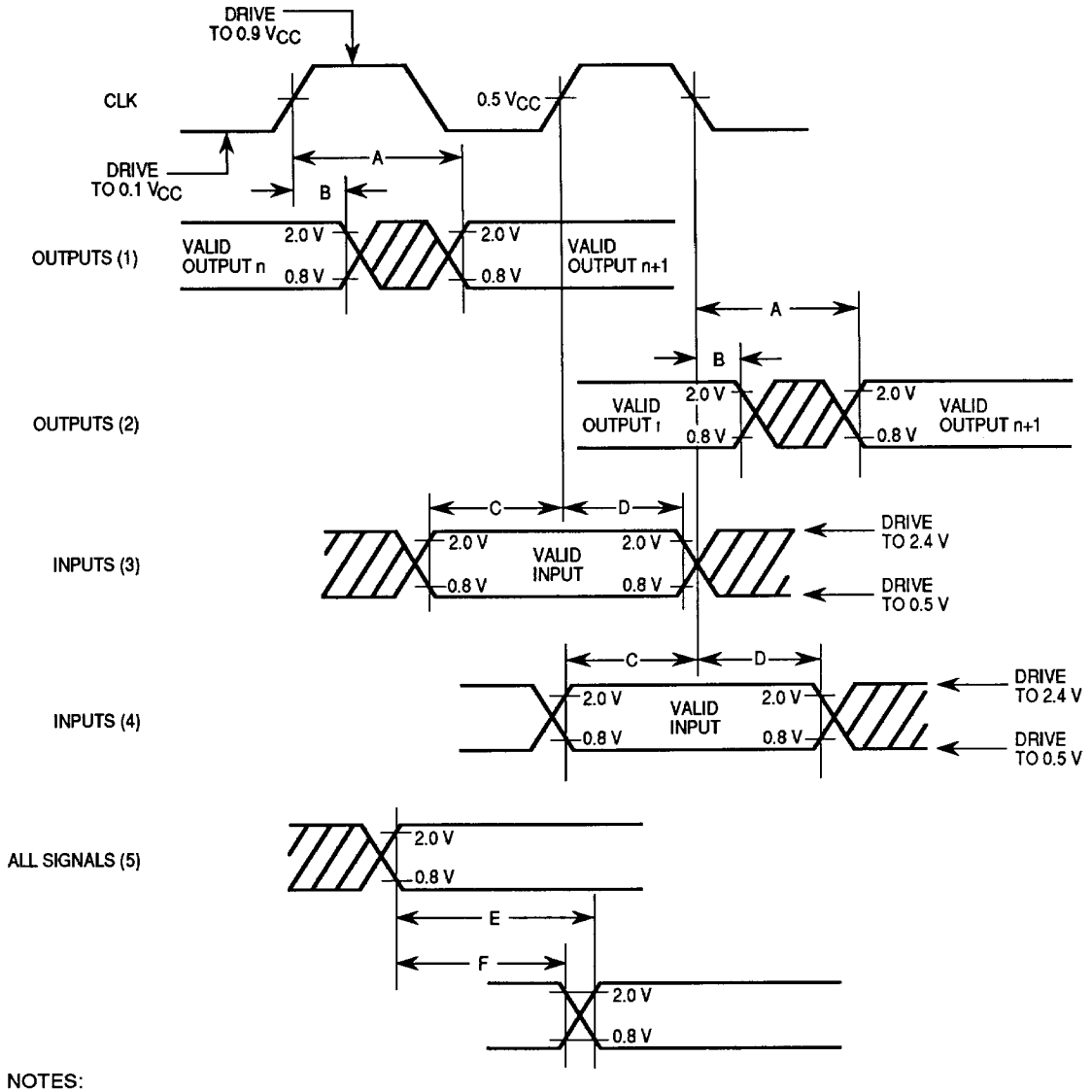
Figure 15. Miscellaneous Signal Timing Diagram

AC ELECTRICAL SPECIFICATIONS DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the M88000 clock input and, possibly, relative to one or more other signals.

The measurement of the AC specifications is defined by the waveforms in Figure 16. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in Figure 16. Outputs of the M88000 are specified with minimum and/or maximum limits, as appropriate, and are measured as shown. Inputs to the M88000 are specified with minimum and, as appropriate, maximum setup and hold times and are measured as shown. Finally, the measurements for signal-to-signal specifications are also shown.

Note that the testing levels used to verify conformance of the M88000 to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical characteristics.



NOTES:

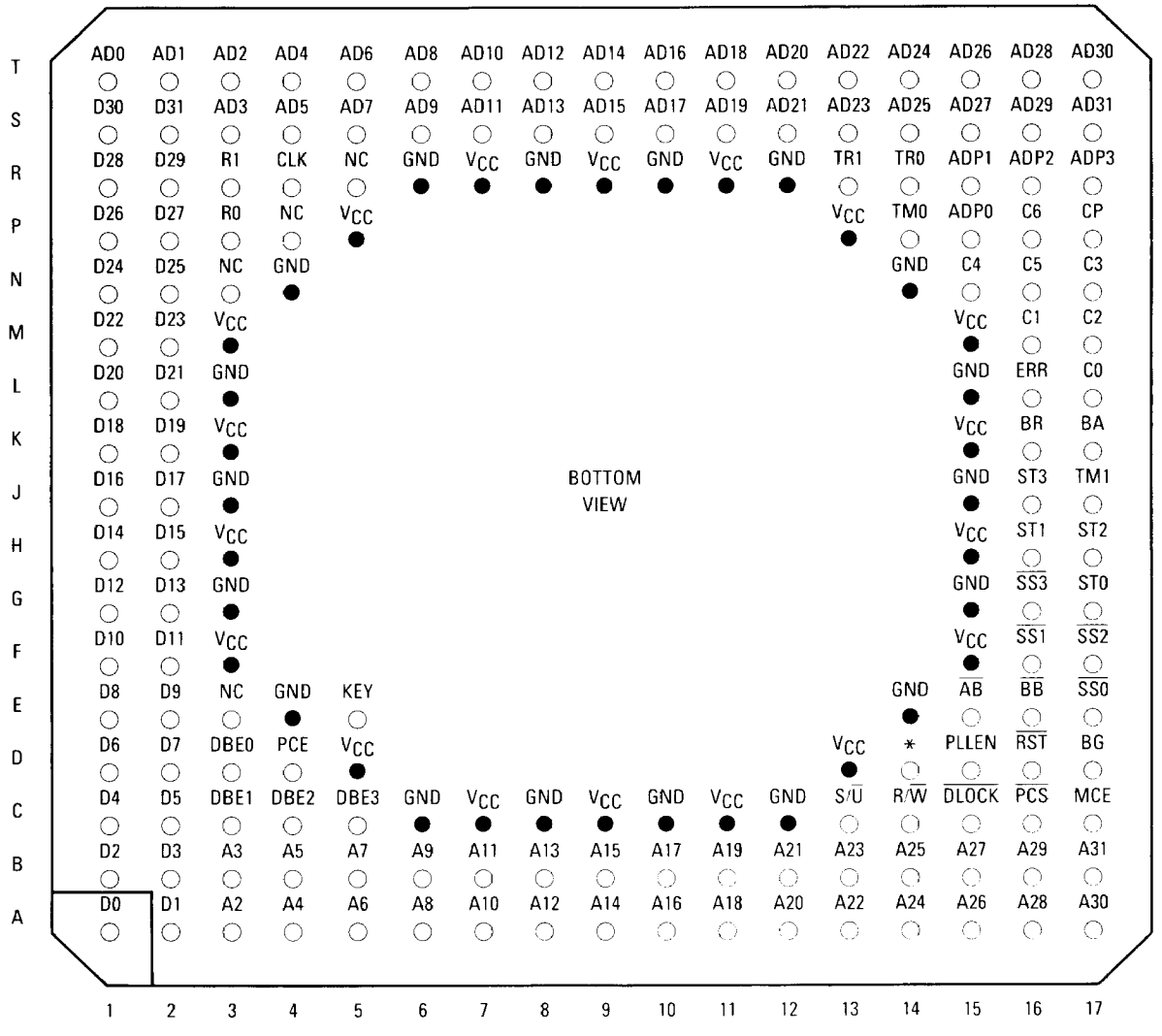
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:

A. Maximum output delay specification.
B. Minimum output hold time.
C. Minimum input setup time specification.
D. Minimum input hold time specification.
E. Signal valid to signal valid specification (maximum or minimum).
F. Signal valid to signal invalid specification (maximum or minimum).

Figure 16. Drive Levels and Test Points for AC Specifications

PIN ASSIGNMENTS



* = SRAMMODE

NC — Do Not Connect

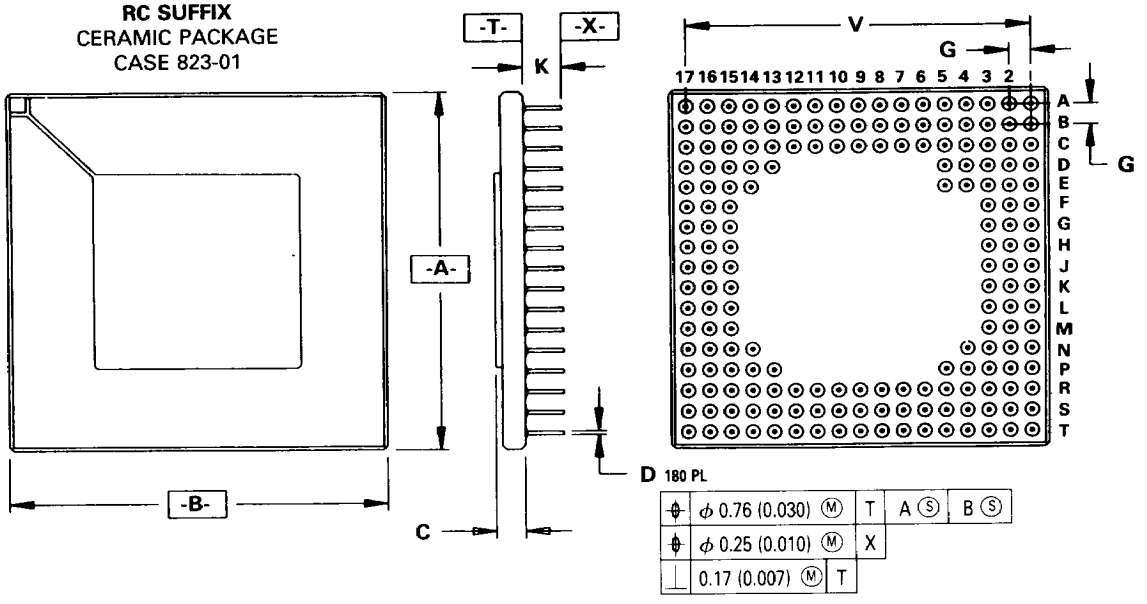
Note: The "KEY" pin is an alignment key with no internal connection.

The V_{CC} and GND pins are separated into two groups to provide individual connections for output buffers and internal logic.

Pin Group	V_{CC}	GND
Internal Logic	C7, C9, C11, D5 D13, P5, P13	C6, C8, C10, C12 N4, N14
External Signals and Buses	F3, F15, H3, H15 K3, K15, M3, M15 R7, R9, R11	E4, E14, G3, G15 J3, J15, L3, L15 R6, R8, R10, R12

PACKAGE DIMENSIONS

RC SUFFIX
CERAMIC PACKAGE
CASE 823-01



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	44.20	45.21	1.740	1.780
B	44.20	45.21	1.740	1.780
C	3.05	3.86	0.120	0.152
D	0.41	0.50	0.016	0.020
G	2.54 BSC		0.100 BSC	
K	4.07	5.08	0.160	0.200
V	40.64 BSC		1.600 BSC	