XILINX

XC7272
Programmable Logic Device

Preliminary Product Description, April 1992

FEATURES

- Second-Generation High Density Programmable Logic Device
- UV-erasable CMOS EPROM technology
- 72 Macrocells, grouped into eight Function Blocks, interconnected by a programmable Universal Interconnect Matrix
- Each Function Block contains a programmable AND-array with 21 complementary inputs, providing up to 16 product terms per Macrocell
- Enhanced logic features:
  - 2-input Arithmetic Logic Unit in each Macrocell
  - Dedicated fast carry network between Macrocells
  - Wide AND capability in the Universal Interconnect Matrix
- Identical timing for all interconnect paths and for all Macrocell logic paths
- 72 signal pins in the 84-pin packages: 42 I/O, 12 inputs, 18 outputs
- Each input is programmable: Direct, latched, or registered
- I/O-pin is usable as input when Macrocell is buried
- Two high-speed, low-skew global clock inputs
- 68-pin and 84-pin leaded chip carrier packages and 84-pin Pin-Grid-Array packages

GENERAL DESCRIPTION

The XC7272 is a second-generation High Density Programmable Logic Device that combines the classical features of the PAL-like EPLD architecture with innovative systems-oriented logic enhancements. This favors the implementation of fast state machines, large synchronous counters and fast arithmetic, as well as multi-level general-purpose logic. Performance, measured in achievable system clock rate and critical delays, is not only predictable, but independent of physical logic mapping, interconnect routing, and resource utilization. Performance, therefore, remains invariant between design iterations. The propagation delay through interconnect and logic is constant for any function implemented in any one of the output Macrocells.

The functional versatility of the traditional programmable logic array architecture is enhanced through additional gating and control functions available in an Arithmetic Logic Unit (ALU) in each Macrocell. Dedicated fast arithmetic carry lines running directly between adjacent Macrocells and Function Blocks support fast adders, subtractors and comparators of any length up to 72 bits.

This additional ALU in each Macrocell can generate any combinatorial function of two sums of products, and it can generate and propagate arithmetic-carry signals between adjacent Macrocells and Functional Blocks.

The Universal Interconnect Matrix (UIM) facilitates unrestricted, fixed-delay interconnects from all device inputs and Macrocell outputs to any Function Block AND-array input. The UIM can also perform a logical AND across any number of its incoming signals on the way to any Functional Block, adding another level of logic without additional delay. This supports bidirectional loadable synchronous counters of any size up to 72 bits, operating at the specified maximum device frequency

As a result of these logic enhancements, the XC7272 can deliver high performance even in designs that combine large numbers of product terms per output, or need more layers of logic than AND-OR, or need a wide AND function in some of the product terms, or perform wide arithmetic functions.

Automated design mapping is supported by Xilinx development software based on design capture using third-party schematic entry tools, PLD compilers or direct text-based equation files. Design mapping is completed in a few minutes on a PC.

ARCHITECTURAL OVERVIEW

Figure 1 shows the XC7272 structure. Eight Function Blocks (FBs) are all interconnected by a central Universal Interconnect Matrix (UIM). Each FB receives 21 signals from the UIM and each FB produces nine signals back into the UIM. All device inputs are also routed via the UIM to all Function Blocks Each FB contains nine output Macrocells (MCs) that draw from a programmable AND array driven by the 21 signals from the UIM. Most Macrocells drive a 3-state chip output, all feed back into the UIM.

The device also contains two dedicated Fast Comparators (FCs) for address compare or decode functions. The following pages describe the elements of this architecture in detail.

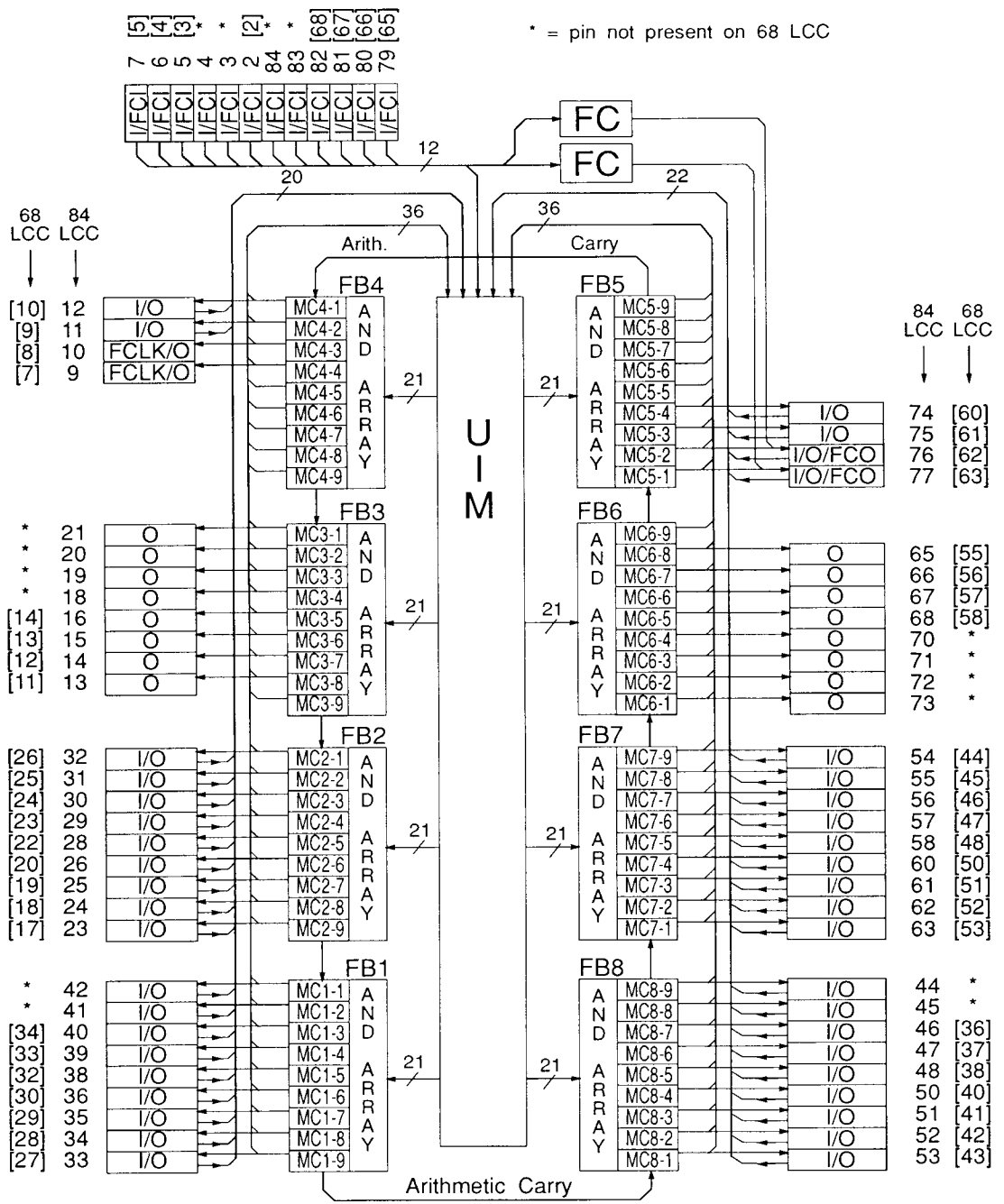


Figure 1. XC7272 Architecture

Function Blocks and Macrocells

The XC7272 contains 72 Macrocells with identical structure, grouped into eight Function Blocks of nine Macrocells each. Each Macrocell is driven by product terms derived from the 21 inputs from the UIM into the Function Block.

Five product terms are private to each Macrocell; an additional 12 product terms are shared among the nine Macrocells in any Function Block. One of the private product terms is a dedicated clock for the flip-flop in the Macrocell. See the description on page 4 for other clocking options.

The remaining four private product terms can be selectively ORed together with up to three of the shared product terms, and drive one input to an Arithmetic Logic Unit. The other input to the ALU is driven by the OR of up-to-nine product terms from the remaining shared product terms.

As a programmable option, two of the private product terms can be used for other purposes. One is the asynchronous active-High Reset of the Macrocell flip-flop, the other can be either an asynchronous active-High Set of the Macrocell flip-flop, or an Output-Enable signal.

The Arithmetic Logic Unit has two programmable modes: In the *logic mode,* it is a 2-input function generator, a 4-bit look-up table, that can be programmed to generate any Boolean function of its two inputs. It can OR them, widening the OR function to max 16 inputs; it can AND them, which means that one sum of products can be used to mask the other; it can XOR them, toggling the flip-flop or comparing the two sums of products. Either or both of the sum-of-product inputs to the ALU can be inverted, and either or both can be ignored. The ALU can implement one additional layer of logic without any speed penalty.

In the *arithmetic mode,* the ALU block can be programmed to generate the arithmetic sum or difference of two operands, combined with a carry signal coming from the lower Macrocell; it also feeds a carry output to the next higher Macrocell. This carry propagation chain crosses the boundaries between Function Blocks, but it can also be configured 0 or 1 when it enters a Function Block.

This dedicated carry chain overcomes the inherent speed and density problems of the traditional EPLD architecture, when trying to perform arithmetic functions like add, subtract, and magnitude compare.

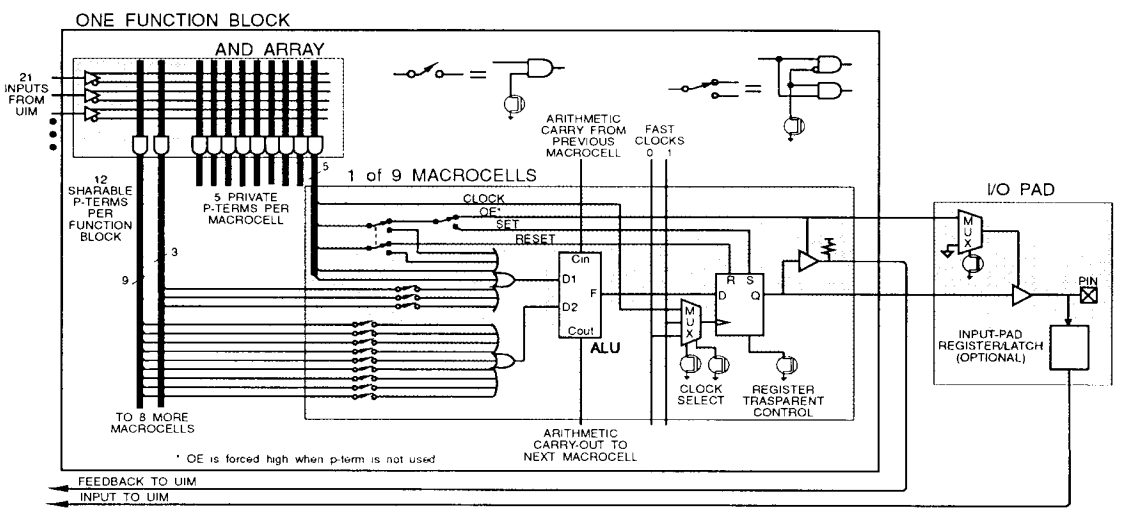


Figure 2. Function Block and Macrocell Schematic Diagram

The ALU output drives the D input of the Macrocell flip-flop.

Each flip-flop has several programmable options:

One option is to eliminate the flip-flop by making it transparent, which makes the Q output identical with the D input, independent of the clock.

If this option is *not* programmed, the flip-flop operates in the conventional manner, triggered by the rising edge on its clock input.

The clock source is programmable: It is either the dedicated product term mentioned above, or it is one of the two global FastCLK signals that are distributed with short delay and minimal skew over the whole chip.

The asynchronous Set and Reset (Clear) inputs override the clocked operation. If both asynchronous inputs are active simultaneously, Reset overrides Set. Upon power-up, each Macrocell flip-flop can be preloaded with either 0 or 1.

In addition to driving the chip output buffer, the Macrocell output is also routed back as an input to the UIM. When the Output Enable product term mentioned above is not active, this feedback line is forced High and thus disabled.

Outputs

Sixty of the 72 Macrocells drive chip outputs directly through 3-state output buffers, each individually controlled by the Output Enable product term mentioned above. For bidirectional I/O pins, an additional programmable cell can optionally disable the output permanently. The buried flip-flop is then still available for internal feedback, and the pin can still be used as a separate input

Inputs

Each signal input to the chip is programmable as either direct, latched, or registered in a flip-flop. Latch and flip-flop can be programmed with either of the two FastCLK signals as latch enable or clock. The latch is transparent when FastCLK is High, and the flip-flop clocks on the rising edge of FastCLK. Registered inputs allow high system clock rates by pipelining the inputs before they incur the combinatorial delay in the device, in cases where a pipeline cycle is acceptable.

The direct, latched, or registered inputs then drive the UIM. There is no propagation-delay difference between pure inputs and I/O inputs.

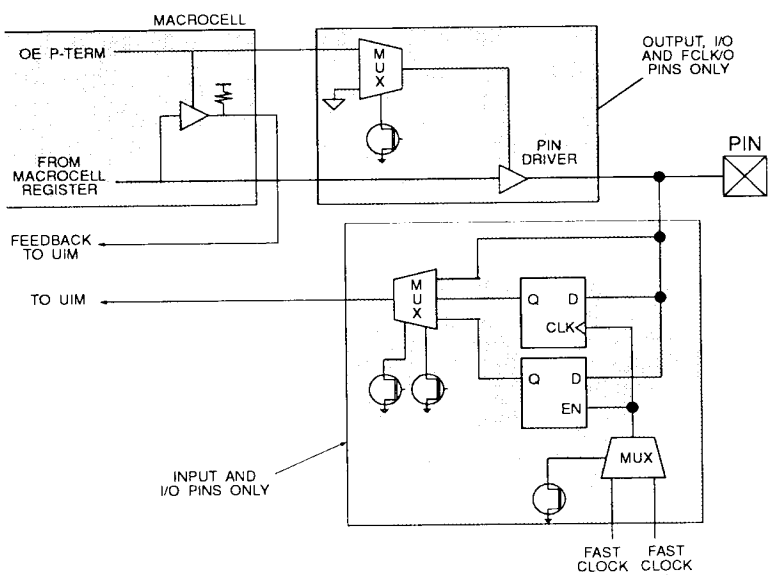


Figure 3. Input/Output Schematic Diagram

Universal Interconnect Matrix

The UIM receives 126 inputs: 72 from the 72 Macrocells, 42 from bidirectional I/O pins, and 12 from dedicated input pins. Acting as an unrestricted crossbar switch, the UIM generates 168 output signals, 21 to each Function Block.

Any one of the 126 inputs can be programmed to be connected to any number of the 168 outputs. The delay through the array is constant, independent of the apparent routing distance, the fan-out, fan-in, or routing complexity. Routability is not an issue: Any UIM input can drive any UIM output, even multiple outputs, and the delay is constant.

When multiple inputs are programmed to be connected to the same output, this output becomes the AND of the input signals if the levels are interpreted as active High. By choosing the appropriate signal inversion in the Macrocell outputs and the Function Block AND-array input, this AND-logic can also be used to implement a NAND, OR, or NOR function, thus offering an additional level of logic without any speed penalty.

A Macrocell feedback signal that is disabled by the output enable product term represents a High input to the UIM. Several such Macrocell outputs programmed onto the same UIM output thus emulate a 3-state bus line. If *one* of the Macrocell outputs is enabled, the UIM output assumes that same level.

FastCompare

Two 12-bit wide fast identity (equality) comparators are driven by the 12 dedicated FCI inputs, which also drive into the UIM. These dedicated circuits compare the input data against two sets of 12-bit data, either loaded previously from the same data inputs, or pre-programmed into the device.

As a programming option, any bit can be excluded from the comparison (disabled), the whole comparison can be disabled (forced false), and the polarity of the response can be chosen. The FCO comparator outputs can substitute the MC 5-1 and 5-2 outputs. Since this compare circuitry bypasses the UIM and the AND/OR logic, it is very fast and can also be used as a high-speed address decoder.

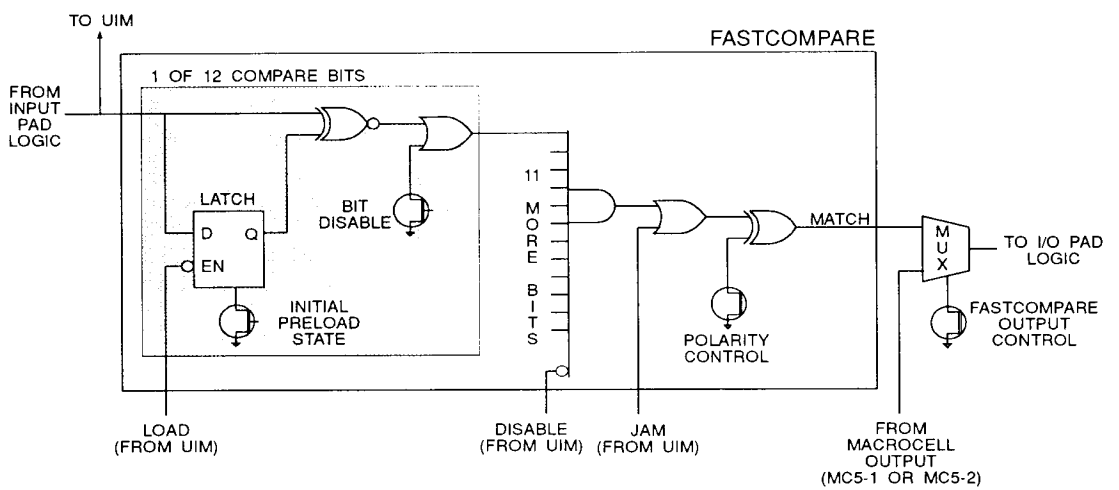


Figure 4. FastCompare Schematic Diagram

PROGRAMMING THE XC7272

The features and capabilities described above are used by the Xilinx development software to program the device according to the specification given either through schematic entry, or through a behavioral description expressed in Boolean equations.

The user can specify a security bit that prevents any reading of the programming bit map after the device has been programmed and verified

The device is programmed in a manner similar to an EPROM (ultra-violet light erasable read-only memory) using the Intel Hex format. Programming support is available from a number of programmer manufacturers. The UIM connections and the AND/OR plane connections are made directly by the EPROM cells.

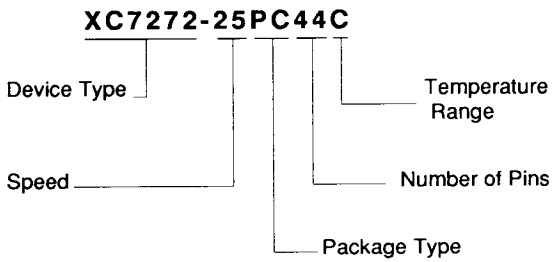
Other control bits are read out of the EPROM array within 1 ms after power-up and are stored in latches. This method, common in EPLD devices, requires either a very fast Vcc rise time (< 5 µs), or a power-on-reset delay lasting until Vcc has risen to 4.5 V, or a >100 ns $\overline{\text{Reset}}$ pulse after Vcc has risen to 4.5 V. The most popular circuit is a capacitor and a pull-up resistor on MR. The RC product must be larger than twice the Vcc rise time.

Unused input and I/O pins should be tied to ground or Vcc or some valid logic level. This is common practice for all CMOS devices to avoid dissipating excess current through the input-pad circuitry.

The recommended decoupling on the three Vcc pins should total 1 µF using high-speed (tantalum or ceramic) capacitors.

ORDERING INFORMATION

Example:



Speed Options

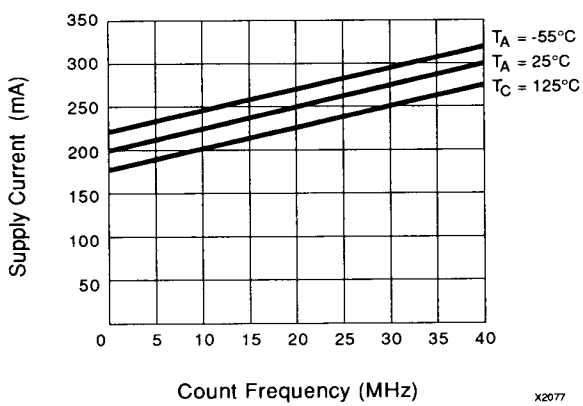
-30	30 ns (33 MHz) sequential cycle time
-25	25 ns (40 MHz) sequential cycle time

Package Options

PC68	68-Pin Plastic Leaded Chip Carrier
WC68	68-Pin Windowed Ceramic Leaded Chip Carrier
PC84	84-Pin Plastic Leaded Chip Carrier
WC84	84-Pin Windowed Ceramic Leaded Chip Carrier
PG84	84-Pin Ceramic Windowed Pin Grid Array

Temperature Options

C	Commercial	0°C to 70°C
I	Industrial	-40°C to 85°C



Typical Power Requirements for XC7272 Configured as Sixteen 4-bit Counters

(V_{CC} = +5.0V, V_{IN} = V_{CC} or GND, all outputs open)

ABSOLUTE MAXIMUM RATINGS

			Units
V_{CC}	Supply voltage relative to GND	–0.5 to 7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to 7.0	V
V_{TS}	Voltage applied to 3-state output	–0.5 to 7.0	V
V_{PP}	Programming voltage	+14	V
T_{STG}	Storage temperature	–65 to + 150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+ 260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

OPERATING CONDITIONS

				Min	Max	Units
V_{CC}	Supply voltage relative to GND	Commercial	0°C to 70°C	4.75	5.25	V
	Supply voltage relative to GND	Industrial	–40°C to 85°C	4.5	5.5	V
V_{IH}	High-level input voltage			2.0	V_{CC}+ 0.3	V
V_{IL}	Low-level input voltage			0	0.8	V

DC CHARACTERISTICS OVER OPERATING CONDITIONS

		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4 mA , V_{CC} min	2.4		V
V_{OL}	Low-level output voltage @ I_{OL} = 8 mA , V_{CC} min		0.5	V
I_{CC}	Supply current while idle			mA
I_{IL}	Leakage current	–10	+10	µA
I_{OZ}	Output High-Z Leakage current	–100	+100	µA
C_{IN}	Input capacitance (sample tested)		10	pF

XC7272 AC Timing Requirements

		Speed Grade	-30		-25				Units
Description	Fig.	Symbol	Min	Max	Min	Max	Min	Max	
Sequential toggle frequency (with feedback) using FastCLK	5	f_{CYC} (Note 1)	0	33	0	40			MHz
Sequential toggle frequency (with feedback) using a Product-Term clock	5	f_{CYC1} (Note 1)	0	33	0	40			MHz
Macrocell register transmission frequency (without feedback) using FastCLK		f_{CLK} (Note 5)	0	45	0	59			MHz
Macrocell register transmission frequency (without feedback) using a Product-Term clock		f_{CLK1} (Note 5)	0	42	0	50			MHz
Input register transmission frequency (without feedback) using FastCLK		f_{CLK2} (Note 5)	0	50	0	67			MHz
Input register to Macrocell register pipeline freq. using FastCLK	6	f_{CLK3} (Note 1)	0	33	0	40			MHz
FastCLK Low pulse width	10	t_{WL}	10		7.5				ns
FastCLK High pulse width	10	t_{WH}	10		7.5				ns
Product-Term clock pulse width (active/inactive)	10	t_{W1}	12		10				ns
Input to Macrocell register set-up time before FastCLK	8	t_{SU}	29		24				ns
Input to Macrocell register hold time after FastCLK	8	t_{H}	-7		-7				ns
Input to Macrocell register set-up time before FastCLK	7	t_{SU1} (Note 1)	12		10				ns
Input to Macrocell register hold time after Product-Term clock	7	t_{H1}	0		0				ns
Input register/latch set-up time before FastCLK	9	t_{SU2}	10		8				ns
Input register/latch hold time after FastCLK	9	t_{H2}	7		6				ns

XC7272 AC Timing Requirements (Continued)

		Speed Grade	-30		-25				Units
Description	Fig.	Symbol	Min	Max	Min	Max	Min	Max	
FastCompare input set-up time before latch-enable input	11	t_{SU3}	4		2				ns
FastCompare input hold time after latch-enable input	11	t_{H3}	18		14				ns
FastCompare input hold time after comparator jam asserted	11	t_{H4}	30		25				ns
Set/reset pulse width	10	t_{WA}	15		12				ns
Set/reset input recovery set-up time before FastCLK	10	t_{RA}	25		20				ns
Set/reset input hold time after FastCLK	10	t_{HA}	-5		-5				ns
Set/reset input recovery time before P-Term clock	10	t_{RA1}	8		6				ns
Set/reset input hold time after P-Term clock	10	t_{HA1}	12		9				ns
Set/reset input hold time after reset/set inactive		t_{HRS}	12		10				ns
FastCompare latch-enable pulse width	10	t_{WC}	22		16				ns

XC7272 Propagation Delays

		Speed Grade	-30		-25				Units
Description	Fig.	Symbol	Min	Max	Min	Max	Min	Max	
FastCLK input to registered output delay	10	t_{CO}	5	19	5	16			ns
P-Term clock input to registered output delay	10	t_{CO1}	10	36	10	30			ns
Set/reset input to registered output delay	10	t_{AO}	13	48	13	40			ns
Input to nonregistered output delay	10	t_{PD} (Note 1)	13	48	13	40			ns
FastCompare input to MATCH output	11	t_{PDC}	8	26	8	23			ns
FastCompare disable input to MATCH output	11	t_{PDC1}	8	30	8	25			ns
FastCompare jam input to MATCH output	11	t_{PDC2}	8	30	8	25			ns
Input to output enable	10	t_{OE}	11	37	11	32			ns
Input to output disable	10	t_{OD}	11	37	11	32			ns

XC7272 Incremental Parameters

		Speed Grade	-30		-25				Units
Description	Fig.	Symbol	Min	Max	Min	Max	Min	Max	
Arithmetic carry delay between adjacent Macrocells	12	t_{PDT1} (Note 2)		1.9		1.6			ns
Arithmetic carry delay through 9 adjacent Macrocells in a Function Block	12	t_{PDT8} (Note 2)		12		10			ns
Arithmetic carry delay through 10 Macrocells from Macrocell #n to Macrocell #n in next F Block	12	t_{PDT9} (Note 2)		17		14			ns
Incremental delay from FastCLK net to registered output feedback	13	t_{COF}		1		1			ns
Incremental delay from UIM-input (for P-Term clock) to registered Macrocell feedback	13	t_{COF1}		18		15			ns
Incremental delay from FastCLK net to latched/registered UIM-input	13	t_{COF2} (Note 3)		1		1			ns
Incremental delay from UIM-input to nonregistered Macrocell feedback	13	t_{PDF} (Note 1)		30		25			ns
Incremental delay from UIM-input (set/reset) to registered Macrocell feedback	13	t_{AOF}		30		25			ns
Incremental delay from UIM-input (used as output-enable/disable) to Macrocell feedback	13	t_{OEF}, t_{ODF}		19		17			ns
Propagation delay through unregistered Input pad (to UIM) plus output pad driver (from Macrocell)	13	$t_{IN} + t_{OUT}$ (Note 4)		18		15			ns

Note 1. Specifications account for logic paths which use the maximum number of available product terms and the ALU.

Note 2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent MACRO(s) for an adder with registered outputs.

Note 3. Parameter t_{COF2} is derived as the difference between the clock period for pipelining input-to-MACRO reigsters ($1/f_{CLK3}$) and the non-registered input set-up time (t_{SU}).

Note 4. Parameter t_{IN} represents the delay from an input or I/O pin to a UIM-input (or from a FastCLK pin to the Fast CLK net); t_{OUT} represents the delay from a MACRO output (feedback point) to an output or I/O pin. Only the sum of $t_{IN} + t_{OUT}$ can be derived from measurements, e.g., $t_{IN} + t_{OUT} = t_{SU} + t_{CO} - 1/f_{CYC}$.

Note 5. Not tested but derived from appropriate pulse-widths, set-up time and hold-time measurements.

TIMING AND DELAY PATH SPECIFICATIONS

Introduction to XC7272 Timing

Timing calculations and verification for the XC7272 are straightforward. The delay path consists of three blocks that can be connected in series.

- Input Buffer and associated latch or register
- Logic Resource (UIM, AND-array and Macrocell)
- Three-state Output Buffer

All inputs have the same delay, regardless of fan-out or location. All logic resources have the same delay, regardless of logic complexity, interconnect topology or location on the chip. All outputs have the same delay. The achievable clock rate is, therefore, determined only by the input method (direct, latched or registered) and the number of times a signal passes through the combinatorial logic.

Timing and Delay Path Descriptions

Figure 5 defines the max clock frequency (with feedback). Any Macrocell output can be fed back to the UIM as an input for the next clock cycle. Figure 6 shows the relevant delay path. The parameters f_{CYC} and f_{CYC1} specify the maximum operating frequency for FastCLK and product-term clock operation respectively.

Figure 6 specifies the max operating frequency (f_{CLK3}) for pipelined operation between the input registers and the Macrocell registers, using FastCLK.

Figure 7 defines the set-up and hold times from the data inputs to the product-term clock used by the output register.

Figure 8 defines the set-up and hold times from the data inputs to the FastCLK used by the output register.

Figure 9 defines the set-up and hold times from the data input to the FastCLK used in an input register.

Figure 10 shows the waveforms for the Macrocell and control paths.

Figure 11 defines the FastCompare timing parameters.

Figure 12 defines the carry propagation delays between Macrocells and between Function Blocks. The parameters describe the delay from the C_{IN}, D1 and D2 inputs of a Macrocell ALU to the C_{IN} input of the adjacent Macrocell ALU. These delays must be added to the standard Macrocell delay path (t_{PD} or t_{SU}) to determine the performance of an arithmetic function.

Figure 13 defines the incremental parameters for the standard Macrocell logic paths. These incremental parameters are used in conjunction with pin-to-pin parameters when calculating compound logic path timing. Incremental parameters are derived indirectly from other pin-to-pin measurement.

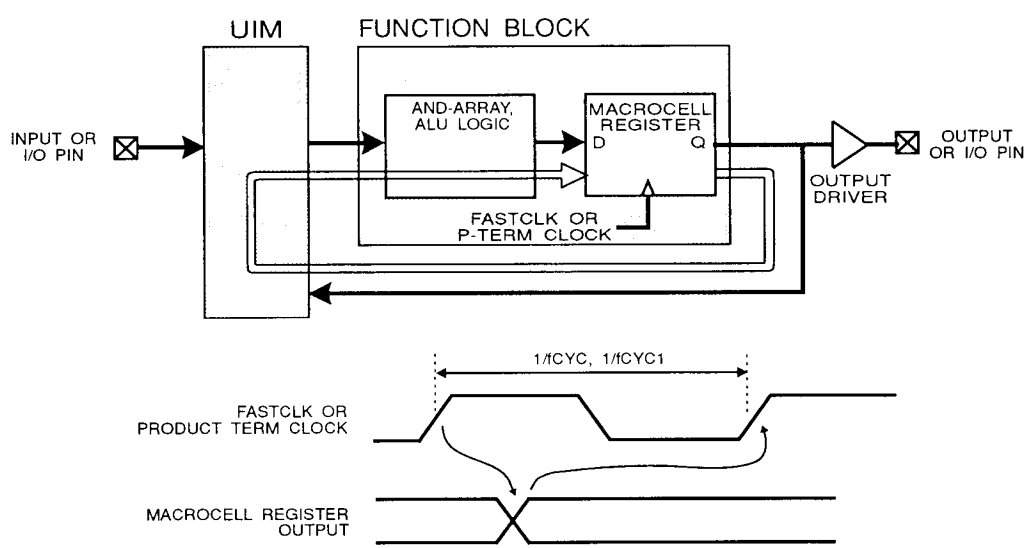


Figure 5. Delay Path Sepcifications for f_{CYC} and f_{CYC1}

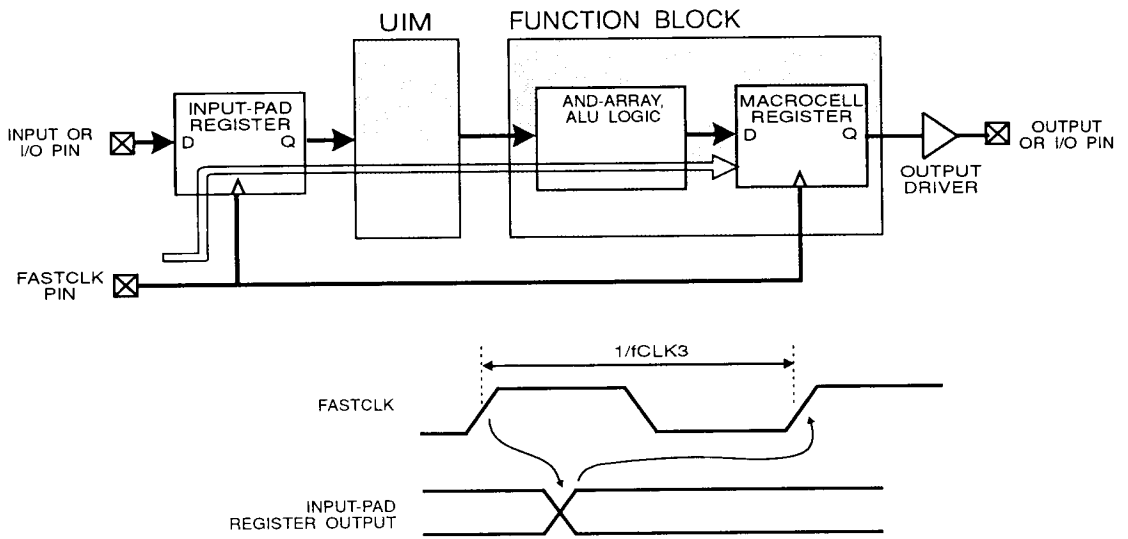


Figure 6. Delay Path Specification for f_{CLK3}

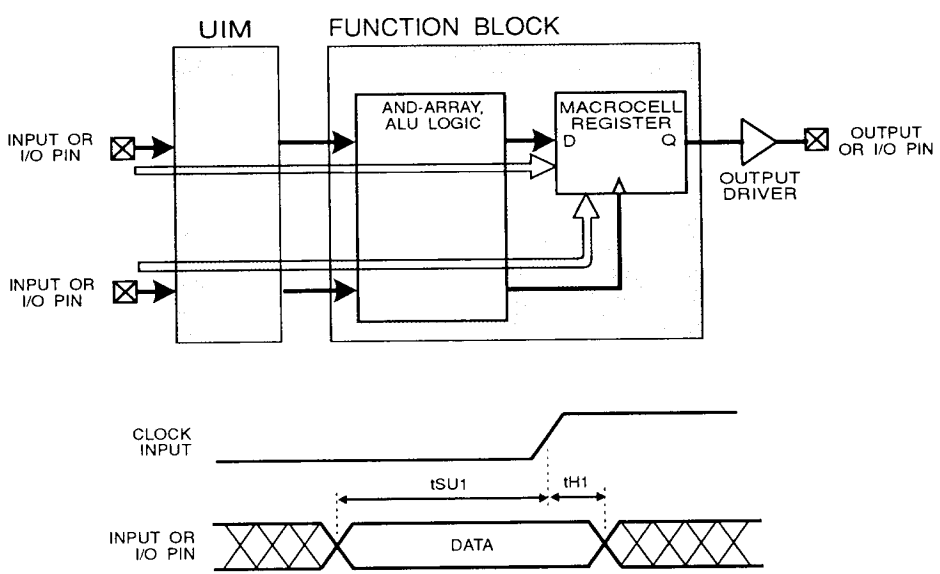


Figure 7. Delay Path Specification for t_{SU1} and t_{H1}

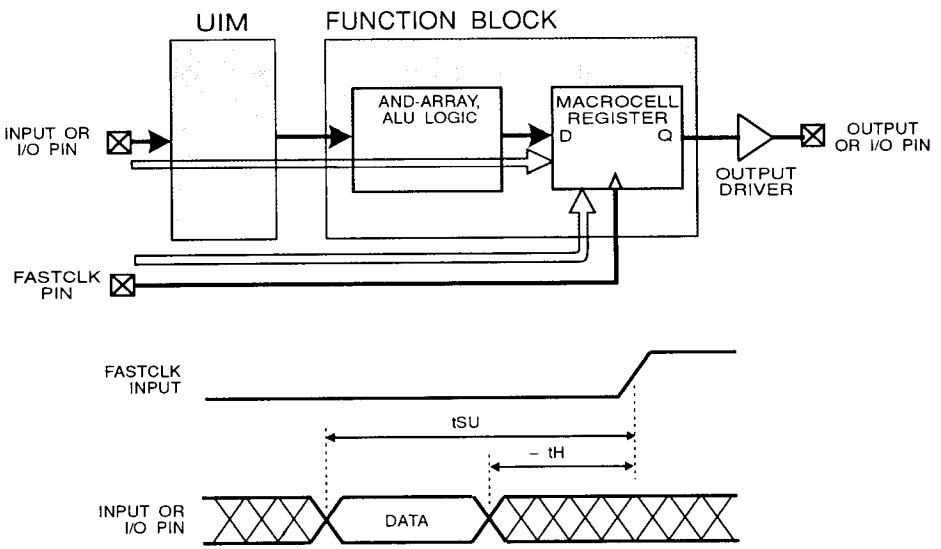


Figure 8. Delay Path Specification for t_{SU} and t_H

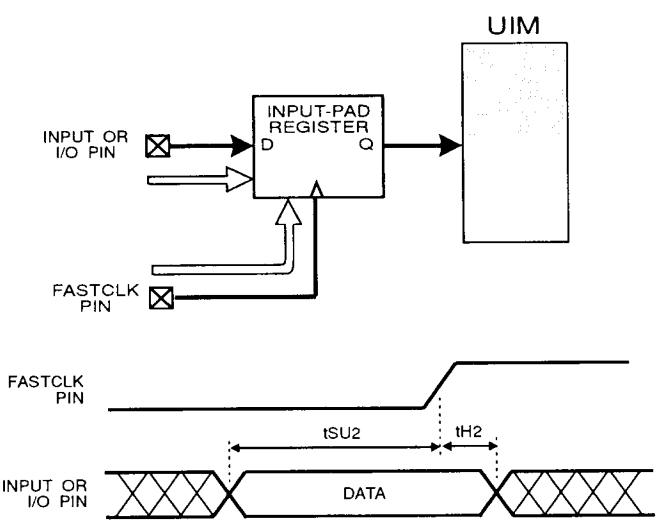


Figure 9. Delay Path Specification for t_{SU2} and t_{H2}

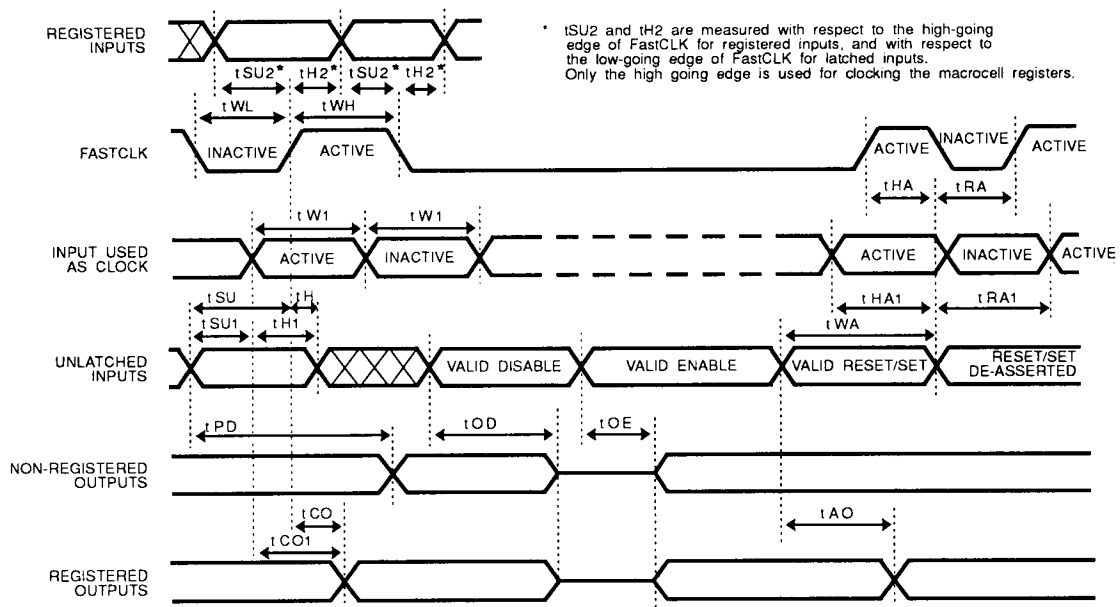


Figure 10. Principal Pin-to-Pin Measurements

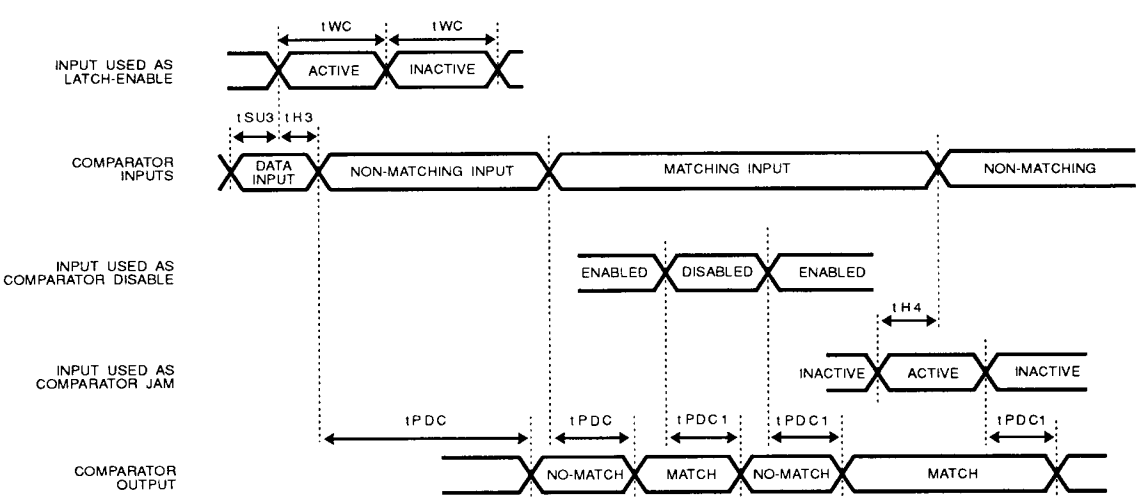


Figure 11. FastCompare Timing Waveforms

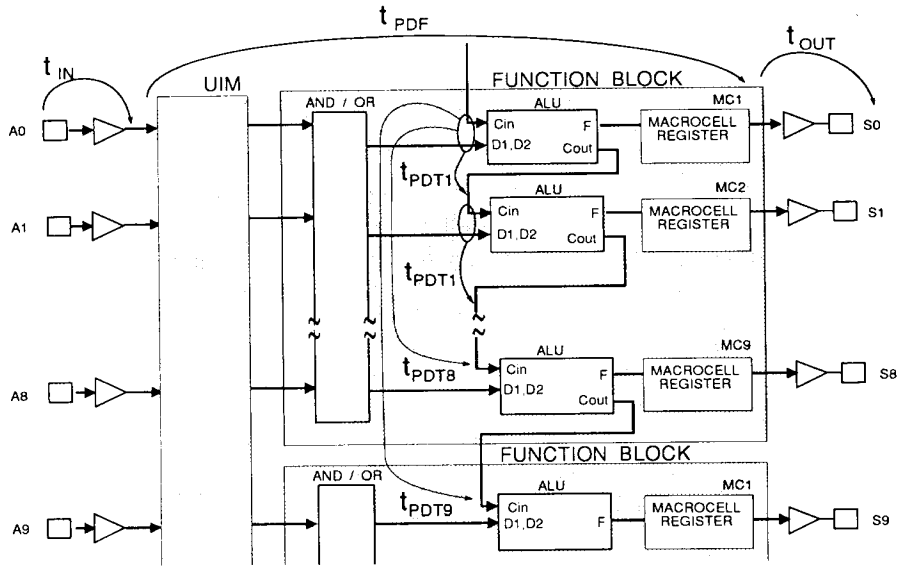


Figure 12. Arithmetic Timing Parameters

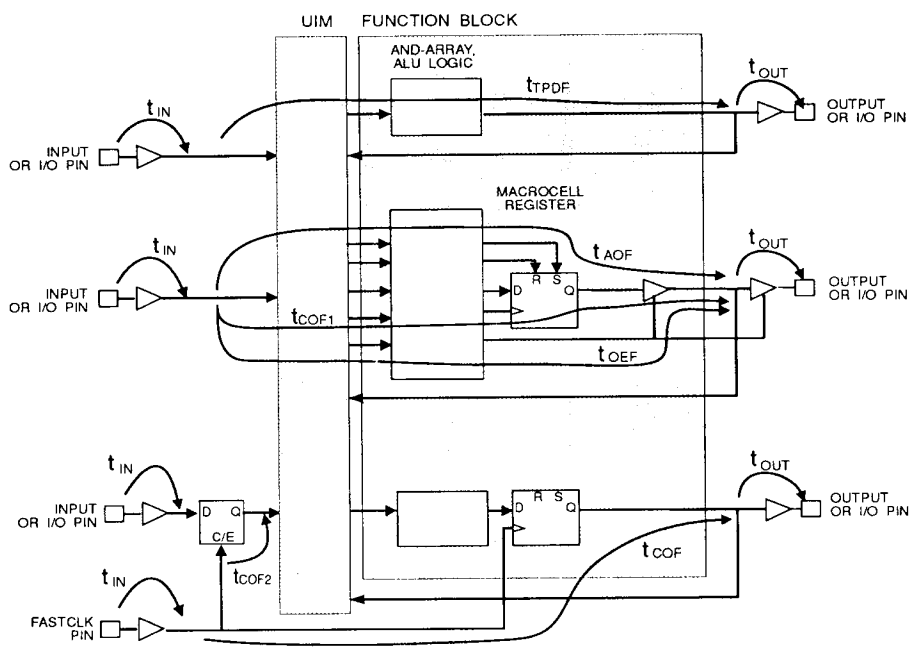


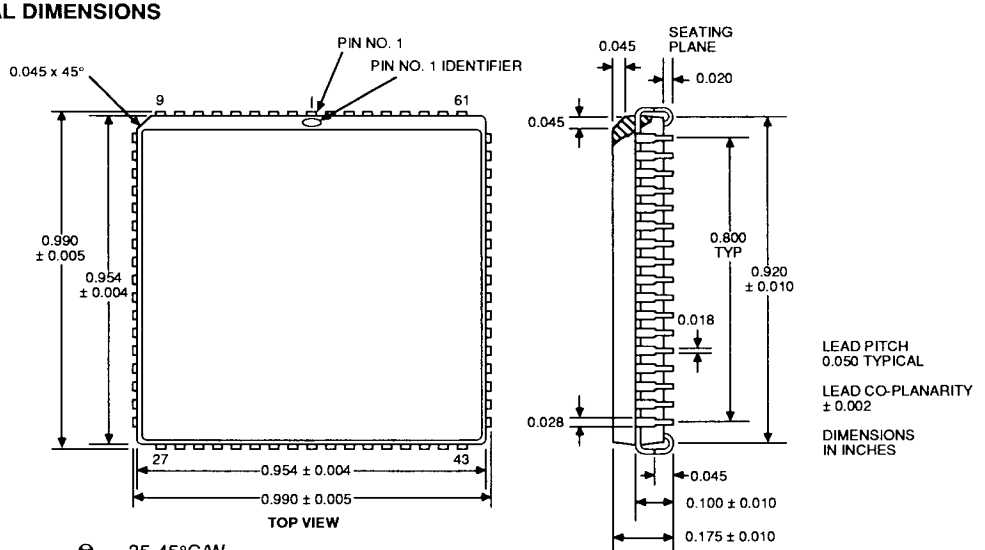
Figure 13. Incremental Timing Parameters

68-Pin LCC, 84-Pin LCC and PGA Pinouts

68 LCC	in XC7272 out	84 LCC	84 PGA
1	Master Reset VPP	1	F-9
2	Input/FCI	2	F-11
-	Input/FCI	3	E-11
-	Input/FCI	4	E-10
3	Input/FCI	5	E-9
4	Input/FCI	6	D-11
5	Input/FCI	7	D-10
6	GROUND	8	C-11
7	Fast CLK0 MC4-4	9	B-11
8	Fast CLK1 MC4-3	10	C-10
9	Input MC4-2	11	A-11
10	Input MC4-1	12	B-10
11	MC3-8	13	B-9
12	MC3-7	14	A-10
13	MC3-6	15	A-9
14	MC3-5	16	B-8
15	GROUND	17	A-8
-	MC3-4	18	B-6
-	MC3-3	19	B-7
-	MC3-2	20	A-7
-	MC3-1	21	C-7
16	Vcc	22	C-6
17	Input MC2-9	23	A-6
18	Input MC2-8	24	A-5
19	Input MC2-7	25	B-5
20	Input MC2-6	26	C-5
21	GROUND	27	A-4
22	Input MC2-5	28	B-4
23	Input MC2-4	29	A-3
24	Input MC2-3	30	A-2
25	Input MC2-2	31	B-3
26	Input MC2-1	32	A-1
27	Input MC1-9	33	B-2
28	Input MC1-8	34	C-2
29	Input MC1-7	35	B-1
30	Input MC1-6	36	C-1
31	GROUND	37	D-2
32	Input MC1-5	38	D-1
33	Input MC1-4	39	E-3
34	Input MC1-3	40	E-2
-	Input MC1-2	41	E-1
-	Input MC1-1	42	F-2

68 LCC	in XC7272 out	84 LCC	84 PGA
35	Vcc	43	F-3
-	Input MC8-9	44	G-3
-	Input MC8-8	45	G-1
36	Input MC8-7	46	G-2
37	Input MC8-6	47	F-1
38	Input MC8-5	48	H-1
39	GROUND	49	H-2
40	Input MC8-4	50	J-1
41	Input MC8-3	51	K-1
42	Input MC8-2	52	J-2
43	Input MC8-1	53	L-1
44	Input MC7-9	54	K-2
45	Input MC7-8	55	K-3
46	Input MC7-7	56	L-2
47	Input MC7-6	57	L-3
48	Input MC7-5	58	K-4
49	GROUND	59	L-4
50	Input MC7-4	60	J-5
51	Input MC7-3	61	K-5
52	Input MC7-2	62	L-5
53	Input MC7-1	63	K-6
54	Vcc	64	J-6
55	MC6-8	65	J-7
56	MC6-7	66	L-7
57	MC6-6	67	K-7
58	MC6-5	68	L-6
59	GROUND	69	L-8
-	MC6-4	70	K-8
-	MC6-3	71	L-9
-	MC6-2	72	L-10
-	MC6-1	73	K-9
60	Input MC5-4	74	L-11
61	Input MC5-3	75	K-10
62	Input MC5-2/FCO	76	J-10
63	Input MC5-1/FCO	77	K-11
64	GROUND	78	J-11
65	Input/FCI	79	H-10
66	Input/FCI	80	H-11
67	Input/FCI	81	F-10
68	Input/FCI	82	G-10
-	Input/FCI	83	G-11
-	Input/FCI	84	G-9

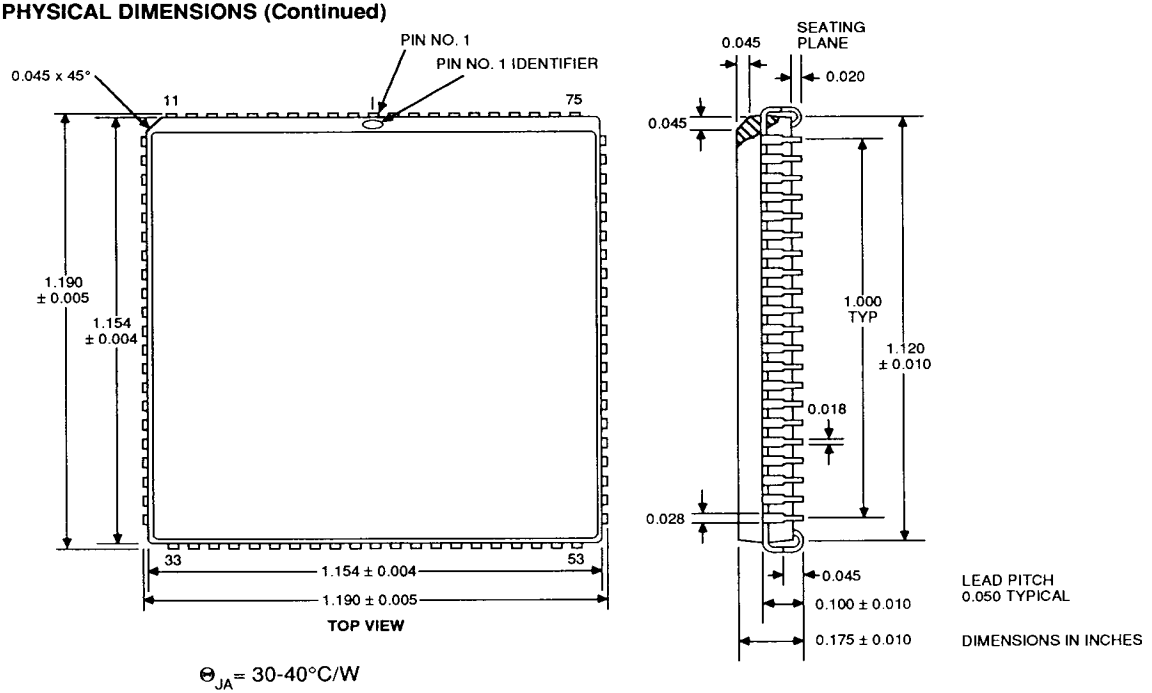
PHYSICAL DIMENSIONS



Θ_{JA} = 35-45°C/W

68-Pin PLCC and WLCC Packages

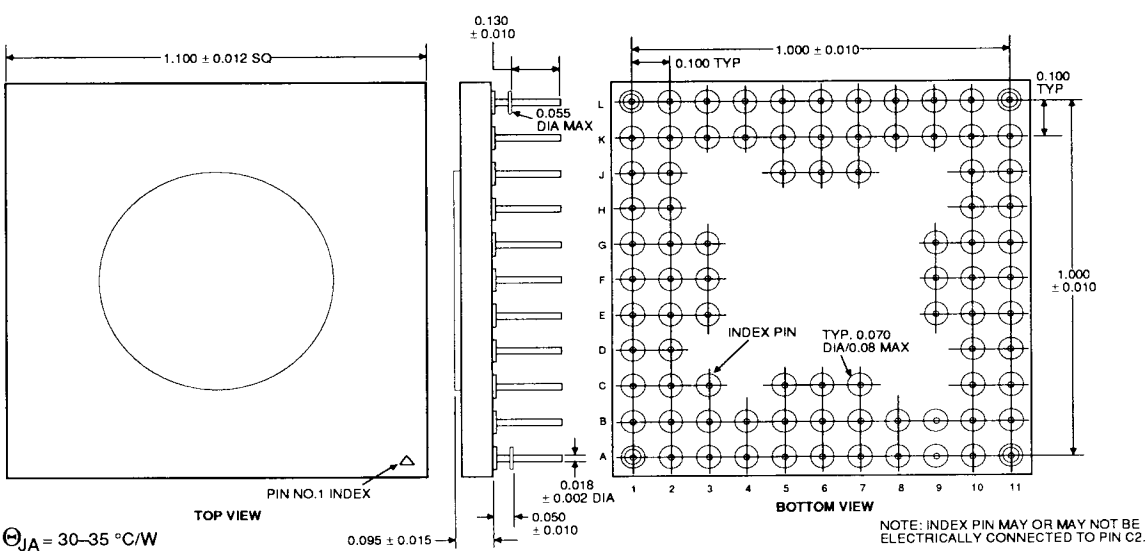
PHYSICAL DIMENSIONS (Continued)



Θ_{JA} = 30-40°C/W

1105 36C

84-Pin Plastic Leaded Chip Carrier and Windowed Ceramic Leaded Chip Carrier Packages



Θ_{JA} = 30–35 °C/W

NOTE: INDEX PIN MAY OR MAY NOT BE ELECTRICALLY CONNECTED TO PIN C2.

DIMENSIONS IN INCHES

1105 35C

84-Pin Windowed Ceramic Pin Grid Array Package