LINEAR INTEGRATED CIRCUIT UTC X3211

FET BIAS CONTROLLER WITH POLARISATION SWITCH AND TONE DETECTION

DESCRIPTION

The UTC X3211 is designed to meet the bias requirements of GaAs and HEMT FETs commonly used in satellite receiver LNBs, PMR, cellular telephones etc. with a minimum of external components.

FEATURES

- * Provides bias for GaAs and HEMT FETs
- * Drives up to three FETs
- * Dynamic FET protection
- * Drain current set by external resistor
- * Polarisation switch for LNBs -supporting zero volt gate COM switching topology.

G1

D1 2

G2 3

D2

G3

D3

GND

CNB1

4

5

6

8 Сив2 9

N/C 10

* 22kHz tone detection for band switching

APPLICATIONS

- *Satellite receiver LNBs
- * Private mobile radio (PMR)
- * Cellular telephones

UTC

PIN CONFIGURATION





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20 Vcc

19

18

17

16

15

14

13 Нв

12 Lв

11

RCAL

VPOL

FIN

N/C

Fout

Lov

CSUB



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	Vcc	-0.6~12	V
Supply Current	Icc	100	mA
Drain Current (per FET) (set by RCAL)	I _D	0~15	mA
Input Voltage (VPOL)	Vin	25 continuous	V
Operating Temperature	Topr	-40~70	°C
Storage Temperature	T _{Stg}	-50~85	°C
Power Disspation(Ta=25°C)	PD	500	mW

ELECTRICAL CHARACTERISTICS

(Ta = 25 °C,Vcc=5V,ID=10mA, Rcal =33k Ω Unless otherwise specified)

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PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	Vcc		5		10	V
Supply Current	Icc	ID1 to ID3=0		6	15	mA
		ID1 =0, ID2 to ID3=10mA,VPOL=14V		25	35	mA
		ID2=0, ID1 to ID3=10mA,VPOL=15.5V		25	35	mA
		ID1 to ID3=0,ILB=10mA		16	25	mA
		ID1 to ID3=0,Iнв=10mA		16	25	mA
Substrate Voltage	V _{SUB}	(Internally generated) I _{SUB} =0	-3.5	-3	-2.5	V
		I _{SUB} = -200μA			-2.4	V
Output Noise						
Drain Voltage	END	Cg=4.7nF,CD=10nF			0.02	Vpkpk
Gate Voltage	Eng	Cg=4.7nF,CD=10nF			0.005	Vpkpk
Oscillator Freq	fo		200	350	800	kHz

GATE CHARACTERISTICS

F	PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output (Current Range	lgo		-30		2000	μA
Output V	Voltage						
Gate 1	Off	Vg10	ID1=0mA, VPOL=14V, IGO1=0μA	-0.05	0	0.05	V
	Low	VG1L	ID1=12mA, VPOL=15.5V, IGO1=-10μA	-2.7	-2.4	-2	v
	High	Vg1h	ID1=8mA, VPOL=15.5V, IGO1=0μA	0.4	0.75	1.0	
Output V	Voltage						
Gate 2	Off	Vg20	ID2=0mA, VPOL=15.5V, IGO2=0μA	-0.05	0	0.05	V
	Low	Vg2L	ID2=12mA, VPOL=14V, IGO2=-10μA	-2.7	-2.4	-2	v
	High	Vg2h	ID2=8mA, VPOL=14V, IGO2=0μA	0.4	0.75	1.0	
Output V	Voltage						
Gate 3	Low	Vg3l	ID3=12mA, IGO3=-10μA	-3.5	-2.9	-2	V
	High	Vдзн	ID3=8mA, IGO3=0μA	0.4	0.75	1.0	

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DRAIN CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current	lD		8	10	12	mA
Current Change With Vcc	Δ Inv	Vcc=5 to12V		0.5		%/\/
With Tj	∆ IDT	Tj= -40 to +70°C		0.05		%/°C
Drain 1 Change : High	VD1	ID1 =10mA VPOL=15.5V	1.8	2.0	2.2	V
Drain 2 Change : High	Vd2	ID2 =10mA VPOL=14V	1.8	2.0	2.2	V
Drain 3 Change : High	Vd3	ID3 =10mA	1.8	2.0	2.2	V
Voltage Change						
With Vcc	$\DeltaV\text{dv}$	Vcc=5 to10V		0.5		%/V
With Tj	ΔVdt	Tj= -40 to +70°C		50		ppm
Leakage Current						
Drain 1	IL1	VD1=0.5V, VPOL=14V			10	μA
Drain 2	L2	VD2=0.5V, VPOL=15.5V			10	

TONE DETECTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Filter Amplifier						μA
Input Bias Current	lв	RF1=150k Ω	0.02	0.07	0.25	
Output Voltage ⁵	Vout	RF1=150k Ω	1.75	1.95	2.05	V
Output Current ⁵	lout	Vout=1.96V, Vfin=2.1V	400	520	650	μA
Voltage Gain	Gv	f=22kHz, Vin=1mV		46		dB
Rejection Frequency	f _R	V(AC)IN=1V p/p sq.w ⁶	1.0	7.5		kHz
V Threshold ⁵	FVT		100		350	mV p/p
Output Stage						
Lov Volt.Range	VLOV	I∟=50mA(Lв or Hв)	-0.5		Vcc-1.8	V
Lov Bias Current	LOV	VLOV=0	0.02	0.15	1.0	μA
LB Output Low	Mu pu	VLOV=0, IL= -10μA, Enable ⁶	-3.5	-2.75	-2.5	V
	VLBL	VLOV=3V, IL=0, Enable ⁷	-0.01	0	0.01	V
LB Output High	Vlbh	VLOV=0, IL=10 mA, Disable ⁶	-0.025	0	0.025	V
		VLOV=3V, IL=50mA, Disable ⁷	2.9	3.0	3.1	V
HB Output Low	Vhbl	VLOV=0, IL= -10 µ A, Disable ⁶	-3.5	-2.75	-2.5	V
		VLOV=3V, IL=0, Disable ⁷	-0.01	0	0.01	V
Нв Output High	Musu	VLOV=0, IL=10mA, Enable ⁶	-0.025	0	0.025	V
	V HBH	VLOV=3V, IL=50mA, Enable ⁷	2.9	3.0	3.1	V

POLY SWITCH CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Current	IPOL	VPOL=25V (Applied via RPOL=10k $\Omega)$	10	20	40	μA
Threshold Voltage	VTPOL	VPOL=25V (Applied via RPOL=10k Ω)	14	14.75	15.5	V
Switching Speed	TSPOL	VPOL=25V (Applied via RPOL=10k Ω)			100	ms

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NOTES:

- 1. The negative bias voltages specified are generated on-chip using an internal oscillator. Two external capacitors, CNB and CsuB of 47nFare required for this purpose.
- 2. The characteristics are measured using an external reference resistors RCAL of value 33k Ω wired from pins RCAL to ground.
- 3. Noise voltage is not measured in production.
- 4. Noise voltage measurement is made with FETs and gate drain capacitors in place on all outputs. CG,4.7nF,are connected between gate outputs and ground,CD,10nF,are connected between drain outputs and ground.
- 5. These parameters are linearly related to Vcc
- 6. These parameters are measured using Test Circuit 1
- 7. These parameters are measured using Test Circuit 2

TEST CIRCUIT 1



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LINEAR INTEGRATED CIRCUIT

TEST CIRCUIT 2



TYPICAL CHARACTERISTICS



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Vcc o lр DΝ VD Sense Set $\hat{}$ ОN ID Set RCAL GN RCAL Sets ID $20 \,\mu \, \text{A}$ C CSUB Negative Supply GND Gen. CSUB CNB1 CNB2 Сив

FUNCTIONAL DESCRIPTION

FUNCTIONAL DIAGRAM

The X3211 provides all the bias requirements for external FETs, including the generation of the negative supply required for gate biasing, from the single supply voltage. It contains 3 such stages. The negative rail generator is common to all devices.

The drain voltage of the external FET Q_N is set by the X3211 device to its normal operating voltage. This is determined by the on board VD Set reference, the X3211 provides nominally 2 volts .

The drain current taken by the FET is monitored by the low value resistor ID Sense. The amplifier driving the gate of the FET adjusts the gate voltage of QN so that the drain current taken matches the current called for by an external resistor RCAL.

Since the FET is a depletion mode transistor, it is usually necessary to drive its gate negative with respect to ground to obtain the required drain current. To provide this capability powered from a single positive supply, the device includes a low current negative supply generator. This generator uses an internal oscillator and two external capacitors, CNB and CSUB.

The following schematic shows the function of the Vpol input. Only one of the two external FETs numberd Q1 and Q2 are powered at any one time, their selection is controlled by the input Vpol. This input is designed to be wired to

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the power input of the LNB via a high value (10k) resistor. With th input voltage of the LNB set at or below 14V.FET Q2 will be enabled. With the input voltage at or above 15.5V,FET Q1 will be enabled. The disabled FET has its gate driven to 0V and its drain terminal is switched open circuit.FET number Q3 is always active regardless of the voltage applied to Vpol.



Control input switch function

INPUT SENSE	POLARISATION	SELECT
<= <= ≤14 volts	Vertical	FET Q2
≥15.5 volts	Horizontal	FET Q1

For many LNB application tone detection and band switching is required. The X3211 includes the circuitry necessary to detect the presence of a 22kHz tone modulated on the supply input to the LNB.Referring to the following schematic diagram, the main elements of this detector are an op-amp enabling the construction of a Sallen key filter, a rectifier/smoother and a comparator. Full control is given over the center frequency and bandwidth of the filter

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by the selection of two external resistors and capacitors (one of these resistors,R2, shares the function of overvoltge protection of pin Vpol).



APPLICATION CIRCUIT



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APPLICATIONS INFORMATION

The device is a partial application circuit for the X3211 showing all external components required for appropriate biasing. The bias circuits are unconditionally stable over the full temperature range with the associated FETs and gate drain capacitors in circuit.

Capacitors Cb and Cg ensure that residual power supply and substrate generator noise is not allowed to affect other external circuits which may be sensitive to RF interference. They also serve to suppress any potential RF feedthrough between stages via the X3211. These capacitor are required for all stages used Values of 10nF and 4.7nF respectively are recommended however this is design dependent and any value between 1nFand 100nF could be used.

The capacitors CNB and CSUB are an integral part of the X3211 negative supply generator. The negative bias voltage is generated on-chip using an internal oscillator. The required value of capacitors CNB and CSUB is 47nF. This generator produces a low current supply of approximately –3 volts. Although this generator is intended purely to bias the external FETs, it can be used to power other external circuits via the CSUB pin.

Resistors RCAL sets the drain current at which all external FETs are operated. If any bias control circuit is not required, its related drain and gate connections may be left open circuit without affecting the operation of the remaining bias circuits.

The X3211 has been designed to protect the external FETs from adverse operating conditions. With a JFET connected to any bias circuit, the gate output voltage of the bias circuit can not exceed the range –3.5V to 1V,under any conditions including power up and powerdown transients. Should the negative bias generator be shorted or overloaded so that the drain current of the external FETs can no longer be controlled, the drain supply to FETs is shut down to avoid damage to the FETs by excessive drain current.

Tone detection and band switching is provided on the X3211. The following diagrams describes how this feature operates in an LNB and the external components required. The presence or absence of a 22kHz tone applied to pin FIN enables one of two outputs, LB and HB.A tone present enables HB and tone absent enables LB. The LB and HB outputs are designed to be compatible with both MMIC and discrete local oscillator applications, selected by pin Lov. Referring to Figure 1 wiring pin Lov to ground will force LB and HB to switch between –2.6V (disabled) and 0V (enabled).Referring to Figure 2 wiring pin Lov to a positive voltage source (e.g. a potential divider across Vcc and ground set to the required oscillator supply,Vosc when enabled.

Lov	Fin	Lв	Нв	Lв	Нв
GND	22kHz	Disabled	Enabled	-2.6 volts	GND
OND	-	Enabled	Disabled	GND	-2.6 volts
CHIP	22kHz	Disabled	Enabled	Note 1	Vosc
GND	-	Enabled	Disabled	Vosc	Note 1

Tone Detection Function

Note 1: 0 volts in typical LNB applications but dependent on external circuits.

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APPLICATIONS INFORMATION (cont)



Figure 2 Lov connected to Vosc

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