Nonvolatile Static RAM

FEATURES

- **Single 5V Supply**
- **Fully TTL Compatible**
- **Infinite E²PROM Array Recall, RAM Read and Write Cycles**
- **Access Time of 300 ns Max.**
- **Nonvolatile Store Inhibit: V_{CC} = 3V Typical**
- **High Reliability**
  - **—Store Cycles: 10,000**
  - **—Data Retention: 100 Years**

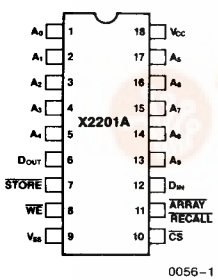
DESCRIPTION

The Xicor X2201A is a 1024 x 1 NOVRAM featuring a high-speed static RAM overlaid bit-for-bit with a nonvolatile E²PROM. The X2201A is fabricated with the same reliable N-channel floating gate MOS technology used in all Xicor 5V nonvolatile memories.

The NOVRAM design allows data to be easily transferred from RAM to E²PROM (store) and from E²PROM to RAM (recall). The store operation is completed in 10 ms or less and the recall is typically completed in 1 μs.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or recalls from E²PROM. The E²PROM array is designed for a minimum 10,000 store cycles and inherent data retention is specified to be greater than 100 years. Refer to RR-520 and RR-515 for details on Xicor nonvolatile memory endurance and data retention characteristics.

PIN CONFIGURATION



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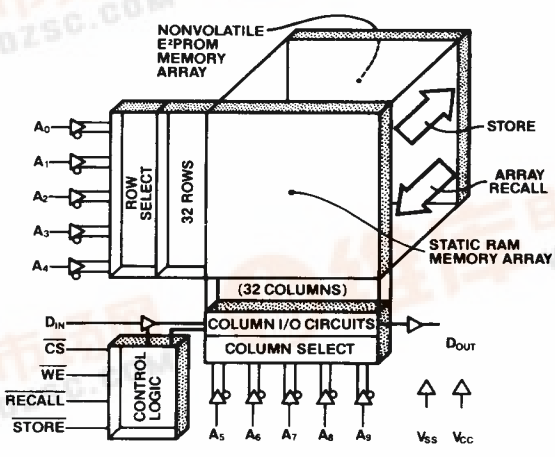
PIN NAMES

A_0–A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Out
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
$\overline{ARRAY\ RECALL}$	Array Recall
$\overline{STORE}$	Store
V_{CC}	+5V
V_{SS}	Ground

FUNCTIONAL DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin with
Respect to Ground ..... −1.0V to +7V
D.C. Output Current ..... 5 mA
Lead Temperature
(Soldering, 10 Seconds) ..... 300°C

*COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. OPERATING CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits		Units	Test Conditions
		Min.	Max.		
I_{CC}	Power Supply Current		60	mA	All Inputs = V_{CC} $I_{I/O}$ = 0 mA
I_{LI}	Input Load Current		10	µA	V_{IN} = GND to V_{CC}
I_{LO}	Output Leakage Current		10	µA	V_{OUT} = GND to V_{CC}
V_{IL}(2)	Input Low Voltage	−1.0	0.8	V	
V_{IH}(2)	Input High Voltage	2.0	V_{CC} +1.0	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 4.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −2 mA

ENDURANCE AND DATA RETENTION

Parameter	Min.	Units	Conditions
Endurance	1,000	Data Changes Per Bit	Xicor Reliability Reports RR-520 and RR-504
Store Cycles	10,000	Store Cycles	Xicor Reliability Reports RR-520 and RR-504
Data Retention	100	Years	Xicor Reliability Report RR-515

CAPACITANCE T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Units	Conditions
$C_{I/O}$(1)	Input/Output Capacitance	8	pF	$V_{I/O}$ = 0V
C_{IN}(1)	Input Capacitance	6	pF	V_{IN} = 0V

Notes: (1) This parameter is periodically sampled and not 100% tested.
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

A.C. CONDITIONS OF TEST

Input Pulse Levels	0V to 3.0V
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	1.5V
Output Load	1 TTL Gate and C_L = 100 pF

MODE SELECTION

Inputs				Input Output I/O	Mode
$\overline{CS}$	$\overline{WE}$	ARRAY RECALL	STORE		
H	X	H	H	Output High Z	Not Selected(3)
L	H	H	H	Output Data	Read RAM
L	L	H	H	Input Data High	Write "1" RAM
L	L	H	H	Input Data Low	Write "0" RAM
X	H	L	H	Output High Z	Array Recall
H	X	L	H	Output High Z	Array Recall
X	H	H	L	Output High Z	Nonvolatile Storing(4)
H	X	H	L	Output High Z	Nonvolatile Storing(4)

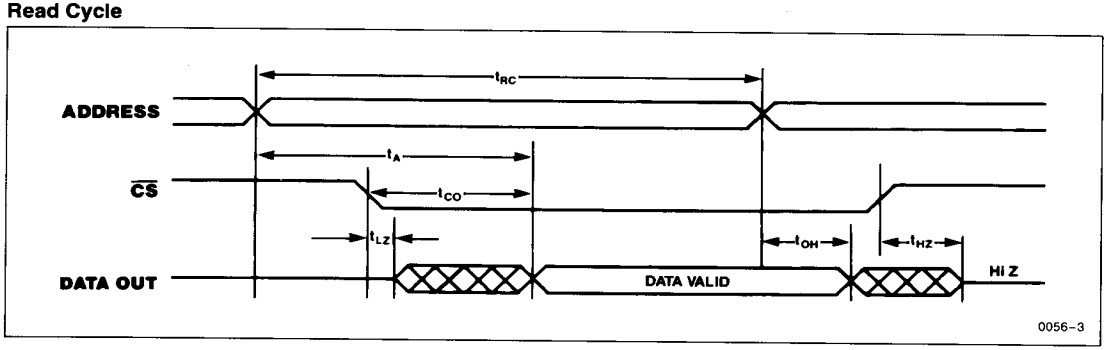
A.C. CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ±10%, unless otherwise specified.

Read Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RC}	Read Cycle Time	300		ns
t_A	Access Time		300	ns
t_{CO}	Chip Select to Output Valid		200	ns
t_{OH}	Output Hold from Address Change	50		ns
t_{LZ}(5)	Chip Select to Output in Low Z	10		ns
t_{HZ}(5)	Chip Deselect to Output in High Z	10	100	ns

Read Cycle



Notes: (3) Chip is deselected but may be automatically completing a store cycle.

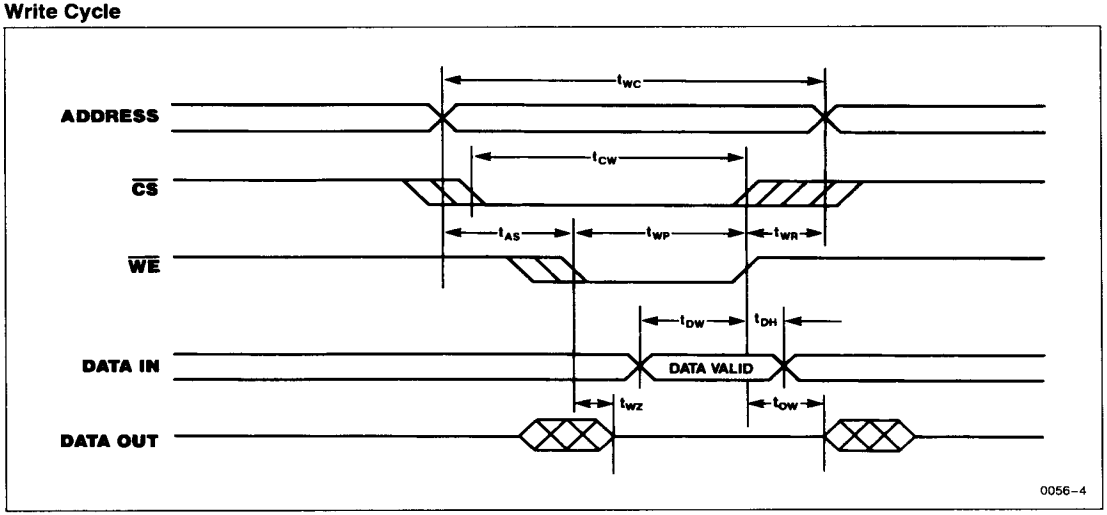
(4) $\overline{STORE}$ = L is required only to initiate the store cycle, after which the store cycle will be automatically completed ($\overline{STORE}$ = X).

(5) t_{LZ} min. and t_{HZ} min. are periodically sampled and not 100% tested.

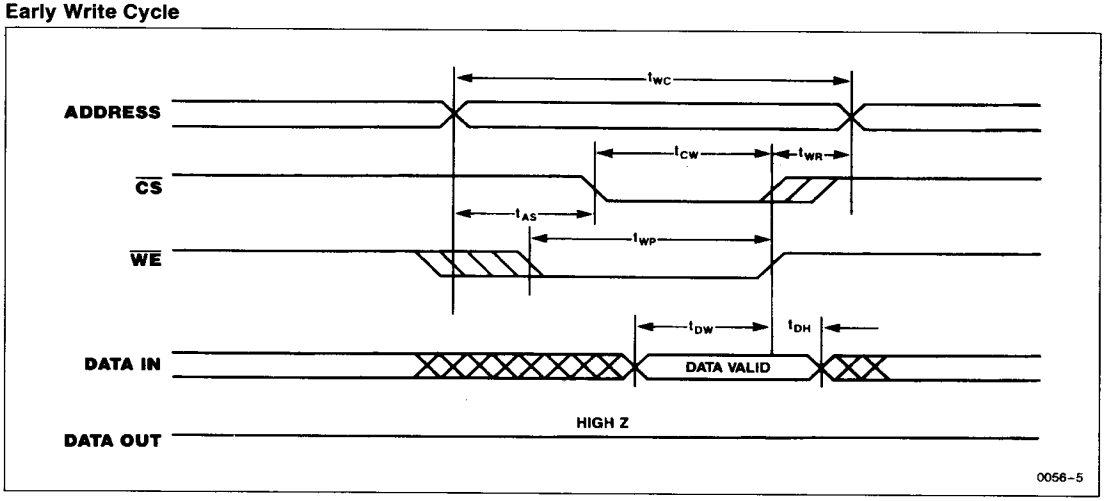
Write Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{WC}	Write Cycle Time	300		ns
t_{CW}	Chip Select to End of Write	150		ns
t_{AS}	Address Setup Time	50		ns
t_{WP}	Write Pulse Width	150		ns
t_{WR}	Write Recovery Time	25		ns
t_{DW}	Data Valid to End of Write	100		ns
t_{DH}	Data Hold Time	0		ns
t_{WZ}	Write Enable to Output in High Z	10	100	ns
t_{OW}	Output Active from End of Write	10		ns

Write Cycle



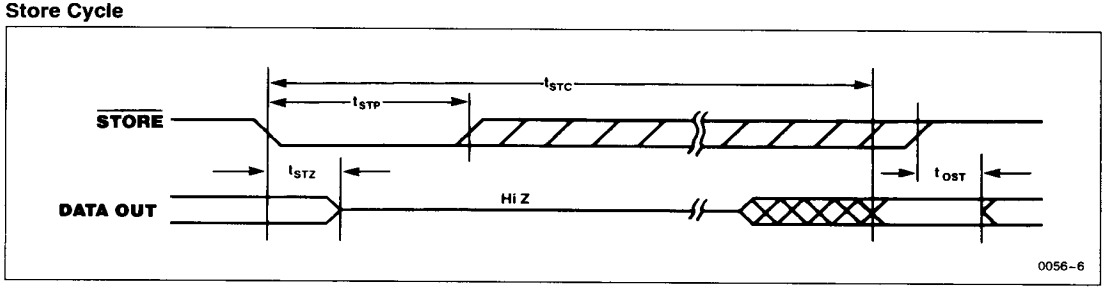
Early Write Cycle



Store Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{STC}	Store Time		10	ms
t_{STP}	Store Pulse Width	100		ns
t_{STZ}	Store to Output in High Z		500	ns
t_{OST}	Output Active from End of Store	10		ns

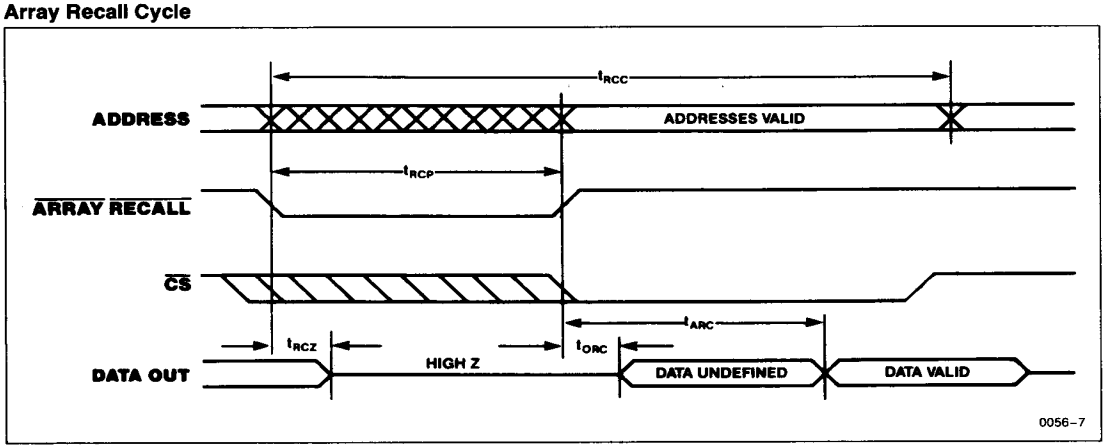
Store Cycle



Array Recall Cycle Limits

Symbol	Parameter	Min.	Max.	Units
t_{RCC}	Array Recall Cycle Time	1200		ns
t_{RCP}	Recall Pulse Width(6)	450		ns
t_{RCZ}	Recall to Output in High Z		150	ns
t_{ORC}	Output Active from End of Recall	10		ns
t_{ARC}	Recalled Data Access Time from End of Recall		750	ns

Array Recall Cycle



Note: (6) Array Recall rise time must be less than 1 μs.

PIN DESCRIPTIONS AND DEVICE OPERATION

Addresses (A_0–A_9)

The address inputs select a memory location during a read or write operation.

Chip Select ($\overline{CS}$)

The Chip Select input must be LOW to enable read/write operations with the RAM array. $\overline{CS}$ HIGH will place the D_{OUT} in the high impedance state.

Write Enable ($\overline{WE}$)

The Write Enable input controls the D_{OUT} buffer, determining whether a RAM read or write operation is enabled. $\overline{WE}$ HIGH enables a read and $\overline{WE}$ LOW enables a write.

Data In (D_{IN})

Data is written into the device via the D_{IN} input.

Data Out (D_{OUT})

Data from a selected address is output on the D_{OUT} output. This pin is in the high impedance state when either $\overline{CS}$ is HIGH or when $\overline{WE}$ is LOW.

$\overline{STORE}$

The $\overline{STORE}$ input, when LOW, will initiate the transfer of the entire contents of the RAM array to the E²PROM array. The $\overline{WE}$ and $\overline{ARRAY\ RECALL}$ inputs are inhibited during the store cycle. The store operation will be completed in 10 ms or less.

A store operation has priority over RAM read/write operations. If $\overline{STORE}$ is asserted during a read operation, the read will be discontinued. If $\overline{STORE}$ is asserted during a RAM write operation, the write will be immediately terminated and the store performed. The data at the RAM address that was being written will be unknown in both the RAM and E²PROM.

$\overline{ARRAY\ RECALL}$

The $\overline{ARRAY\ RECALL}$ input, when LOW, will initiate the transfer of the entire contents of the E²PROM array to the RAM array. The transfer of data will typically be completed in 1 μs or less.

An array recall has priority over RAM read/write operations and will terminate both operations when $\overline{ARRAY\ RECALL}$ is asserted. $\overline{ARRAY\ RECALL}$ LOW will also inhibit the $\overline{STORE}$ input.

WRITE PROTECTION

The X2201A has three write protect features that are employed to protect the contents of the nonvolatile memory.

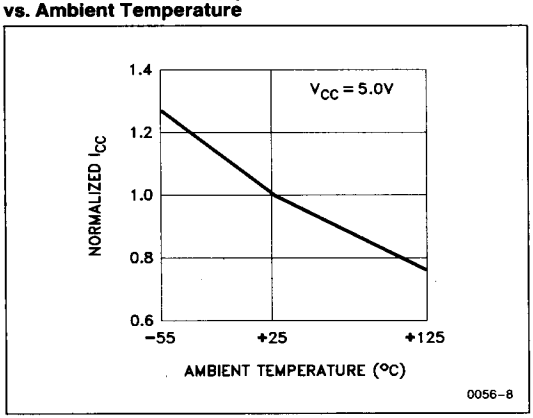
- V_{CC} Sense—All functions are inhibited when V_{CC} is ≤3V, typically.
- Write Inhibit—Holding either $\overline{STORE}$ HIGH or $\overline{ARRAY\ RECALL}$ LOW during power-up or power-down will prevent an inadvertent store operation and E²PROM data integrity will be maintained. It should be noted; whichever method is employed, all control inputs should be stable and the device deselected prior to release of the controlling protection signal.
- Noise Protection—A $\overline{STORE}$ pulse of less than 20 ns (typical) will *not* initiate a store cycle.

Part Number	Store Cycles	Data Changes Per Bit
X2201A	10,000	1,000

SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Normalized Active Supply Current vs. Ambient Temperature



Normalized Access Time vs. Ambient Temperature