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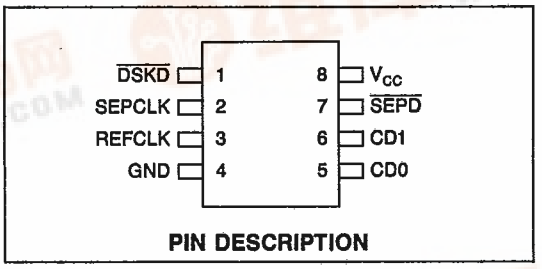
WD92C32
Digital Phase Lock Loop Disk Data Separator (DPLL)

FEATURES

- Performs complete data separation function for floppy disk drives
- Separates FM or MFM encoded data from any magnetic media
- Contains internal power up reset and all logic to provide classical 2nd order, type 2, phase locked loop performance
- Eliminates several SSI and MSI devices normally used for data separation
- No external adjustments or additional logic required
- Superior performance in terms of available bit jitter window tolerance
- TTL compatible inputs and outputs
- Small 8 pin dual-in-line package
- Single +5 volt power supply



PIN DESCRIPTION

DESCRIPTION

The WD92C32 Digital Phase Lock Loop Disk Data Separator (DPLL) is a CMOS LSI that was designed to address high performance error rates on floppy disk drives. The DPLL is a product with TTL compatible I/O which operates from a single +5 volt power supply. Supplied in an 8 pin dual-in-line package, the WD92C32 represents significant cost savings versus the analog components required to equal its performance.

The WD92C32 contains an internal power-up reset along with all the necessary logic to achieve classical 2nd order, type 2, phase locked loop performance. Implemented digitally, the WD92C32 does not require any external adjustments or any additional logic to perform data separation.

Figure 1 illustrates a typical system with the WD92C32 used as the data separator.

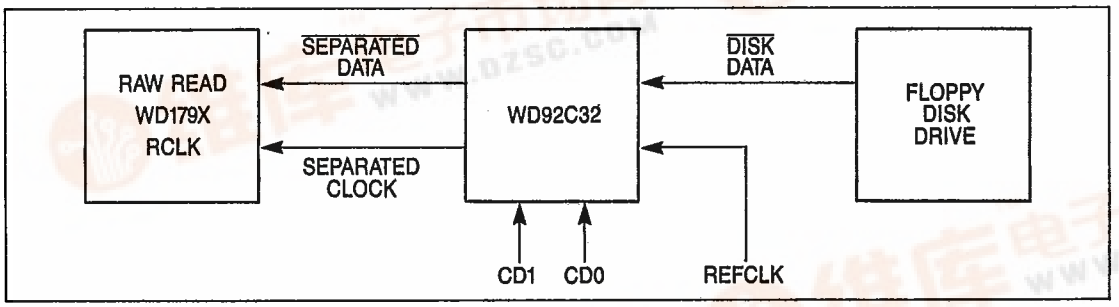


FIGURE 1. TYPICAL SYSTEM WITH WD92C32 AS DATA SEPARATOR

PIN DESCRIPTIONS

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D/P PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	$\overline{\text{DSKD}}$	$\overline{\text{DISK DATA}}$	I	Data input signal from the floppy disk drive containing both clock and data information.
2	SEPCLK	SEPARATED CLOCK	O	Clock signal output recovered from the disk drive serial bit stream. Sometimes called RCLK.
3	REFCLK	REFERENCE CLOCK	I	Reference clock input from crystal oscillator.
4	V_{SS}	GROUND		Ground.
5, 6	CD0, CD1	CLOCK DIVISOR		CD0 and CD1 control the internal clock divider circuit. The internal clock is a submultiple of the REFCLK according to the following: CD1 CD0 DIVISOR 0 0 1 0 1 2 1 0 4 1 1 8
7	$\overline{\text{SEPD}}$	$\overline{\text{SEPARATED DATA}}$	O	Sometimes called RDATA, this is still the encoded serial bit stream which has been re-synchronized to the phase of recovered clock.
8	V_{CC}	POWER SUPPLY		+15V power supply.

ARCHITECTURE

The WD92C32 provides seven major functions: Digital Controlled Oscillator, Phase Detection, Transient Response State Filtering, Steady State Frequency Filtering, Data Synchronization, RDATA Resynchronization, and Clock Generation.

Digital Controlled Oscillator

The Digital Controlled Oscillator (DCO), is made up of a Variable Length Ring Shift Register and a finite State Machine. The State Machine controls the time-averaged steady state frequency. The Variable Length Ring Shift Register rotates a single "1" around a loop, passing through the last shift state causes the separated clock (RCLK) to toggle. The last state is determined by the steady state frequency. Any instantaneous phase corrections are made by the filtering State Machines.

Phase Detection

The ideal Phase Detection is accomplished by comparing the location of the "1" in the DCO Shift Register upon the occurrence of an encoded data flux transition. Each rotation of the "1" represents a phase window used for detection. The deviation from the ideal is a discrete measure of the phase error and the detection pulse causing filter execution. Each of the two filtering State Machines decodes the various amounts of error as possible conditionals used during execution.

Transient Response State Filtering

This State Machine functions to provide instantaneous phase corrections to RCLK upon occurrence of a pulse. The magnitude of the correction is dependent on the magnitude of the detected phase error. This value is summed with the current phase of the steady state frequency from the DCO and then output as RCLK.

Steady State Frequency Filtering

This State Machine functions to determine if the DCO frequency should be incremented or decremented. Upon occurrence of a pulse it calculates a trend in slew rate and, if the probability of a correctly identified trend is high and of sufficient magnitude, the DCO is flagged to change. Periodic phase corrections control the rate of detection and guarantees zero steady state phase error in the output signal as a 2nd order, type 2, PLL must.

Data Synchronization

This logic contains the sampling resolvers converting the asynchronous raw data stream to the synchronous digital machine. It then creates a single pulse, of one sample clock period, used by the DDS algorithm. The initial detection of the flux transition is edge sensitive.

RDATA Resynchronization

This logic generates an output pulse of fixed duration with a known phase relationship to SEPCLK. Effectively, incoming pulses are latched and then held until

a fixed one clock delay beyond the next edge of RCLK. At this time, the logic generates an output phase whose duration is two clock cycles.

Clock Generation

This circuit will divide REFCLK into submultiples according to the clock divisor inputs. It is this internal clock rate that drives the DDS algorithm determining sampling, delays, and pulse durations. The clock dividers are chosen for different data rates such that this internal SCLK is always 32X the desired data rate. The following table presents clock divider selection.

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CLOCK DIVIDER SELECTION

DRIVE DENSITY	DATA RATE	CODE	REFCLK	CD1	CD0
8 DD 5¼ QD 3½ QD	500 K	MFM	16 MHz	0	0
8 SD	250 K	FM	16 MHz	0	1 Select either
	250 K	FM	8 MHz	0	0 one
5¼ DD 3½ DD	250 K 250 K	MFM MFM	16 MHz 8 MHz	0 0	1 Select either 0 one
5¼ SD	125 K	FM	16 MHz	1	0 Select
3½ SD	125 K	FM	8 MHz	0	1 any
	125 K	FM	4 MHz	0	0 one

Figure 2 illustrates the WD92C32 simplified block diagram.

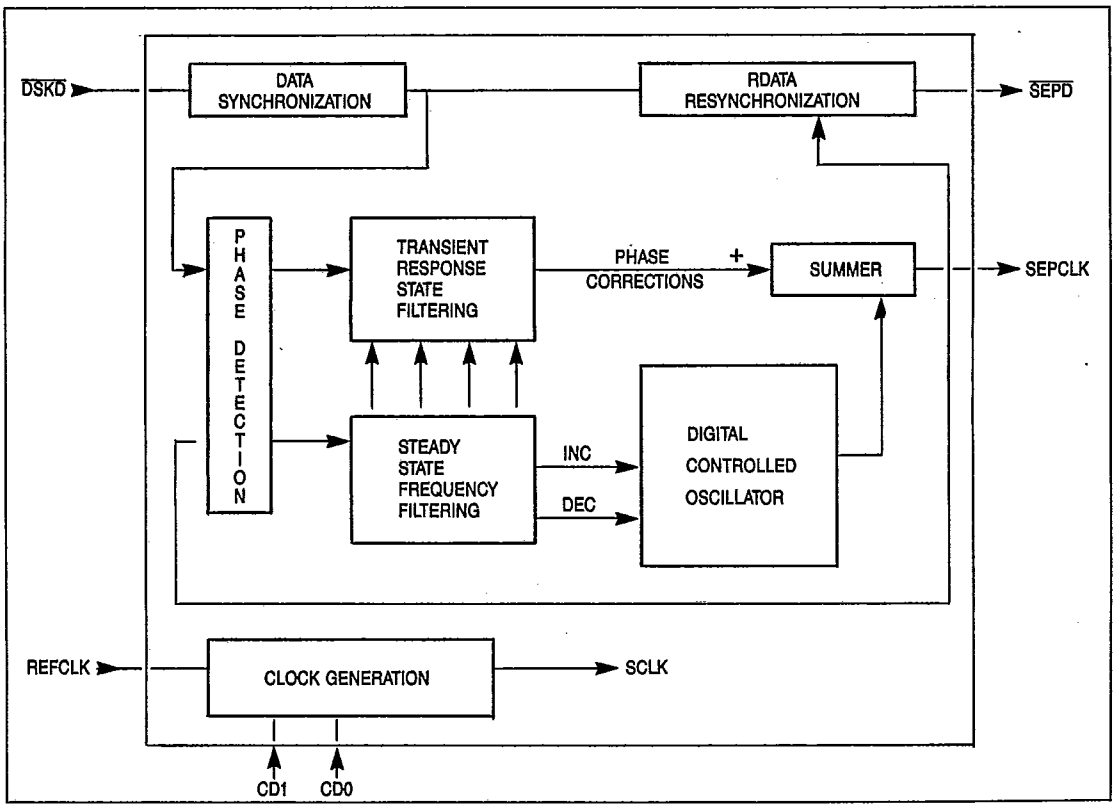

FIGURE 2. WD92C32 SIMPLIFIED BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C (32°F) to 70°F (158°F)
Storage Temperature ..... −55°C (−67°F) to +125°C (257°F)
Voltage on any pin with respect to ground ..... −0.3V to V_{CC} +0.3V
Voltage with respect to ground ..... 0.5V to +7.0V

NOTE

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Operating Characteristics.

DC Operating Characteristics
T_A = 0°C (32°F) to 70°C (158°F); V_{CC} = ±5V ±0.5V

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
V_{CC}	+5V Power Supply	4.5	5.5	V	
V_{IL}	Input Low Voltage		0.8	V	
V_{IH}	Input High Voltage	2.0		V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			I_{OH} = −100μA
I_{IL}	Input Leakage Current		±10	μA	
I_{DD}	V_{DD} Supply Current		7.0	mA	16 MHz Clock

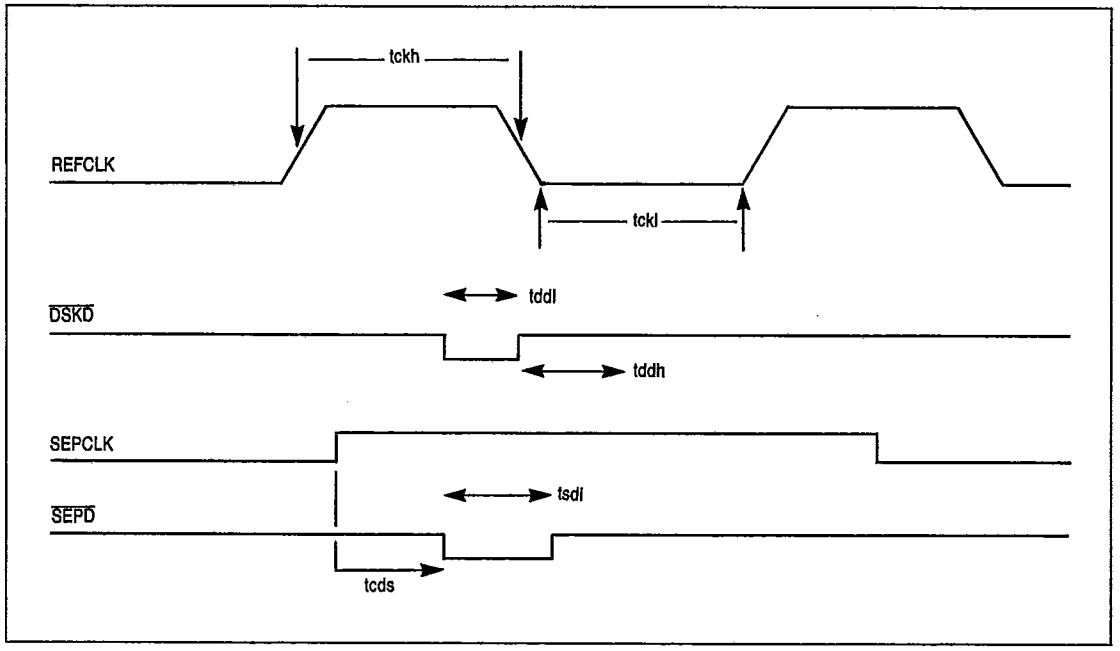

FIGURE 3. AC OPERATING CHARACTERISTICS

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AC Operating Characteristics
T_A = 0°C (32°F) to 70°C (158°F); V_{CC} = +5V ±0.5V

SYMBOL	CHARACTERISTICS	MIN	TYP	MAX	UNITS	CONDITIONS
Freq	REFCLK Frequency			16.7	MHz	
tckh	REFCLK High Time	25			ns	
tckl	REFCLK Low Time	25			ns	
tddl	$\overline{\text{DSKD}}$-Low Time	50			ns	
tddh	$\overline{\text{DSKD}}$-High Time	100			ns	
tsdl	$\overline{\text{SEPD}}$-Low Time		125		16 MHz	
			250		8 MHz	
			500		4 MHz	
tcds	SEPCLK to $\overline{\text{SEPD}}$-Low	0.8			tcyc	REFCLK

PERFORMANCE CHARACTERISTICS

Capture Range:	±8%
Lock Range:	+18%, −15%
Frequency Tracking:	±6% of nom (DCO bandwidth of 12%)
Lock Up Response Time:	Four byte times maximum 00 Hex Sync over frequency delta of 6%, data within DCO BW.
Error Rate Window Tolerance:	60% maximum distribution of gaussian data for < 10E−9 errors, data within DCO BW.
Peak Shift Tolerance:	±500 nsec, 250 Kb/s, data within DCO BW. ±250 nsec, 500 Kb/s, data within DCO BW.
Phase Detection Window Margin:	94% minimum, data within DCO BW.