1.0 INTRODUCTION

1.1 DESCRIPTION

The Floppy Disk Controller (FDC) portion of the WD76C20 is a VLSI Super Cell that provides all needed functions between the host processor peripheral bus and the cable connector to the floppy disk drive. This provides a total solution to floppy subsystem control. The FDC has a software transparent power down mode feature which broadens its use in laptop and portable systems.

On the disk drive interface, the FDC includes data separation and write precompensation in addition to the usual formatting, encoding/decoding, stepper motor control and status sensing functions. All inputs are TTL compatible, and outputs are high-current, open-drain drivers meeting the ANSI specification of 48 mA.

The host interface has been designed to support up to 12 MHz bus speeds without the use of wait states. Additionally, input strobes are Schmitt Triggers. The data bus drive capability is12 mA IOL, and 5 mA IOH, allowing, in most applications, direct interconnection to bus structures without the use of buffers or transceivers. For PC and PC /AT applications, qualification of interrupt request and DMA request is provided.

Traditionally, data rate selection, drive selection, and motor control have been output ports of the host processor architecture. In the PC AT, these functions were latched into registers addressed within the I/O mapping of the system. These registers, Operations and Control, are incorporated into the FDC.

All clock generation necessary for the floppy disk subsystem is included in the FDC portion of the WD76C20. A 16 MHz crystal oscillator circuit provides the necessary signals for internal timing when external clocks are unavailable. The 16 MHz signal handles all standard data rates (500 and 250 Kbits/sec) used in PC/AT designs, and a non-standard data rate (300 Kbits/sec.). If neither the board space nor the 16 MHz TTL clock is available, FCLK1/FX1 can be driven with a 16 MHz TTL level clock, and FCLK2 with a 9.6 MHz TTL clock. This will handle standard data rates (500, 250, and 125 Kbits/sec.), and a non-standard data rate (300 Kbits/sec.).

The Real Time Clock plus SRAM provides all the functionality of a Motorola MC146818A usable in the PC/AT environment. It provides a complete time-of-day clock with alarm, calendar, periodic interrupt generator, and 114 bytes of low power static RAM.

The Bus Interface Logic (BIL) section of the WD76C20 provides the DB7 multiplexing necessary to implement a PC/AT compatible IDE drive interface and the Chip Select Logic section incorporates miscellaneous chip selects and control strobes necessary for the implementation of a PC/AT compatible system. The Suspend/Resume section supports the chip set power down mode by providing a 14.318 MHz clock during Resume and a 32.768 KHz clock during Suspend mode. An external DRAM refresh signal is also provided by the Suspend/Resume section to support the chip set.

The WD76C20 is designed with Western Digital's 1.25 micron CMOS process. It is available in 84-lead PLCC and PQFP packages.

1.2 FEATURES

- 84-pin PLCC and PQFP packages
- 5V only supply requirement
- 3.0V battery backup supply for the RTC and 114 byte SRAM
- Implemented in a low-power, high performance CMOS technology
- Floppy Disk Controller (FDC) software transparent power-down mode with low standby ICC current. FDC features:
  - 256 tracks support
  - 100% software compatible with NEC 765A
  - Integrated high performance DPLL data separator:
    - 125, 250, 300, 500 Kbits/sec and 1 MB/sec data rates
    - Option to select 150 Kb/sec FM and 300 KB/sec MFM data rates only
    - Automatic Write Precompensation:
    - Defeat option
    - Inner track value of 125 or 187 ns pin selectable
  - On chip clock generation:
    - 2 TTL clock inputs, or
    - Single 16 or 32 MHz crystal circuit and one TTL clock input
  - Host interface read/write accesses compatible with 80286 microprocessors at speeds up to 12 MHz with 0 wait states
  - Direct floppy disk drive interface - no buffers needed
    - 48 mA sink output drivers
    - Schmitt Trigger input line receivers
  - FDC direct PC XT/AT interface compatibility
    - Floppy Control and Operations Registers on chip
    - In PC/AT mode, provides required signal qualification to DMA channel
    - IBM BIOS compatible
    - Dual-speed spindle drive support
  - PS/2 type drive support
- Real Time Clock (RTC) features:
  - Software compatible with Motorola MC146818A.
  - Internal time base and oscillator circuitry
  - Counts seconds, minutes and hours
  - Counts days of the week, date, month, and year
  - Time base input for 32.768 KHz square wave
  - Time base oscillator for parallel resonant crystals
  - Binary or BCD representation of time, calendar, and alarm
  - 12 or 24 hour clock with AM and PM in 12-hour mode
  - Daylight savings time option
  - Automatic leap year compensation
  - Interfaced with sofware as 128 RAM locations
  - 114 bytes of general purpose RAM
  - Status bit indicates data integrity
  - Bus compatible interrupt signals (IRQ)
  - Three interrupts are separately software maskable and testable:
    - Time-of-day alarm, once-per-second to once-per-day
    - Periodic interrupt rates from 122 us to 500 ms
    - End-of-clock update cycle

2.0 ARCHITECTURE

This section contains a general architectural overview of the WD76C20 which provides a cost-effective, power-efficient solution to PC systems design problems, especially those relating to "laptop" devices. The section also illustrates the WD76C20's packaging and includes a listing of pin numbers with associated signal mnemonics and functions.

2.1 FUNCTIONAL COMPONENTS

Referring to Figure 2-1, the WD76C20 has three principal functional boundaries. First, it exchanges control signals with the WD76C10 System Controller. Then, under control of the WD76C10, it exchanges data and qualified operational/status information with the host via the system's AT Bus. Finally, on the media side, it provides complete control and data read/write services for from one to four floppy disk units.

Internally, the WD76C20 has the following functional components:

- Chip Select Logic
- Bus Interface Logic
- Floppy Disk Controller

Additional supporting components are:

- Real Time Clock
- 114-byte SRAM (affiliated with the Real Time Clock)
- Suspend/Resume Logic

These functional components are briefly described in the following sections with detailed descriptions provided in Section 3. Signals mentioned in the following narratives are listed and described in Tables 2-1 and 2-2 later in this section.

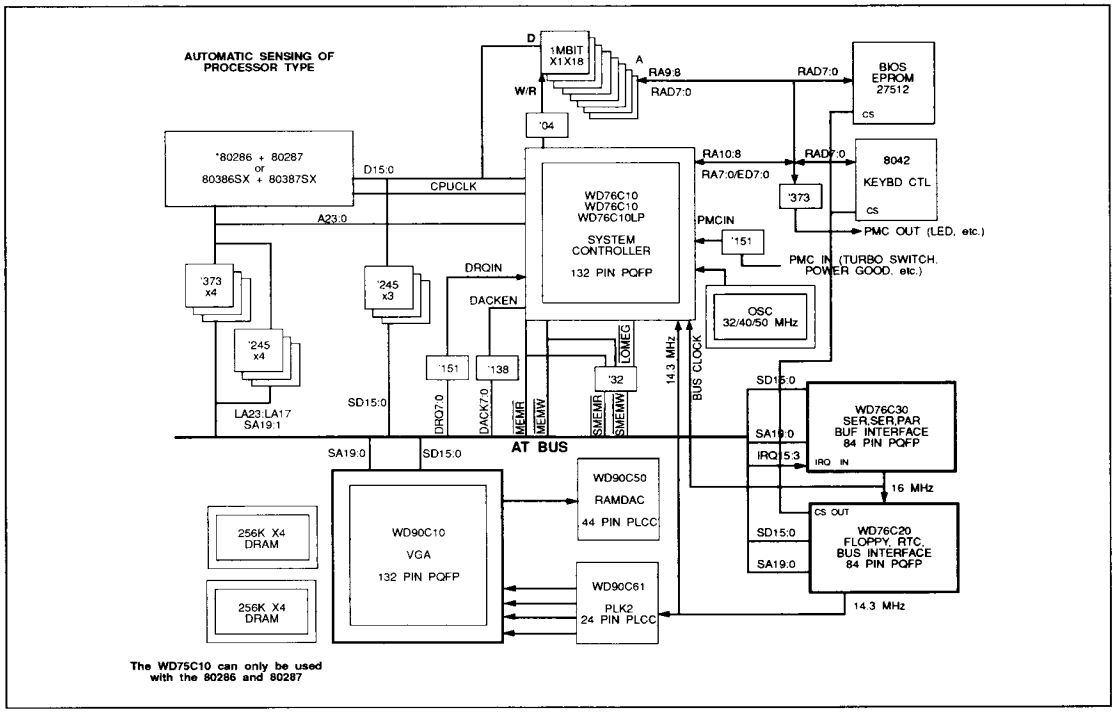


FIGURE 2-1. SYSTEM LEVEL FUNCTIONAL BLOCK DIAGRAM

2.1.1 Chip Select Logic

The Chip Select Logic (CSL) component of the WD76C20 provides the decoding needed both for selecting chip functions within the WD76C20 and on the PC/AT motherboard as well. It gets the DPL, DPH, and RA8-RA10 signals from the WD76C10 Systems Controller and outputs appropriately decoded chip select signals (detailed in Section 3.) Overall control of the decoding processes is effected with the CSEN and DACKEN signals from the WD76C10. CSEN enables the decoded output, while DACKEN causes the CSL to ignore the inputs from the WD76C10. Optionally, the chip select inputs (CSEN, DPH, DPL, RA10, RA9, RA8) can be latched by dropping the BALE from a logic 1 to a logic 0. These latches are transparent when BALE is held high or left unconnected.

2.1.2 Bus Interface Logic

The Bus Interface Logic (BIL) component of the WD76C20 controls the buffering of bits D0-D7 between the system's AT Bus and any WD76C20 internal source/destination 8-bit storage cell via the internal bus. It gets the IOR and IOW signals from the WD76C10, and with the appropriate chip selects from the CSL, the BIL parallel-passes D0-D7 from the AT Bus to an internal WD76C20 cell, or vice-versa. The internal cells are:

- The Control, Master Status, Data, or Operation Registers in the Floppy Disk Controller
- The 128 registers in the SRAM affiliated with the Real Time Clock.

The BIL also provides a controlled bidirectional path for bit D7 between the AT Bus and the IDE Drive Port.

2.1.3 Floppy Disk Controller

765A Core - The core of the 765A floppy disk controller has been maintained so the micro-sequencer is functionally equivalent and all commands will execute identically, hence software compatibility is assured. The floppy control state machine on the front-end is also functionally equivalent. The micro-sequencer and control state machine operate at 8 times the selected bit data rate in MFM and 16 times the bit data rate in FM.

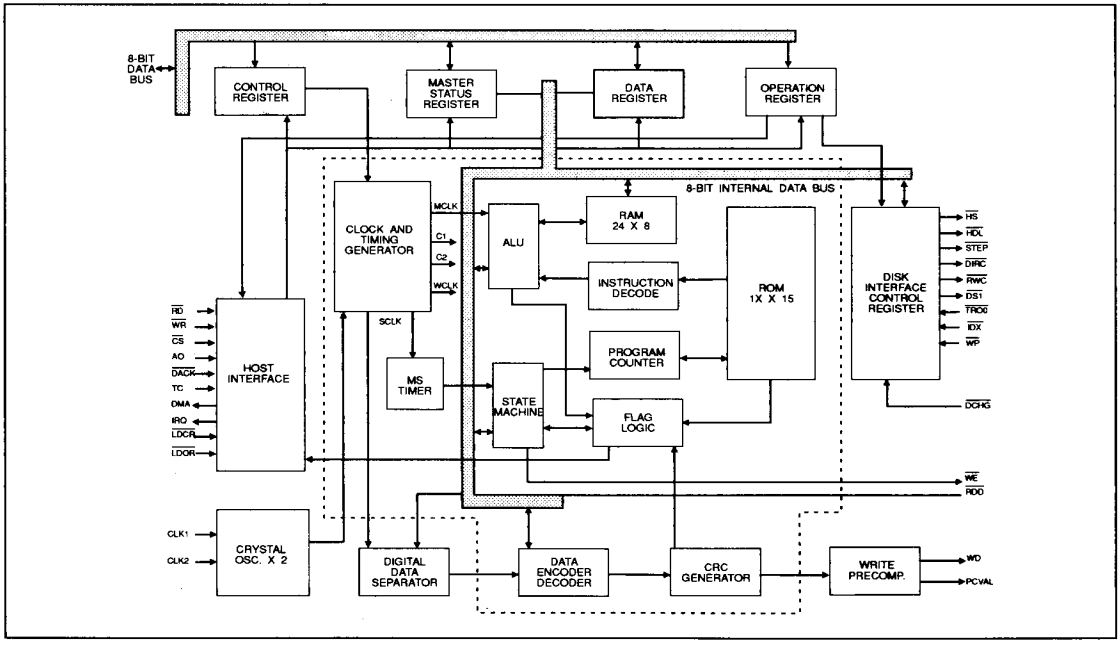


FIGURE 2-2. FLOPPY DISK CONTROLLER BLOCK DIAGRAM

Host Interface - The host access signals are identical to 765A floppy disk controller, but timings have been enhanced. The FDC has 8 internal registers.

The 8-bit main status register contains status information of the FDC and may be accessed any time. Another 4 status registers under system control also give various status and error information. The Control Register provides support logic that latches the two LSB's used to select the desired data rate that controls internal clock generation. Bit 2 of this register is also used to disable the write precompensation logic. The Operations Register provides all the control signals required to select the drive and the spindle motor. In PC/AT mode, Interrupt Request and DMA Request are tristated and qualified by DMA Enable, internally provided by the Operations Register. The data bus is designed to handle 20 LSTTL loading.

Automatic Power Down Mode - In this mode, the FDC powers down all circuitry except for the Data Register, the Operations Register, the Control Register, the Master Status Register and the I/O path leading to and from the data bus. Since the crystal oscillator controller circuitry and all non-essential linear circuitry is turned off, the controller will draw very low current. The FDC can return from power down mode by simply polling the Master Status Register, after which the crystal oscillator will turn on, along with the other circuitry.

Data Separator - The FDC incorporates the patent pending digital phase lock loop used in the WD92C32 product. The sample clock rate, SCLK, must be 32 times the data rate.

Write Precompensation - The FDC maintains the standard first level algorithm to determine when write precompensation should be applied. These EARLY and LATE signals are used internally to select the appropriate delay in the Write Data pulse stream. The encoded write data signal is synchronized to the 32 MHz clock, if this is the frequency on pin FCLK1, and clocked through a shift register, FX1. Signals EARLY, NOM, and LATE determine the amount of delay through the shift register before a multiplexer gates the chosen bit to the output. The output data pulse width has 25% duty cycle, i.e. 1/4 of the bit cell period, also equal to 1/2 the WCLK period.

With PCVAL pin = 1, all data will be precompensated by +/- 125 ns regardless of track number and data rate, but only for MFM encoding (no write precomp for FM). If PCVAL = 0, and if a track inside number 28 is accessed, then +/- 187 ns of precomp will be generated. For frequencies other than 32 MHz on FX1, these precomp values will be 2 and 3 SCLK clock cycles respectively.

When a non-standard data rate using FCLK2 is chosen, the precompensation logic is run from this frequency. In this case, the PCVAL function is disabled. Hence precomp values will always be 2 clock cycles. For 9.6 MHz this value is +/- 208 ns. The write precomp can be disabled by the use of bit 2 of Control register for PC AT. With no write precomp, the PCVAL input to the chip is ignored.

Drive Interface - The FDC no longer supports certain pin functions provided for in the 765 predecessor. The output RW/SEEK is used in the 765 based subsystem as a multiplexer select line to allow a pin to have 2 functions depending on whether a read, write or seek type command are under execution. This signal is no longer available externally, but is used within the WD76C20 to assure that no improper pin functionality occurs.

The LCT function has been renamed $\overline{\text{RWC}}$ and resides on a pin of its own with slightly altered active conditions and in PC/AT mode is RPM. DIRC is the only function on that pin and is enabled only during seeks as a power conservation measure.

$\overline{\text{STEP}}$ is also only enabled during seeks and a fault rest (FR) is no longer needed since FLT, fault detects, are not sensed. FLT status, status register #3, bit 7, will always be a logic 0 Track zero, /TR00, status is only sensed during seeks as well.

TS, two-sided, drive status is no longer supported, and status register #3, bits 6 and 3 will both now reflect Write Protect status. The FDC device assumes the drive is ready all the time as DRDY signal is set to logic = 1 internal. This will still result in a FIRQ. This action is acknowledged as a change in status and demands a Sense Interrupt Status command execution in order to clear the FIRQ. Also note that the signals MFM, RDW, WCK and VCO are no longer necessary since all logic associated with these is wholly contained within the FDC.

2.1.4 Clock Generation

This logical block provides all the clocks needed by the FDC, including SCLK (Sampling Clock), WCLK (Write Clock) and MCLK (Master Clock). SCLK is the clock which drives the digital phase lock loop data separator during data recovery. This clock frequency is always 32 times the selected data rate, and its frequency is directly the frequency of the signals on FX1 (FCLK1) and FCLK2, whether or not standard data rates are being used (see Table 1). The use of the 32 MHz oscillator output FX1 is optional if the 1 Mb/sec data rate is not required. If the oscillator is not used, either a 32 MHz or a 16 MHz TTL clock should be applied at FCLK1 (FX1).

WCLK is used by the encoder logic to place MFM or FM on the serial Write Data stream to the disk. WCLK always has a frequency 2 times the selected data rate.

MCLK is used by the microsequencer. MCLK and $\overline{MCLK}$ clock all latches in a 2 phase scheme. One micro-instruction cycle is 4 MCLK cycles. MCLK has a frequency equal to 8 times the selected MFM data rate or 16 times the FM data rate.

In the power down mode, the crystal oscillator and all the clock circuitry is turned off. The FDC will turn on the crystal oscillator, which will in turn activate all the clock circuitry on the chip once the device returns from power down mode.

FX1 FCLK1	FCLK2	SCLK	
		STANDARD	NON STANDARD
16.0 MHz TTL	9.6 MHz TTL	16.0 MHz	9.6 MHz
16.0 MHz TTL	TIED LOW	16.0 MHz	DISABLED
32.0 MHz XTAL[1]	9.6 MHz TTL	32.0 MHz	9.6 MHz
32.0 MHz XTAL[1]	TIED LOW	32.0 MHz	DISABLED

TABLE 2-1. FDC SAMPLING CLOCK (SCLK) GENERATION

[1] Can be either a crystal or 32 MHz TTL level clock

DATA RATE	CODE	SCLK	MCLK	WCLK
1Mb/s	MFM	32.0 MHz	8.0 MHz	2.0 MHz
500 Kb/s	MFM	16.0 MHz	4.0 MHz	1.0 MHz
500 Kb/s	FM	16.0 MHz	8.0 MHz	1.0 MHz
250 Kb/s	FM	9.0 MHz	4.0 MHz	500 KHz
250 Kb/s	MFM	8.0 MHz	2.0 MHz	500 KHz
300 Kb/s	MFM	9.6 Mhz	2.4 Mhz	600 Khz

TABLE 2-2. FDC MCLK AND WCLK GENERATION

2.1.5 Real Time Clock and SRAM

The Real Time Clock (RTC) component of the 76C20, in conjunction with the 128 byte-register file, provides calendar (day-of-week, day-of-month, month, and year) and clock (hours, minutes, and seconds) information, along with clocked alarms and a periodic interrupt. Referring to Figure 2-3, ten SRAM data registers contain all the clock/time/alarm information with the RTC crystal-controlled oscillator and frequency divider providing the appropriate clock "ticks" that keep them current. Control and status information for the RTC is contained in Registers A-D of the SRAM (detailed in Section 3). Remaining SRAM registers (114) are user-available.

Read and/or write access to the SRAM (control/status, calendar/clock/alarm, and general purpose registers) is through the RTC bus interface. This interface gets signals from the 76C20 Bus Interface and Chip Select Logic functions and appropriately buffers bits D0-D7 between the 76C20 internal bus and the RTC internal bus accessing the SRAM. Calendar/clock/alarm information is processed through Update Logic that:

- Increments calendar/clock counts based on "ticks" received from the Frequency Divider,
- Attends to Daylight/Standard Time and Leap Year adjustments, and
- Formats/deformats the information as straight binary or binary coded decimal data, as selected.

Input power to the RTC component is from the VBAT pin. Switching from System VDD to battery power is accomplished through two diodes as seen in Figure 2-3a.

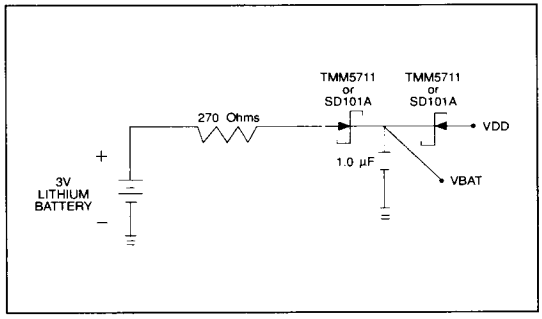


FIGURE 2-3A. VBAT EXTERNAL SUPPORT

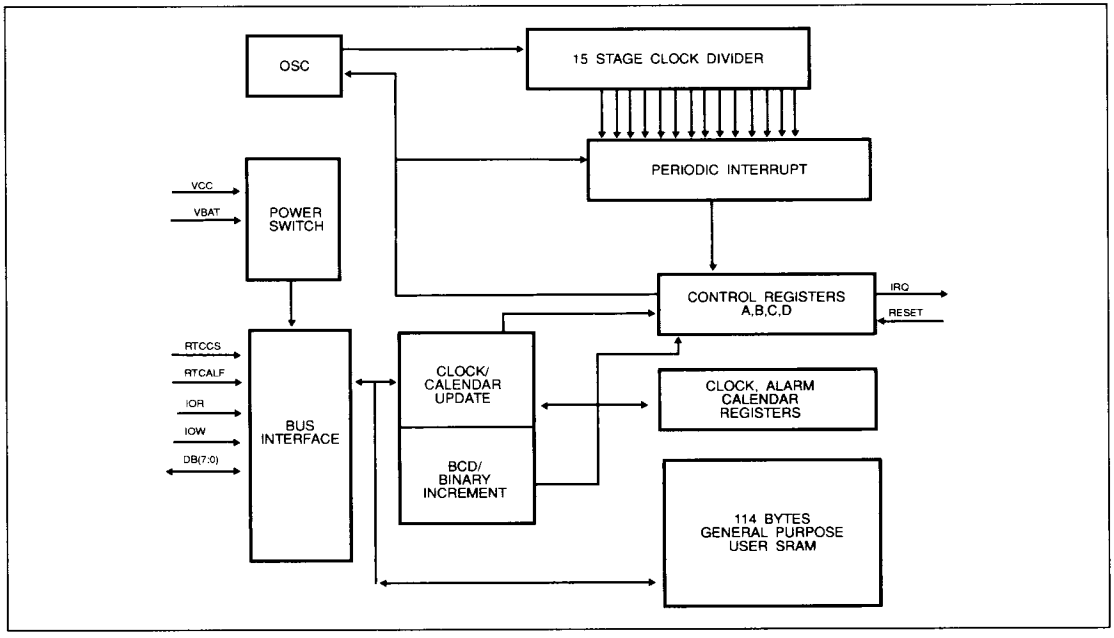


FIGURE 2-3. RTC BLOCK DIAGRAM

Time Base Oscillator Circuit - The oscillator used to provide the time base for the RTC requires the external circuit shown in Figure 2-4 with the values listed in Table 2-3. The crystal to be used in parallel with the on-chip oscillator should be an AT-cut crystal, with a 32.768 KHz resonant frequency as described in Figure 2-5 and Table 2-3. When in battery backup mode, this circuit is still active, and providing the rest of the RTC with a valid time base.

Power Switch - This functional block is used to detect when the system power is shutting down and the RTC needs to go into battery backup mode. In the event of a full chip power down without a battery backup, the VRT bit of register D will be reset to zero, indicating that the contents of the SRAM and RTC operational registers are not guaranteed. In order to reset the bit, register D must be read after a full power up.

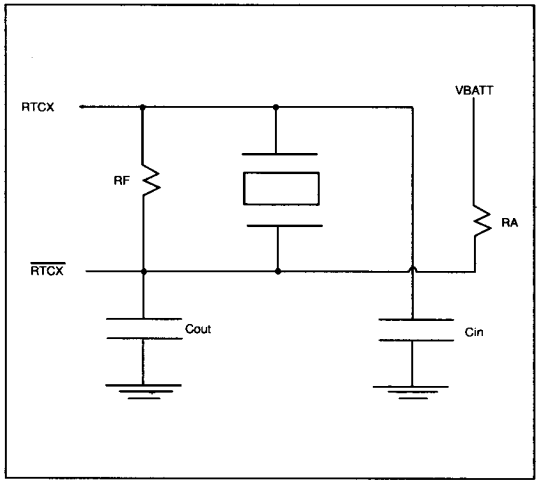


FIGURE 2-4. RTC CRYSTAL OSCILLATOR CONNECTIONS

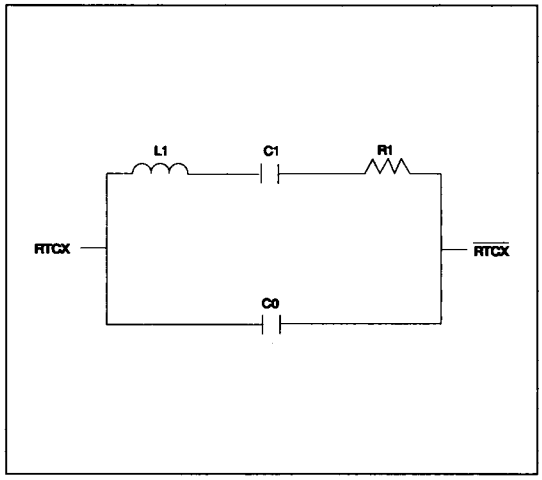


FIGURE 2-5. RTC CRYSTAL PARAMETERS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
R1	Crystal Motional Resistance		40	K Ohm
C0	Crystal Shunt Capacitance		1.7	pF
C1	Crystal Motional Capacitance		0.0035	pF
Q	Crystal Quality Factor	50		K
Clin	Crystal Circuit Input Capacitance	30	± 5%	pF
Cout	Crystal Circuit Output Capacitance	22	± 5%	pF
RA	Crystal Circuit Drive Level Resistor	340	± 1%	K Ohm
Rf	Crystal Circuit Feedback Resistor	15	22	M Ohm

TABLE 2-3. RTC CRYSTAL CIRCUIT SPECIFICATION

Bus Interface - The RTC Bus Interface block is used to access the internal bus for the WD76C20. Protocol is maintained between the BIL block (Bus Interface Logic) and the RTC Bus Interface. The BIL block generates the RD and WR strobes, and the CS signals are decoded from the external bus by the Chip Select Logic.

Clock Divider - This functional block uses clock divider logic to divide the 32.768 KHz time base into a 1 Hz signal used by the timekeeping blocks. As a side duty, it provides the periodic interrupt block with access to all stages of the division.

Periodic Interrupt - This functional block has access to the various stages of the Clock Divider. With these signals, and under the direction of register A, an RTCIRQ pulse can be periodically generated for the processor from once every 122 µS to once every 500 ms. The Periodic Interrupt function is enabled by the PIE bit in register B.

BCD/Binary Increment & Clock/Calendar Update - This dual purpose logic block is used to increment and update the 10 timing registers and to check for the existence of an alarm condition. Several register bits are used to control this block to prevent contention between a processor access to the information registers and the occurrence of an update cycle.

2.1.6 Suspend/Resume Logic

This functional block is used in conjunction with the RTC time base to provide a 14.318 MHz clock output to the WD76C10, which will switch to a 32.768 KHz clock during the chip set low power suspend mode. The Suspend/Resume block also provides the external DRAM refresh signal, PDREF, that will pulse active low once every 15.26 µS. This block also supports a latched signal that causes CSSERA, CSSERB and CSPAR0 to remain low during Suspend mode, signaling the WD76C30 to disable the 48 MHz crystal.

2.2 PINOUT

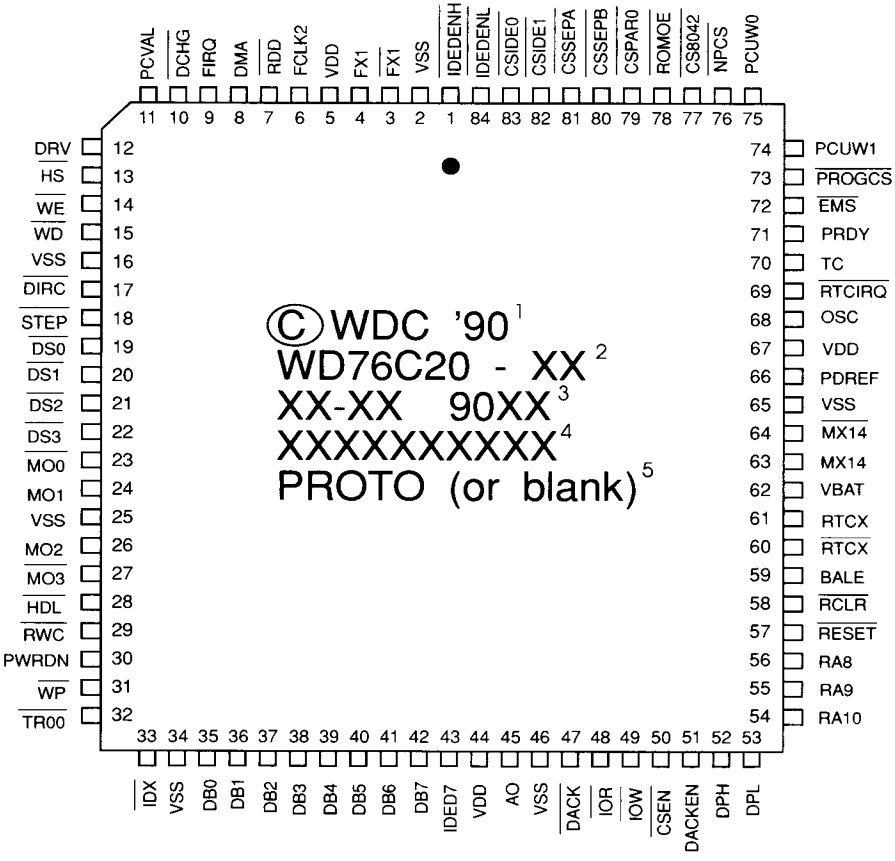
Figure 2-6 illustrates the signal names and pin locations on the 84-pin PLCC/PQFP WD76C20 package. Table 2-4a lists the signal names alphabetically and Table 2-4b lists the signal names in pin number order. Table 2-5 lists the signal names and descriptions, grouped by function.

NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN
A0	45	DS1	20	MO2	26	ROMOE	78
BALE	59	DS2	21	MO3	27	RPM/RWC	29
CSEN	50	DS3	22	MX14	63	RTCIRQ	69
CSIDE0	83	EMS	72	MX14	64	RTCX	60
CSIDE1	82	FIRQ	9	NPCS	76	RTCX	61
CSPAR0	79	FCLK1/FX1	4	OSC	68	RWC/RPM	29
CSSERB	80	FCLK2	6	PCUW1	74	STEP	18
CSSERA	81	FX1	3	PCUW0	75	TC	70
CS8042	77	FX1/FCLK1	4	PCVAL	11	TR00	32
DACK	47	HDL	28	PDREF	66	VBAT	62
DACKEN	51	HS	13	PRDY	71	VDD	5,44,67
DB0-DB7	35-42	IDEDENH	1	PROGCS	73	VSS	2,16,25,34,46,65
DCHG	10	IDEDENL	84	PWRDN	30	WD	15
DIRC	17	IDED7	43	RA8	56	WE	14
DMA	8	IDX	33	RA9	55	WP	31
DPH	52	IOR	48	RA10	54		
DPL	53	IOW	49	RCLR	58		
DRV/PS2	12	MO0	23	RDD	7		
DS0	19	MO1	24	RESET	57		

TABLE 2-4A. PIN ASSIGNMENTS (ALPHABETIC ORDER)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
1	IDEDENH	22	DS3	43	IDED7	64	MX14
2	VSS	23	MO0	44	VDD	65	VSS
3	FX1	24	MO1	45	A0	66	PDREF
4	FX1	25	VSS	46	VSS	67	VDD
5	VDD	26	MO2	47	DACK	68	OSC
6	FCLK2	27	MO3	48	IOR	69	RTCIRQ
7	RDD	28	HDL	49	IOW	70	TC
8	DMA	29	RWC	50	CSEN	71	PRDY
9	FIRQ	30	PWRDN	51	DACKEN	72	EMS
10	DCHG	31	WP	52	DPH	73	PROGCS
11	PCVAL	32	TR00	53	DPL	74	PCUW1
12	DRV/PS2	33	IDX	54	RA10	75	PCUW0
13	HS	34	VSS	55	RA9	76	NPCS
14	WE	35	DB0	56	RA8	77	CS8042
15	WD	36	DB1	57	RESET	78	ROMOE
16	VSS	37	DB2	58	RCLR	79	CSPAR0
17	DIRC	38	DB3	59	BALE	80	CSSEPB
18	STEP	39	DB4	60	RTCX	81	CSSEPA
19	DS0	40	DB5	61	RTCX	82	CSIDE1
20	DS1	41	DB6	62	VBAT	83	CSIDE0
21	DS2	42	DB7	63	MX14	84	IDEDENL

TABLE 2-4B. PIN ASSIGNMENTS (NUMERIC ORDER)



1 Copyright Information

2 Part Number - Package Type
XX = UU (Low Profile 84 Lead PQFP
LU (Standard 84 Lead PQFP)
JU (PLCC)
GU (CLCC)

3 ROM Version-Test Bin Date
XX-XX = 06 (Current ROM Version)
02 (Current Passing Test Bin)

4 In-House Control Code

5 Proto-Type Indicator
PROTO indicates unreleased device

FIGURE 2-6. 84-PIN PLCC/PQFP PIN ASSIGNMENTS

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		Integrated Drive Electronics (IDE)		
1	$\overline{\text{IDEDENH}}$	IDE High Byte Drive Enable	O	CMOS level output goes active low to enable the IDE Drive Interface Bus transceivers for the high byte of of the 16-bit interface. The signal is used with the $\overline{\text{CSIDE0}}$ card select oupt signal to the IDE drive only during 16-bit IDE data transfers.
43	IDED7	IDE Data Bit 7	I/O	TTL level I/O providing a data path for bit 7 between the Host and the IDE drive interface. IDED7 is an output, passing data to the IDE drive from DB7 of the Host data bus whenever an $\overline{\text{IOW}}$ to the IDE drive interface is detected. IDED7 is an input, passing data from the IDE drive to DB7 of the Host data bus whenever an $\overline{\text{IOR}}$ of the IDE drive interface is detected, except when reading from address 3F7H. During an $\overline{\text{IOR}}$ of 3F7H, the floppy DCHG status is output on the Host data bus pin DB7.
82	$\overline{\text{CSIDE1}}$	IDE Card Selected Aux. Registers	O	CMOS level output is used by the Host to address and communicate with the IDE drive auxiliary registers. Host activates the signal through a decode in the CSL logic block, while at the same time asserting $\overline{\text{IDEDENL}}$.
83	$\overline{\text{CSIDE0}}$	IDE Card Selected Registers 0-7	O	CMOS level output is used by the Host to address and communicate with the IDE drive on the I/O channel. The Host activates the signal through a decode in the CSL logic block, while at the same time asserting $\overline{\text{IDEDENL}}$ or both $\overline{\text{IDEDENL}}$ and $\overline{\text{IDEDENH}}$.
84	$\overline{\text{IDEDENL}}$	IDE Low Byte Drive Enable	O	CMOS level output goes active low to enable the IDE drive interface bus transceivers for the high byte of the 16-bit Interface. The signal is used with the CSIDE0 card select output signal to the IDE drive only during 16-bit IDE data transfers.
		Host Interface		
8	DMA	FDC DMA Request	O	DMA request for byte transfers of data. In PC/AT mode, this pin is tristated, enabled by DMAEN signal from the Operations Register.
45	AO	BIL Address Line	I	Address line selecting data (=1) or status (=0) information for the FDC. A0 = logic 0 during $\overline{\text{IOW}}$ is illegal except when putting the FDC into sleep mode.
47	$\overline{\text{DACK}}$	FDC DMA Acknowledge	I	Used by DMA controller to transfer data from FDC onto the bus. Logical equivalent to $\overline{\text{FDCS}}$ and A0=1. In PCAT mode, this signal is qualified by DMAEN from the Operations Register.

TABLE 2-5. PIN DESCRIPTIONS

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		Host Interface, Continued		
48	$\overline{IOR}$	BIL Input/Output Read	I	Read enable allowing data or status information to be transferred onto data bus by the WD76C20.
49	$\overline{IOW}$	BIL Input/Output Write	I	Write enable latching data from the bus into sub-system buffer registers.
57	$\overline{RESET}$	Chip Reset	I	TTL input resets the WD76C20 with the exception of the normal timekeeping operations which will remain uninterrupted. Resets all device outputs. Resets FDC controller, placing microsequencer in idle, and puts FDC in base mode, not PC/AT mode.
		Data To/From Floppy - Floppy Control		
3	$\overline{FX1}$	FDC XTAL Output #1	I/O	This pin is an oscillator drive output for a 32 MHz resonant crystal. FX1 should be left floating if a TTL level clock is used at pin FX1.
4	FX1	FDC XTAL Input #1	I	XTAL oscillator input requiring 32 MHz resonant crystal. This oscillator is used for all standard data rates, and may be driven with either a 32 MHz or 16 MHz TTL level signal instead of using the 32 MHz or 16 MHz crystal.
	FCLK1	FDC CLK Input #1	I	
6	FCLK2	FDC CLK Input #2	I	TTL level input used for non-standard data rates; can be driven with a 9.6 MHz clock for 300 Kbs MFM data rate and only be selected from the control register.
7	$\overline{RDD}$	FDC Read Disk	I	This is the raw serial bit stream from the disk drive. Each falling edge of the pulses represents a flux transition of the encoded data.
9	FIRQ	FDC Interrupt Request	O	Interrupt request indicating completion of command execution or data transfer requests (non-DMA mode). In PCAT mode, this pin is tri-stated, enabled by DMAEN signal from the Operations Register.
10	$\overline{DCHG}$	FDC Disk Changed	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low and drive door is open or that the diskette has possibly changed since last drive selection. The pin has an internal pull-up register.
11	PCVAL	FDC Precompensation Value Select	I	This pin determines the amount of write precompensation used on the inner tracks of the diskette. Logic 1 = 125 ns, 0 = 187 ns. In the defeat option, the PCVAL input is a don't care, and internally the pre-comp value is disabled.

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		Data To/From Floppy - Floppy Control, Continued		
12	DRV PS2	FDC Drive Type FDC PS2 Drive Type	I O	In the input mode, a logic 0 indicates to the FDC that a 2-speed spindle motor is present and that FCLK2 should be grounded because it will not be used. As an option, this pin can be defined as an output to support the floppy drive connector pin 2 for PS/2 style drives, indicating the FDC is set internally for a single spindle motor. The pin has an internal pull-up resistor.
13	$\overline{HS}$	FDC Head Select	O	This high current driver (HCD) output selects the head, i.e., side, of the floppy disk that is being read or written. Logic 1 = side 0, logic 0 = side 1.
14	$\overline{WE}$	FDC Write Enable	O	This HCD output becomes true, active low, just prior to writing on the diskette. This allows current to flow through the write head.
15	$\overline{WD}$	FDC Write Data	O	This HCD is the write data output. Each falling edge of the encoded data pulse stream causes a flux transition on the media.
17	$\overline{DIRC}$	FDC Stepper Direction	O	This HCD output determines the direction of head stepper motor. Logic 1 = outward motion, logic 0 = inward motion.
18	$\overline{STEP}$	FDC Stepper Step	O	This HCD output issues an active low pulse for each track to track movement of the head.
28	$\overline{HDL}$	FDC Head Load	O	This HCD output, when active low, causes the head to be loaded against the media in the selected drive.
29	$\overline{RWC}$ $\overline{RPM}$	FDC Reduce Write Current Revolutions Per Minute	O O	This HCD output, when active low, causes a reduced write current when bit density is increased toward the inner tracks, becoming active when tracks > 2. In PCAT mode, this signal can be used on 2-speed drives to select 300 RPM, active low, when 250 MFM or 125 FM KBs is selected and DRV = 0.
30	PWRDN	FDC Power Down	O	CMOS output, when active high, indicates the FDC portion of the WD76C20 has gone into power down mode. This signal can be used to power down the floppy drive if supported.
31	$\overline{WP}$	FDC Write Protected	I	This Schmitt Trigger (ST) input senses status from the disk drive indicating active low when a diskette is write protected.

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
		Data To/From Floppy - Floppy Control, Continued		
32	$\overline{TR00}$	FDC Track Zero	I	This ST input senses status from the drive indicating active low, when the head is positioned over the outermost track, track 00.
33	$\overline{IDX}$	FDC Index Hole	I	This ST input senses status from the drive indicating active low when the head is positioned over the beginning of a track, marked by an index hole.
		Chip Select		
50	$\overline{CSEN}$	CSL Chip Select Enable	I	Chip Select Enable TTL input used to output enable the appropriate CSL control line as decoded from the RA8, RA9, RA10, DPL and DPH inputs. When DACKEN is asserted low, the function of $\overline{CSEN}$ is negated. When used to enable and disable the WD76C30 48 MHz clock, $\overline{CSEN}$ acts as a strobe to a latch. When it and DACKEN are both asserted, the TC output will go high.
51	DACKEN	CSL Dack Enabled	I	TTL input that indicates the host is performing a DMA transfer unrelated to the WD76C20. When active high, it is used to disqualify all CSL input lines.
52	DPH	CSL Address Parity High	I	Decoded chip select TTL input pad, bit CS4.
53	DPL	CSL Address Parity Low	I	Decoded chip select TLL input pad, bit CS3.
54	RA10	CSL Address Line 10	I	Decoded chip select TTL input pad, bit CS2.
55	RA9	CSL Address Line 9	I	Decoded chip select TTL input pad, bit CS1.
56	RA8	CSL Address Line 8	I	Decoded chip select TTL input pad, bit CS0.
58	BALE	CSL Bus ALE	I	TTL input which, when active high, causes latches on the CSL Input Code ($\overline{CSEN}$, DPH, DPL, RA10, RA9, RA8) to become transparent. When BALE is forced low, the data in the transparent latches is latched. This pin has an internal pull-up resistor so the pin can be left unconnected and the latches transparent.
70	TC	CSL Host Terminal Count	O	CMOS level output used to indicate the final count has been reached during a host DMA transfer unrelated to the WD76C20. It is also used internally by the FDC to indicate a DMA transfer to the floppy drive is complete. TC asserts high when both DACKEN and $\overline{CSEN}$ are asserted. (DACKEN=1, $\overline{CSEN}$=0).

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
			Chip Select, Continued	
71	PRDY	CSL Processor Ready	I	ST input senses processor ready status to help latch the CSL inputs correctly during system byte swapping activities. This pin has an internal pull-up resistor so that it can be left unconnected when not needed. The PRDY input should be used in system designs that use the BALE pin.
72	$\overline{\text{EMS}}$	CSL External EMS Access	O	CMOS card select output decoded from CSL input lines and issued to select external EMS.
73	$\overline{\text{PROGCS}}$	CSL Program Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a programmable chip select.
74	PCUW1	CSL Power Control Unit Write Strobe #1	O	CMOS write strobe output decoded from CSL input lines and issued to write to the PCU #1.
75	PCUW0	CSL Power Control Unit Write Strobe #0	O	CMOS write strobe output decoded from CSL input lines and issued to write to the PCU #0.
76	$\overline{\text{NPCS}}$	CSL Numerical Processor Chip Select	O	CMOS chip select output decoded from CSL input lines and issued to select the numerical processor, the 80287.
77	$\overline{\text{CS8042}}$	CSL 8042 Chip Select	O	CMOS chip select output decoded from CSL input lines and issued to select the 8042.
78	$\overline{\text{ROMOE}}$	CSL ROM Output Enable	O	CMOS chip select output decoded from CSL input lines and issued to output enable the BIOS ROM.
79	$\overline{\text{CSPAR0}}$	CSL Parallel Port #0 Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the parallel port #0.
80	$\overline{\text{CSSSEB}}$	CSL Serial Port B Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the serial port B.
81	$\overline{\text{CSSERA}}$	CSL Serial Port A Chip Select	O	CMOS chip select output decoded from CSL input lines and issued as a chip select to the WD76C30 to enable the serial port A.
			Real Time Clock	
58	$\overline{\text{RCLR}}$	RTC RAM Clear	I	A dual function pin. As long as it is held low, all 76C20 outputs are held in a high impedance state to facilitate testing. It is also used as a ST input to clear all 114 bytes of the general purpose RAM. None of the clock or calendar functions are interrupted, and the 14 registers that are used by the RTC are left unchanged. This pin has an internal pull-up so it can be left unconnected.

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
				Real Time Clock, Continued
60	$\overline{\text{RTCX}}$	RTC Time Base XTAL Out	O	XTAL oscillator output for parallel resonant AT cut crystal at 32.768 KHz.
61	RTCX	RTC Time Base XTAL In	I	32.768 KHz XTAL oscillator input for use with crystal oscillator circuit.
62	VBAT	RTC Battery Backup	NA	Battery backup power supply VDD pin. A 3-volt battery connector can be attached to maintain the RTC timekeeping functions and SRAM integrity during system power downs. (See Figure 2-3a)
69	$\overline{\text{RTCIRQ}}$	RTC Interrupt Request	O	Open-drain CMOS output that is set to tristate unless the RTC needs to interrupt the processor, when the pin goes low and stays low until register C is read, or the part is reset through the RESET pin.
				Suspend/Resume Support
63	MX14	S/R 14.318 MHz Crystal In	I	Crystal oscillator input for the 14.318 MHz oscillator.
64	$\overline{\text{MX14}}$	S/R 14.318 MHz Crystal Out	O	Crystal oscillator output for the 14.318 MHz oscillator.
66	PDREF	Suspend/Resume DRAM Refresh	O	External DRAM refresh line used to support the WD76C10 when it goes into Suspend/Resume mode. During Suspend/Resume mode, this pad provides a 1.0 µS ± 0.5 µS pulse once every 15.26 µS and is used to maintain the DRAM integrity with as little power as possible. Suspend/Resume mode is entered when a CSL address of 15H is detected and exited when a CSL address of 16H is issued.
68	OSC	S/R WD76C10 Clock Driver	O	CMOS level clock driver output used to support the WD76C10. When not in the WD76C10's suspend/resume mode, the output waveform is a 14.318 MHz square wave, and when in suspend/resume mode, it becomes a 32.768 KHz square wave. The WD76C10 suspend/resume mode is entered when a CSL address of 15H is detected and exited when a CSL address of 16H is issued.
				Data Bus
35-42	DB(0-7)	BIL Processor Data/Address Bus	I/O	8-bit bi-directional, tristateable data bus.

TABLE 2-5. PIN DESCRIPTIONS, continued

PIN	MNEMONIC	SIGNAL NAME	I/O	DESCRIPTION
				Motor Control
23	$\overline{MO0}$	FDC Motor on #0	O	This HCD output, when active low, is motor on enable for disk drive #0, in PCAT mode.
24	$\overline{MO1}$	FDC Motor on #1	O	This HCD output, when active low, is motor on enable for disk drive #1, in PCAT mode.
26	$\overline{MO2}$	FDC Motor on #2	O	Reserved for 4 Mbyte support (density select).
27	$\overline{MO3}$	FDC Motor on #3	O	Reserved for 4 Mbyte support (density select).
				Drive Select
19	$\overline{DS0}$	FDC Drive Select #0	O	This HCD output, when active low, is Drive #0 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN0 bit.
20	$\overline{DS1}$	FDC Drive Select #1	O	This HCD output when active low is Drive #1 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN1 bit.
21	$\overline{DS2}$	FDC Drive Select #2	O	This HCD output, when active low, is Drive #2 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN2 bit.
22	$\overline{DS3}$	FDC Drive Select #3	O	This HCD output, when active low, is Drive #3 select in PC/AT mode, enabling the interface in the disk drive. The signal is qualified by the MOEN3 bit.
				Miscellaneous
2, 16, 25, 34, 46, 65		VSS		
5, 44, 67		VDD		

TABLE 2-5. PIN DESCRIPTIONS, continued

2.3 CHIP SELECT DECODE

The following codes are qualified by $\overline{CSEN}$ (Logic = 0) and disabled by DACKEN (Logic = 1).

CSL INPUT LINES						
CS#	DPH	DPL	RA10	RA9	RA8	FUNCTION
00H	0	0	0	0	0	Assert $\overline{ROMOE}$ to Output Enable the ROM BIOS[1]
01H	0	0	0	0	1	Assert $\overline{CS8042}$ to Chip Select the Keyboard Control[1]
02H	0	0	0	1	0	Assert $\overline{NPCS}$ to Chip Select the Numerical Processor[1]
03H	0	0	0	1	1	Assert PCUW0 to Write Strobe PCU #0
04H	0	0	1	0	0	Assert $\overline{LCLACK}$ to Acknowledge Keyboard Processor[1]
05H	0	0	1	0	1	Assert RTC ALE for RTC I/O[1]
06H	0	0	1	1	0	Assert RTC Write Strobe Gated by $\overline{CSEN}$ & $\overline{IOW}$[1]
07H	0	0	1	1	1	Assert RTC Read Stobe Gated by $\overline{CSEN}$ & $\overline{IOR}$[1]
08H	0	1	0	0	0	Assert FDC $\overline{LDOR}$ Register Select Line[1]
09H	0	1	0	0	1	Assert FDC $\overline{FDCS}$ Chip Select Line[1]
0AH	0	1	0	1	0	Assert FDC $\overline{LDCR}$ Register (Read/Write) Select Line[1]
0BH	0	1	0	1	1	Assert FDC $\overline{LDCR}$ Register (Read/Write) Select Line & assert $\overline{IDEDENL}$ and $\overline{CSIDE1}$ IDE Card Select Lines1
0CH	0	1	1	0	0	Assert $\overline{IDEDENL}$ and $\overline{CSIDEO}$ IDE Card Select Line & assert $\overline{IDEDENH}$ if A0 = 0[1]
0DH	0	1	1	0	1	Assert $\overline{IDEDENL}$ and $\overline{CSIDE1}$ IDE Card Select Line[1]
0EH	0	1	1	1	0	Assert $\overline{CSSERA}$ to Chip Select Serial Port A[1]
0FH	0	1	1	1	1	Assert $\overline{CSPAR0}$ to Chip Select Parallel Port 0[1]
10H	1	0	0	0	0	Assert $\overline{CSSERB}$ to Chip Select Serial Port B[1]
11H	1	0	0	0	1	Assert $\overline{PROGCS}$[1]
14H	1	0	1	0	0	Assert $\overline{EMS}$ to signify external EMS memory access[1]
15H	1	0	1	0	1	WD76C30 48 MHz Clk Disable , CSL Latches Code, In, so $\overline{CSSERA}$, $\overline{CSSERB}$ & $\overline{CSPAR0}$ stay asserted[2]
16H	1	0	1	1	0	48 MHz Clk Enable for WD76C30, CSL Un-Latches code, so $\overline{CSSERA}$, $\overline{CSSERB}$ & $\overline{CSPAR0}$ De-Assert[3]
17H	1	0	1	1	1	Assert PCUW1 to Write Strobe PCU #1

TABLE 2-6. CSL INPUT LINE DECODER

[1] These signals are generated using latched CSL inputs if BALE is used.
[2] Suspend Mode is entered by asserting code 15H on the CSL inputs, while qualifying it by $\overline{CSEN}$=0, $\overline{IOW}$=0, and the falling edge of OSC.
[3] Suspend Mode is left by asserting code 16H on the CSL inputs, while qualifying it by an OSC falling edge.

2.4 PIN STATES DURING POWER DOWN MODE

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND MODE IN	SUSPEND MODE OUT
1	$\overline{\text{IDEDENH}}$	OUTPUT		O		O		Z
2	VSS	VSS						
3	$\overline{\text{FX1}}$	OUTPUT		Z		Z		Z
4	FX1	INPUT	IH		IH		IH	
5	VDD	VDD						
6	FCLK2	INPUT	IH		IH		IH	
7	$\overline{\text{RDD}}$	SCH INPUT	IH		IH		IH	
8	DMA	BIDIRECT (input unused)	IH	Z***	IH	Z***	IH	Z
9	FIRQ	BIDIRECT	IH	Z***	IH	Z***	IH	Z
10	$\overline{\text{DCHG}}$	SCH W/PULLUP	IH		IH		IH	
11	PCVAL	SCH INPUT	IH		IH		IH	
12	DRV	BIDIRECT SCH (W/PULLUP)	IH	Z	IH	Z	IH	Z
13	$\overline{\text{HS}}$	OUTPUT		Z		Z		Z
14	$\overline{\text{WE}}$	OUTPUT		Z		Z		Z
15	$\overline{\text{WD}}$	OUTPUT		Z		Z		Z
16	VSS	VSS						
17	$\overline{\text{DIRC}}$	OUTPUT		Z		Z		Z
18	$\overline{\text{STEP}}$	OUTPUT		Z		Z		Z
19	$\overline{\text{DS0}}$	OUTPUT		Z		Z		Z
20	$\overline{\text{DS1}}$	OUTPUT		Z		Z		Z
21	$\overline{\text{DS2}}$	OUTPUT		Z		Z		Z
22	$\overline{\text{DS3}}$	OUTPUT		Z		Z		Z
23	$\overline{\text{MO0}}$	OUTPUT		Z		Z		Z
24	$\overline{\text{MO1}}$	OUTPUT		Z		Z		Z
25	VSS	VSS						
26	$\overline{\text{MO2}}$	OUTPUT		Z		Z		Z
27	$\overline{\text{MO3}}$	OUTPUT		Z		Z		Z
28	$\overline{\text{HDL}}$	OUTPUT		Z		Z		Z
29	$\overline{\text{RWC}}$	OUTPUT		Z		Z		Z
30	PWRDN	OUTPUT		OH		OH		OH
31	$\overline{\text{WP}}$	INPUT	IH		IH		IH	

TABLE 2-7. PIN STATES DURING POWER DOWN MODES

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND IN	MODE OUT
32	$\overline{TR00}$	INPUT	IH		IH		IH	
33	$\overline{IDX}$	INPUT	IH		IH		IH	
34	VSS	VSS						
35	*DB0	BIDIRECT	I	O	I	O	IH	Z
36	*DB1	BIDIRECT	I	O	I	O	IH	Z
37	*DB2	BIDIRECT	I	O	I	O	IH	Z
38	*DB3	BIDIRECT	I	O	I	O	IH	Z
39	*DB4	BIDIRECT	I	O	I	O	IH	Z
40	*DB5	BIDIRECT	I	O	I	O	IH	Z
41	*DB6	BIDIRECT	I	O	I	O	IH	Z
42	*DB7	BIDIRECT	I	O	I	O	IH	Z
43	IDED7	BIDIRECT	I	O	I	O	IH	Z
44	VDD	VDD						
45	A0	INPUT	I		I		IH	
46	VSS	VSS						
47	$\overline{DACK}$	INPUT	I		I		IH	
48	$\overline{IOR}$	INPUT	I		I		IH	
49	$\overline{IOW}$	INPUT	I		I		IH	
50	$\overline{CSEN}$	INPUT	I		I		I	
51	DACKEN	INPUT	I		I		I	
52	DPH	INPUT	I		I		I	
53	DPL	INPUT	I		I		I	
54	RA10	INPUT	I		I		I	
55	RA9	INPUT	I		I		I	
56	RA8	INPUT	I		I		I	
57	RESET	INPUT	I		I		I	
58	$\overline{RCLR}$	INPUT	I		I		IH	
59	BALE	INPUT W/PULLUP	I		I		IH	
60	$\overline{RTCX}$	OUTPUT		O		O		O
61	RTCX	INPUT	I		I		I	
62	VBAT	VDD						
63	MX14	INPUT	I		I		IH	
64	$\overline{MX14}$	OUTPUT		O		O		Z
65	VSS	VSS						

TABLE 2-7. PIN STATES DURING POWER DOWN MODES, continued

PIN NO.	SIGNAL NAME	INPUT/ OUTPUT	PD OPT1 IN	PD OPT1 OUT	PD OPT2 IN	PD OPT2 OUT	SUSPEND IN	MODE OUT
66	PDREF	OUTPUT		O		O		O
67	VDD	VDD						
68	OSC	OUTPUT		O		O		O
69	RTCIRQ	OUTPUT		O		O		O
70	TC	OUTPUT		O		O		O
71	PRDY	INPUT	I		I		IH	
72	$\overline{EMS}$	OUTPUT		O		O		Z
73	$\overline{PROGCS}$	OUTPUT		O		O		Z
74	PCUW1	OUTPUT		O		O		O
75	PCUW0	OUTPUT		O		O		O
76	$\overline{NPCS}$	OUTPUT		O		O		Z
77	$\overline{CS8042}$	OUTPUT		O		O		Z
78	$\overline{ROMOE}$	OUTPUT		O		O		Z
79	$\overline{CSPAR0}$	OUTPUT		O		O		O
80	$\overline{CSSERB}$	OUTPUT		O		O		O
81	$\overline{CSSERA}$	OUTPUT		O		O		O
82	$\overline{CSIDE1}$	OUTPUT		O		O		Z
83	$\overline{CSIDE0}$	OUTPUT		O		O		Z
84	$\overline{IDEDENL}$	OUTPUT		O		O		Z

TABLE 2-7. PIN STATES DURING POWER DOWN MODES, continued

NOTES:

IH = Input High, internally forced high

IL = Input Low, internally forced low

OH = Output High, internally forced high

Z = Output tristated; 1 = Input active; 0 = Output active

* DB is always powered down and Z-state unless chip access is in progress

** Bond option pad, not an additional pin

*** Z only if DMAEN = 0; 0 if DMAEN = 1

3.0 FUNCTIONAL DESCRIPTIONS

3.1 CONTROL REGISTER

(LDCR=0, IOW=0) is a write only register used to set the transfer data rate and disable write precomp. The support logic latches the 3 LSB's of the data bus upon receiving LDCR and IOW. These bits are used to select the desired data rate, which in turn controls the internal clock generation. Clock switchover is internally deglitched, allowing continuous operation after changing data rates. If the Control Register is not used, the data rate is governed by the supplied clock, or crystal, frequency and must be 64 times the desired MFM data rate. This implies a maximum frequency of 16 MHz for the data rate of 250 Kb/s and a maximum frequency of 32 MHz for the data rate of 500 Kb/s, unless the Control Register is used as shown in Table 3-1 and 3-2. Switching this clock must be glitchless, or the device will need to be reset. For all non-standard transfer data rates, Table 3-3 should be used.

As an option, FDC also supports 150 Kb/s FM data transfer rate. The Control Register is used to set the transfer data rate as shown in Table 3-3. FX1 (pin 10) of the part may be driven with a TTL level 9.6 MHz signal. With this setup, only 150 Kb/s (FM) and 300 Kb/s (MFM) data transfer rates can be selected.

In PC/AT mode, precomp can be disabled by the use of the No Write Precomp (NWP) bit of the Control Register.

6

CR1	CR0	DRV	DATA RATE	COMMENTS	PC/ATRPM
0	0	X	500 K	MFM	1
0	0	X	250 K	FM	1
0	1	0	250 K	MFM	0
0	1	1	300 K	MFM (9.6 MHz)	0
1	0	X	250 K	MFM, RESET DEFAULT	0
1	0	X	125 K	FM, RESET DEFAULT	0
1	1	X	125 K	FM	0

TABLE 3-1. 16 MHZ FCLK1 CR1, CR0, DRV DATA RATE DECODER

CR1	CR0	DRV	DATA RATE	COMMENTS	PC/ATRPM
0	0	X	1 M	MFM	1
0	0	X	500 K	FM	1
0	1	0	500 K	MFM	0
0	1	1	300 K	MFM (9.6 MHz)	0
1	0	X	500 K	MFM, RESET DEFAULT	0
1	0	X	250 K	FM, RESET DEFAULT	0
1	1	X	250 K	FM	0

TABLE 3-2. 32 MHZ FX1/FCLK1 CR1,CR0,DRV DATA RATE DECODER

CR1	CR0	DRV	DATA RATE	COMMENTS	PC/AT RPM
0	0	X	300 K	MFM	1
0	0	X	150 K	FM	1

TABLE 3-3. 9.6 MHZ FCLK1 CR1, CR0, DRV DATA RATE DECODER

BIIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	DATA RATE 0 (CR0)	0
1	DATA RATE 1 (CR1)	0
2	NO WRITE PRECOMP (NWP)	0
3-7	RESERVED	NONE

TABLE 3-4. FDC CONTROL REGISTER, ADDR=3F7, PCAT MODE

3.2 OPERATIONS REGISTER

This register includes support logic that latches the data bus upon receiving LDOR and IOW. It replaces the typical latched port seen in floppy subsystems used to control disk drive spindle motors and select desired drive.

DSEL1, DSEL0 - Encoded drive select bits are decoded in Table 3-5 and are valid only if in PC/AT mode.

DS1	DS0	DRIVE SELECT
0	0	$\overline{DS0}$ ACTIVE
0	1	$\overline{DS1}$ ACTIVE
1	0	$\overline{DS2}$ ACTIVE
1	1	$\overline{DS3}$ ACTIVE

TABLE 3-5. DRIVE SELECT DECODER

$\overline{SRST}$ - This is the Soft Reset bit which will reset the FDC when set to a logic level 0. After the Soft Reset has occurred, the bit itself will be reset to a logic 1.

DMAEN - Active in the PC/AT mode, this DMA Enable bit qualifies DMA and FIRQ outputs and $\overline{DACK}$ input.

MOEN3, MOEN2, MOEN1, MOEN0 - These Motor On Enable bits produce the inverted outputs $\overline{MO3}$, $\overline{MO2}$, $\overline{MO1}$ and $\overline{MO0}$ in PC/AT mode.

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	DRIVE SELECT (DSEL0)	0
1	DRIVE SELECT (DSEL1)	0
2	SOFT RESET ($\overline{SRST}$)	1
3	DMA ENABLE (DMAEN)	0
4	MOTOR ON ENABLE (MOEN0)	0
5	MOTOR ON ENABLE (MOEN1)	0
6	MOTOR ON ENABLE (MOEN2)	0
7	MOTOR ON ENABLE (MOEN3)	0

TABLE 3-6. OPERATIONS REGISTER, ADDR=3F2

3.3 MASTER STATUS REGISTER

In the WD76C20, the Master Status Register is a read/write register, where the read only register in the X765 FDC core is an 8-bit register that contains the status information of the FDC and may be accessed at any time. The new write register is called MSR1 and contains support for the power down mode 1 and the PS/2 drive type select. The user may write to this register to enable the power down mode (option 1), to disable user transparent power down mode (option 2), and to set up the PS/2 type drive configuration.

BIT	SIGNAL NAME & FUNCTION	STORAGE ELEMENT	RESET CONDITION	CLOCK QUALIFIER
0	POWER DOWN MODE1 (OPTION 1)	FF	0 (RSTB)	MSRCK
1	PD2ENAB2 DISABLE PDM (OPTION 2)	FF	1 (RSTB)	MSRCK
2	PSSEL0 PS2 DRIVE 0	FF	0 (RSTB)	MSRCK
3	PSSEL1 PS2 DRIVE 1	FF	0 (RSTB)	MSRCK
4	PSSEL2 PS2 DRIVE 2	FF	0 (RSTB)	MSRCK
5	PSSEL3 PS2 DRIVE 3	FF	0 (RSTB)	MSRCK
6	CTST0 PDM3 OPTION 2 (Reserved)	FF	0 (RSTN)	MSRCK
7	CTST1 PDM3 OPTION 2 (Reserved)	FF	0 (RSTN)	MSRCK

TABLE 3-7A. MASTER STATUS REGISTER, ADDR=3F4, WRITE ONLY

Notes:
1. PDM (Power Down Mode). If Option 1 set to PD2ENAB = Disable Power Down Mode 2.
2. If DB0 is set to logic 1, the FDC will enter into user initiated PDM (Power Down Mode) immediately.
3. If DB1 is set to logic 0, the FDC will disable the user transparent PDM Option 2; the hard reset enable enables the PDM Option 2.
4. User transparent power down mode counter test.

BIT	NAME	SYMBOL	DESCRIPTION
DB0	FDD 0 BUSY	D0B	FDD number 0 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB1	FDD 1 BUSY	D1B	FDD number 1 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB2	FDD 2 BUSY	D2B	FDD number 2 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB3	FDD 3 BUSY	D3B	FDD number 3 is in Seek Mode. If any bit is set, FDC will not accept READ or WRITE commands.
DB4	FDC BUSY	CB	A READ or WRITE command is in progress. FDC will not accept any other command.
DB5	EXECUTION MODE	EXM	This bit is set only during Execution phase in non-DMA mode. When DB5 goes low, Execution phase has ended and Results Phase has started. It operates only during non-DMA mode of operation.
DB6	DATA INPUT	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO=1, then transfer is from Data Register to processor. If DIO=0, then transfer is from processor to Data Register.
DB7	REQUEST FOR MASTER	RQM	Indicates Data Register is ready to send or receive data to or from processor. Both DIO and RQM should be used to perform "handshaking" functions of "ready" and "direction" to the processor.

TABLE 3-7B. MASTER STATUS REGISTER, ADDR=3F4, READ ONLY

3.4 PS/2 SUPPORT

The WD76C20 supports up to four PS/2 type drives, and Table 3-8 summarizes the sequence details for PS/2 drive configuration setup by the FDC.

The Master Status Register (MSR) is used in a write mode to set the conditions for drive select and motor enable signals and also to have correct polarity on DRV/PS2 pin for PS/2 type of drives.

Table 3-8 shows the sequence to select the PS/2 type of drives and the polarity on DRV/PS2 pin which is tied to pin 2 on the floppy disk drive connector. Otherwise, if this register is not programmed for PS/2 configuration, the RWC/output from FDC should go to pin 2 of the floppy disk drive connector. The default is AT mode.

3.5 OVERRUN ERROR STATUS REPORTING

The WD76C20 has the capability to detect and flag data overruns during DMA operations. This situation may occur, as an example, when a floppy operation, DRAM refresh, and DMA channel 2 transfer occur simultaneously. Should a data overrun occur, D4 (OR) in Status Register 1 will be set.

Versions of the WD76C20 which contain this feature can be distinguished easily by reading RTC RAM location 66H after reset. If the device contains the overrun flag feature, the LSB location 66H will be a logic level 1. In these devices, 66H is read only.

SEQUENCE	CODE	REGISTER VALUE	DESCRIPTION	RWC	DRV
Step 1	3F4	00	Disable FDC sleep mode	X	X
Step 2	3F7	00	Select 500 Kb/s data rate and 3 1/2" 1.44 MB in AT mode	1	1[1]
Step 3	3F2	1C	Disable $\overline{SRST}$, enable $\overline{DS0}$, $\overline{MO0}$ and DMAEN bit of OP register	1	1
Step 4	3F4	04	Enable bit 2 of MSR and select PS2 drive0 (1.44 MB)	1	1[2]
Step 5	3F2	1C	Disable SRST, enable DS0, MO0 and DMAEN bit of OP register	1	0[3]
Step 6	3F4	08	Enable bit 3 of MSR and select	X	X[4]
Step 7	3F7	02	Select 250 Kb/s data rate and 3 1/2" 720 KB drive	0	0
Step 8	3F2	2D	Disable SRST, enable DS1, MO1 and DMAEN bit of OP register PSSEL1 (3 1/2" 720 KB)	0	1[5]

TABLE 3-8. PS/2 SUPPORT

Notes:

[1] Default for $\overline{RWC}$ and DRV/PS2 is AT mode.

[2] Since 500K data rate is selected, the PSSEL0 will select drive 0, and the system configuration for this should be set up for 3 1/2" and 1.44M PS/2 type of drive.

[3] Operation Register will select drive 0 and motor 0.

[4] Master Status Register will select PSSEL1.

[5] Step 5 and 6 will select 250K data rate, the PSSEL1 will select drive 1, and the system configuration for this should be set up for 3 1/2" and 720 KB PS/2 type of drive.

3.6 REAL TIME CLOCK REGISTERS

Shown in Figure 3-1 is a memory map of the RTC SRAM and operational registers. Under normal operating conditions all of the registers may be written to or read from except the following:

- Registers C and D are Read Only.
- Bit 7 of register A is Read Only.
- The high order bit of the seconds byte is Read Only.

0	14 BYTES	00H
13		0DH
14	114 BYTES GENERAL PURPOSE RAM	0EH
102	VERSION NUMBER	66H
127		7FH

0	SECONDS	00H
1	SECONDS ALARM	01H
2	MINUTES	02H
3	MINUTES ALARM	03H
4	HOURS	04H
5	HOURS ALARM	05H
6	DAY OF THE WEEK	06H
7	DAY OF THE MONTH	07H
8	MONTH	08H
9	YEAR	09H
10	REGISTER A	0AH
11	REGISTER B	0BH
12	REGISTER C	0CH
13	REGISTER D/ID	0DH

FIGURE 3-1. RTC ADDRESS MAP

Writing the correct time to the RTC is accomplished by first programming the SET bit in register B to a logic 1, and the Data Mode bit (DM) of Register B to the appropriate level. Then the ten bytes representing the current time and alarm status can be loaded from the host into the RTC without a chance of internal bus contention by simply addressing the appropriate memory locations and performing a normal I/O write operation. After all ten timing bytes and the DM bit have been written to the RTC, the SET bit should be cleared. After this, the DM bit cannot be changed without re-initializing all ten registers. Table 3-9 shows the Binary and BCD formats of the time, calendar and alarm locations. When the 12 hour format is selected, the high order bit of the hours byte represents AM when it is a logic 0, and PM when it is a logic 1. Once a second, the ten bytes are updated and checked for alarm conditions. If a Host read of the time occurs during an update, the hours, minutes and seconds may not agree. Methods to avoid this possibility are covered later.

Alarms can be set to interrupt the Host in a variety of different ways, including intervals ranging from once a day to once a second. The method used to set the periodicity is to write don't care bytes (any value from C0 to FF) into the appropriate alarm registers. Therefore an alarm scheduled to interrupt the Host only once a day would have all alarm registers programmed to the proper values. An alarm scheduled to go off once an hour would have a don't care value in the hour register. One scheduled to go off every minute would have don't care values programmed into hours and minutes. And finally, an alarm will go off every second if all three registers are programmed to don't cares.

ADDRESS LOCATION	FUNCTION	DECIMAL RANGE	RANGE BINARY DATA MODE	BCD DATA MODE
00	SECONDS	0-59	00-3B	00-59
01	SECONDS ALARM	0-59	00-3B	00-59
02	MINUTES	0-59	00-3B	00-59
03	MINUTES ALARM	0-59	00-3B	00-59
04	HOURS - 12 HR MODE	1-12	01-0C AM, 81-8C PM	01-12 AM, 81-92 PM
	HOURS - 24 HR MODE	0-23	00-17	00-23
05	HRS ALARM - 12 HR MODE	1-12	01-0C AM, 81-8C PM	01-12 AM 81-92 PM
	HRS ALARM - 24 HR MODE	0-23	00-17	00-23
06	DAY OF WEEK (SUNDAY=1)	1-7	01-17	01-17
07	DATE OF MONTH	1-31	01-1F	01-31
08	MONTH	1-12	01-0C	01-12
09	YEAR	0-99	00-63	00-99

TABLE 3-9. RTC DATA MODES

REGISTER A SELECT BITS RS3	RS2	RS1	RS0	PERIODIC INTERRUPT RATE
0	0	0	0	NONE
0	0	0	1	3.90625 mS
0	0	1	0	7.8125 mS
0	0	1	1	122.070 µS
0	1	0	0	244.141 µS
0	1	0	1	488.281 µS
0	1	1	0	976.5625 µS
0	1	1	1	1.953125 mS
1	0	0	0	3.90625 mS
1	0	0	1	7.8125 mS
1	0	1	0	15.625 mS
1	0	1	1	31.25 mS
1	1	0	0	62.5 mS
1	1	0	1	125 mS
1	1	1	0	250 mS
1	1	1	1	500 mS

TABLE 3-10. RTC PERIODIC INTERRUPT RATE DECODER

RS3, RS2, RS1 and RS0 are used to select the periodic interrupt rate as seen in the table above. Once the rate is selected, use the PIE bit to enable the interrupt. Functionally, these pins are decoded to choose which spot to tap on the divider chain to generate the interrupts.

DV2, DV1 and DV0 enable and disable the oscillator for use during product shipping. The code 010 will turn the oscillator on and start dividing.

UIP is the Update In Progress bit, which can be used by the Host to determine when updates are not going to occur. If the UIP bit is low, the Host can assume that a transfer is not going to happen for at least another 244 µS, during which time registers 0-9 are fully available. Writing a logic 1 to the SET bit inhibits any further updates and clears the UIP bit.

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	PERIODIC INTERRUPT RATE SELECT BIT 0 (RS0)	UNAFFECTED
1	PERIODIC INTERRUPT RATE SELECT BIT 1 (RS1)	UNAFFECTED
2	PERIODIC INTERRUPT RATE SELECT BIT 2 (RS2)	UNAFFECTED
3	PERIODIC INTERRUPT RATE SELECT BIT 3 (RS3)	UNAFFECTED
4	OSCILLATOR CONTROL BIT 0 (DV0)	UNAFFECTED
5	OSCILLATOR CONTROL BIT 1 (DV1)	UNAFFECTED
6	OSCILLATOR CONTROL BIT 2 (DV2)	UNAFFECTED
7	UPDATE IN PROGRESS (UIP)	UNAFFECTED

TABLE 3-11. RTC REGISTER A, BIT 7 IS READ ONLY

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0	DAYLIGHT SAVINGS ENABLE (DSE)	UNAFFECTED
1	HOURS FORMAT (24/12)	UNAFFECTED
2	DATA MODE (DM)	UNAFFECTED
3	RESERVED	NONE
4	UPDATE ENDED INTERRUPT ENABLE (UIE)	0
5	ALARM INTERRUPT ENABLE (AIE)	0
6	PERIODIC INTERRUPT ENABLE (PIE)	0
7	WRITE TO REGISTERS 0-9 IN PROGRESS (SET)	UNAFFECTED

TABLE 3-12. RTC REGISTER B

DSE - This Daylight Savings Enable bit allows the RTC to perform the adjustments required to maintain daylight savings. On the first Sunday in April, the time increments from 1:59:59 AM to 3:00:00 AM, and on the last Sunday in October at 1:59:59 AM, it changes to 1:00:00 AM

24/12 - This control bit sets the time to a 24 hour format if set to a logic 1, and to a 12 hour AM, PM format if reset to 0.

DM - This DATA Mode control bit sets and indicates whether the time is stored in binary or BCD format. A logic 1 in the DM bit indicates binary, and a logic 0 indicates binary coded decimal data.

UIE - When the Update Interrupt Enable bit is set to logic 1, it enables a function that interrupts the Host whenever the Update Flag (UF) is set to 1.

AIE - When the Alarm Interrupt Enable bit is set to logic 1, it enables a function that interrupts the Host whenever the Alarm Flag (AF) is set to 1.

PIE - When the Periodic Interrupt Enable bit is set to logic 1, it enables a function that interrupts the Host whenever the Periodic Interrupt Flag (PF) is set to 1.

SET - When the SET bit is written to a logic 1, a write to registers 0-9 can proceed without the possibility of an update cycle occurring part way through.

UF - The Update Ended Interrupt Flag is set to logic 1 after, and reset to logic 0 during, each update cycle.

AF - The Alarm Interrupt Flag is set to logic 1 whenever an alarm condition is met, either through a timing match or don't care conditions. It is cleared by reading Register C or resetting the part.

PF - A read only bit, this Periodic Interrupt Flag is a logic 1 when the divider tap determined by the decoded RSX lines changes state. The bit is independent of the PIE bit, but the PIE bit still controls whether or not an RTCIRQ pulse is generated. The

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0-3	RESERVED	NONE
4	UPDATE ENDED INTERRUPT FLAG (UF)	0
5	ALARM INTERRUPT FLAG (AF)	0
6	PERIODIC INTERRUPT FLAG (PF)	0
7	INTERRUPT REQUEST FLAG (IRQF)	0

TABLE 3-13. RTC REGISTER C, READ ONLY

BIT	SIGNAL NAME & FUNCTION	RESET CONDITION
0-3	REVISION ID CODE (ID0, ID1, ID2, ID3)	UNAFFECTED
4-6	RESERVED	NONE
7	VALID RAM AND TIME (VRT)	UNAFFECTED

TABLE 3-14. RTC REGISTER D, READ ONLY

bit is cleared by reading Register C or resetting the part.

IRQF -The Interrupt Request Flag is set to logic 1 whenever the RTC is issuing a Host service interrupt request. The Boolean equation for the flag is IRQF = PF·PIE + AF·AIE + UF·UIE.

ID3, ID2, ID1 and ID0 - used to indicate the device ID code, which exists to identify the chip during board level testing.

VRT - Valid RAM and Time is a read only bit used by the RTC to indicate the possibility of a corruption of the SRAM memory locations. A logic 0 would indicate an interrupt in the power, during which sufficient voltage was not provided by either VBAT or VDD.

3.7 FDC FUNCTIONAL MODE SELECT

PCAT and Test Modes - Each of these modes allow subtle differences which the user may find desirable. Note, the Control Register may be used in any mode without altering functionality.

PCAT Mode

For PCAT compatibility, users will write to the Operations Register after a hardware reset.

FDC Power Down Mode Option 1 - The WD76C20 should enter in Power Down Mode Option 1 when bit 0 of MSR1 register (OPT1) is set to logical 1 and the following conditions are met:

- The PD bit of the MSR1 write only register is set to logic 1
- The RST pin to FDC is inactive
- The bit 2 of Operations Register $\overline{SRST}$=1
- FDC is waiting command from Host

The FDC will return from Power Down Mode Option 1 when the WD76C20 RESET is active and the FDC is reset. This will also reset bit 0 of MSR1 register to logic 0. The XTAL oscillator will turn on automatically once the chip is reset, but may need 20 ms to stabilize. The FDC standby current during the mode is maximum 100 µA. During this time through the normal Master Status register protocol the "request for master" (RQM) bit 7 in the MSR will be inactive. (ROM bit indicates that data register is ready to send or receive data to or from the processor). The FDC can also be brought out from Power Down Mode.

When exiting power down mode option 1, a soft reset assures that an internal reset is generated and the reset is active long enough for the internal clocks and oscillator to start cleanly. If the mode is ever exited by merely writing to the MSR, then it is recommended that a soft reset be issued and a timeout be instituted to allow the oscillator to stabilize (20 ms). The soft reset can be released after this stabilization wait period.

FDC Power Down Mode Option 2 - This is a user transparent power down mode. The FDC has been designed to enter in Power Down Mode automatically 500 ms after the beginning of IDLE state (based on the 500 Kb/s data rate). During this time the XTAL oscillator, all the internal clocks, drive interface signals and all the interface signals to FDC will be shut off. The Host interface path to FDC will be active during this time. For low power consumption, the Host interface signals should be held to DC logic levels 1 or 0.

The FDC will come out from PDM by any Host access to FDC. The XTAL oscillator will turn on automatically and need at least 20 ms for oscillator to stabilize and during this time bit 7 of Master Status Register will be logic = 0. Once the Bit 7 of the MSR is set to logic 1, the FDC will be ready to receive any command from Host. During power down mode, the contents of FDC registers will not be affected, and FDC will come up in the same mode as it was before it entered into PDM. The power down mode can be disabled by writing a logic 0 in Bit 1 of the MSR. The default is power down mode enabled all the time after hard reset or chip power up.

Chip Set Power Down

The following denotes I/O status during three different power down options:

- **#1 - FDC Core and Disk Interface I/O Only**
  - During this power down mode, all the input signals to floppy core, except RESET, are shut off. All the floppy disk interface input and output pins are either disabled or tristated.
  - The WD76C20 Host interface input and output pins not related to FDC core are left unaffected by this mode.
  - All the analog circuitry, the XTAL oscillator and clock internal to FDC are shut off.
- **#2 - FDC Core and Disk Interface I/O Only**
  - This is a user transparent power down mode for FDC core and all the FDC disk interface pins. The Host interface to and from FDC core and WD76C20 pins is not affected by this power down mode.
  - All the analog circuitry, the XTAL oscillator and clock internal to FDC are shut off.
- **#3 - WD7600 Core Chip Set Power Down Mode**
  - For FDC core, this mode is exactly the same as Option #2.
  - Only signals which must be active in suspend mode remain active. All other pins are shut off, disabled or tristated.

Device Reset

When asserted, the $\overline{\text{RESET}}$ pin causes the WD76C20 to perform a a hardware reset on the entire chip, including all the subsystems. The FDC supports both a hardware reset pin, $\overline{\text{RESET}}$, and software reset, SRST, through use of the Operations Register. The $\overline{\text{RESET}}$ pin will cause a device reset for the active duration. Default selects 500K MFM (or 250 K FM code dependent) as the data rate (32 MHz input clock). SRST also causes a reset condition for the active duration which will reset the microcontroller as did the $\overline{\text{RESET}}$, but will NOT affect the current data rate selection or the Mode. When both $\overline{\text{RESET}}$ and SRST are active, the high current driver outputs to the disk drive will be disabled.

If the XTAL oscillator is used, instead of the TTL driven clock inputs, the hardware $\overline{\text{RESET}}$ active time requirement will be extended. The oscillator circuit is designed so $\overline{\text{RESET}}$ will bootstrap the circuit into guaranteed oscillation in a fixed amount of time. The extended reset time allows the growth of the oscillation to produce stable internal clock timing.

Within the RTC, neither the clock, calendar, nor SRAM are affected by the hardware reset function. On powerup, the $\overline{\text{RESET}}$ pin must be held low for at least 200 ms to allow the power supply to stabilize. Some Control Register bits have affected reset conditions as shown in Tables 3-10 to 3-13.

4.0 SPECIFICATIONS

4.1 OPERATIONAL

Absolute Maximum Ratings - All voltages referenced to VSS

VCC . . . . . 7.0 Vol

Voltage at any pin . . . . . + 0.3 Volts

Storage Temperature . . -55 ° to +150 ° C

Operating Temperature . 0° to +70° C

TA = 0°C (32°F) to 70°C (158°F)

VCC = 5V = ± 10%

CL = 100 pf

VIL/VOL referenced to 0.8V

VIH/VOH referenced to 2.0V

CY specifies FX1 period

MCY specifies MCLK period, dependent on selected data rate

WCY specifies WCLK period, dependent on selected data rate.

4.2 INTERFACE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
VCC	+5V Supply	4.5	5.5	V
VBAT	Battery Backup Voltage	2.6	VDD	V
VIL	Input Low Voltage - Data Bus & XTOCS		0.8	V
VIH	Input High Voltage - Data Bus & XTOCS	2.0		V
VILT	Input Low Threshold - Schmitt Trigger	0.8	1.1	V
VIHT	Input High Threshold - Schmitt Trigger	1.7	2.0	V
VHYS	Schmitt Trigger Hysteresis	0.45		V
VOLAT	Output Low - DBus, FIRQ, DMA; IO=12.0 mA		0.4	V
VOHAT	Output High - DBus, FIRQ, DMA; IO= -5.0 mA	2.8		V
VOLHC	Output Low - Drive Interface IO=48 mA		0.4	V
VOL	Output Low - All Others; IO=4.0 mA		0.4	V
VOH	Output High - All Others; IO=400 µA	2.8		V
ILUL	Latch Up Current Low	40		mA
ILUH	Latch Up Current High	-40		mA
ILL	Leakage Current Low		10	µA
ILH	Leakage Current High		-10	µA
ICC	Supply Current - 100 µA source loads		70	mA
ICC	Supply Current - 5 mA source loads		140	mA
ICCPDM1	Supply current in power down mode[1] (Option 1)		200	µA
ICCPDM2	Supply current in power down mode[1] (Option 2)		2	mA
ICCPDM3	Supply current in chip set power down mode		200	µA
ICCBAT	Supply current in battery backup mode[1]		50	µA
PD	Power Dissipation - ICC max[3]		700	mW
PDHL	Power Dissipation - ICCHL max[2 3]		850	mW

TABLE 4-A. DC CHARACTERISTICS

[1] Vin = VCC or GND, IO=0 mA
[2] Includes DBx; IO=-5.0 mA source loads
[3] Includes open drain high current drivers at Vol=0.4V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1MCY	+150 ns

TABLE 4-1. FDC READ TIMING SPECFICIATION

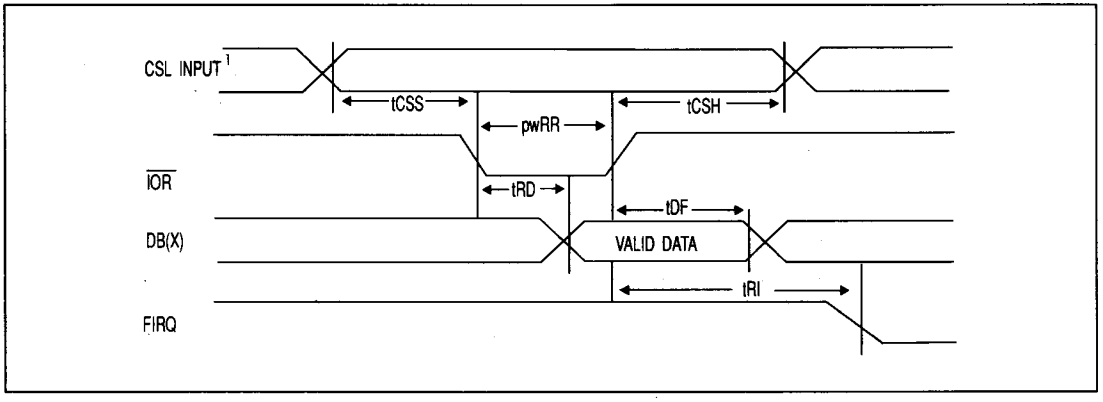


FIGURE 4-1. FDC READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRR	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tRD	Data Access Time from $\overline{IOR}$ Low		175	ns
tDF	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns
tRI	FIRQ Reset Delay Time from $\overline{IOR}$ High		1 MCY+150 ns	

TABLE 4-2. FDC READ W/BALE TIMING SPECIFICATION

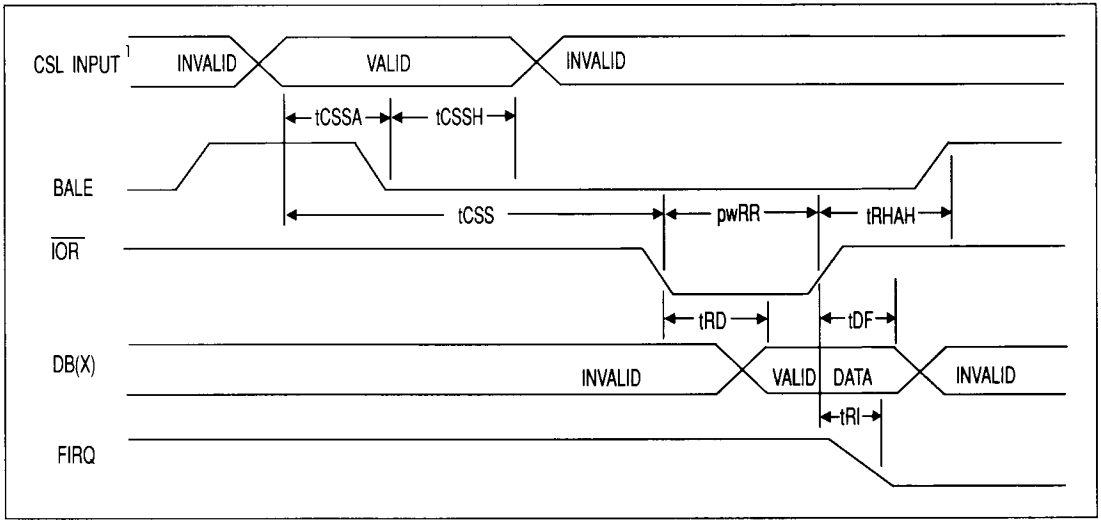


FIGURE 4-2. FDC READ W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1MCY +	150ns

TABLE 4-3. FDC WRITE TIMING SPECIFICATION

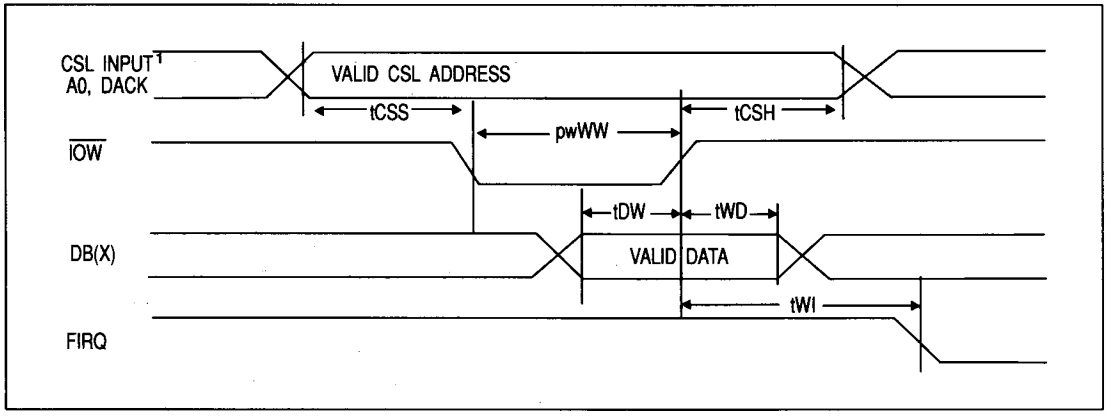


FIGURE 4-3. FDC WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns
tWI	FIRQ Reset Delay from $\overline{IOW}$ High		1 MCY+150ns	

TABLE 4-4. FDC WRITE W/BALE TIMING SPECIFICATION

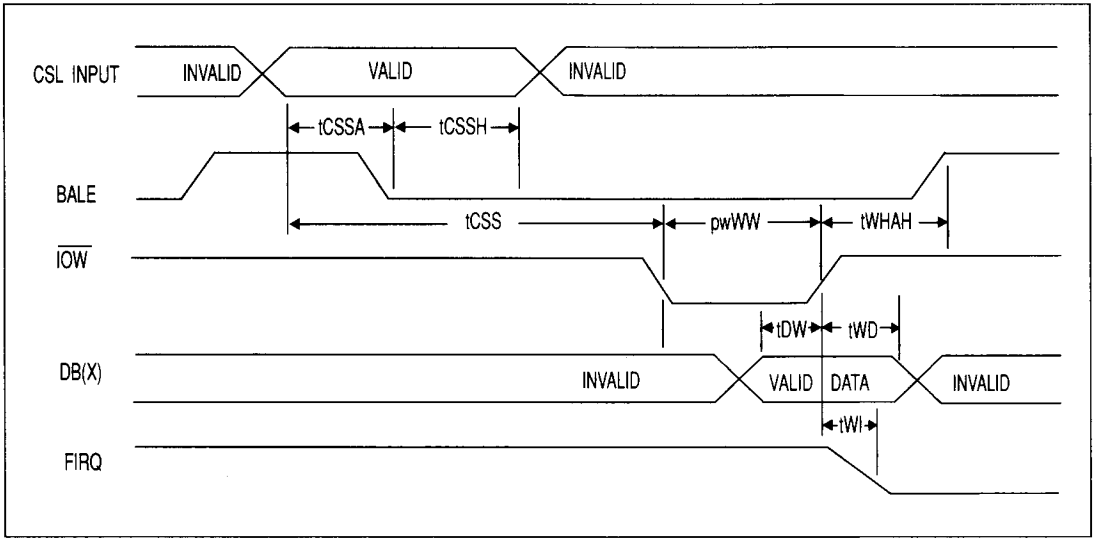


FIGURE 4-4. FDC WRITE W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tMCY	DMA Cycle Time	52		MCY
tMA	$\overline{DACK}$ Delay Time from DMA High	0		ns
tAM	DMA Reset Delay Time from $\overline{DACK}$ Low		140	ns
tAA	$\overline{DACK}$ Width	125		ns
tMRW	$\overline{IOR}$ or $\overline{IOW}$ Response from DMA High		48	MCY
tMtMR	$\overline{IOR}$ Delay from DMA	0		ns
tMW	$\overline{IOW}$ Delay from DMA	0		ns
tRD	Data Access Time from $\overline{IOR}$ Low		120	ns
tDW	Data Set Up Time to $\overline{IOW}$ High	100		ns
tDF	DB to Float Delay from $\overline{IOR}$ High	10	80	ns
tWD	Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 4-5. FDC DMA TIMING SPECIFICATION

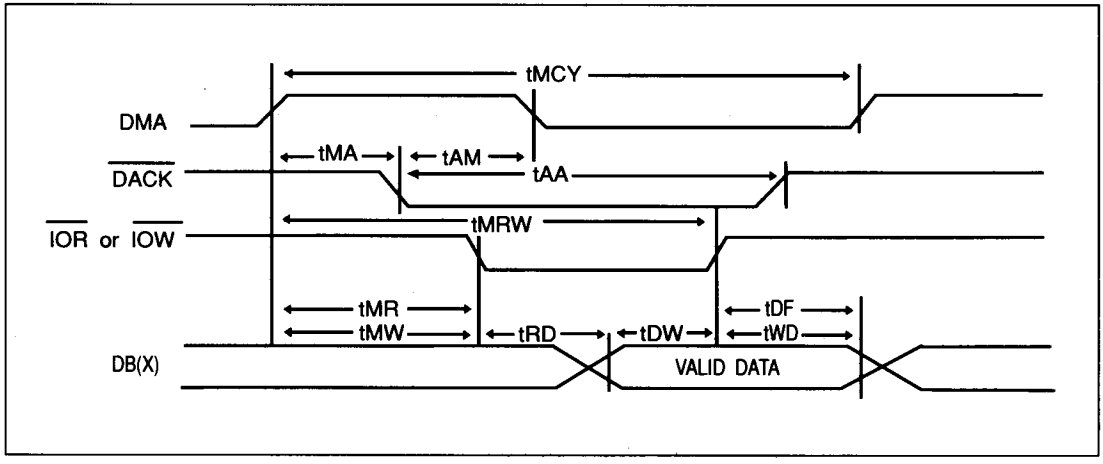


FIGURE 4-5. FDC DMA TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tTCR	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOR}$	0	192	MCY
tTCW	DACKEN, $\overline{CSEN}$ Delay from Last DMA or FIRQ, $\overline{IOW}$	0	384	MCY
tTC	DACKEN High, $\overline{CSEN}$ Low Pulse Width	60		ns
tTCA	DACKEN High, $\overline{CSEN}$ Low to TC Asserted	0	30	ns
tTCD	DACKEN Low, $\overline{CSEN}$ High to TC De-Asserted	0	30	ns

TABLE 4-6. FDC TERMINAL COUNT TIMING SPECIFICATION

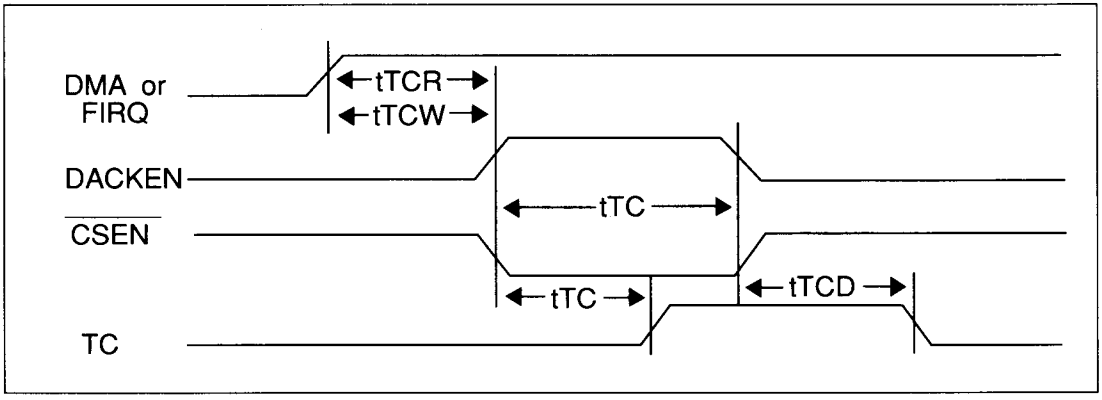


FIGURE 4-6. FDC TERMINAL COUNT TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCY	Clock Period	31		ns
tR	Clock Rise Time		2	ns
tF	Clock Fall Time		2	ns
tPH	Clock Active (High or Low)	13		ns

TABLE 4-7. FDC 32 MHZ CLOCK TIMING SPECIFICATION

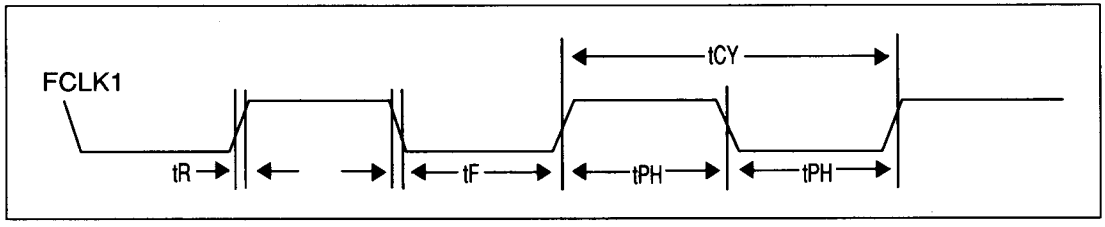


FIGURE 4-7. FDC 32 MHZ CLOCK TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tDST	$\overline{\text{DIRC}}$ Set Up to $\overline{\text{STEP}}$ Low	4		MCY
tSTP	STEP Active Time Low	24		MCY
tSTD	DIRC Hold Time from STEP High	96		MCY
tSC	STEP Cycle Time	132		MCY
tSTU	DS(x) Hold Time from STEP Low	20		MCY
tIDX	IDX Index Pulse Width	1		MCY
tRDD	RDD Active Time Low	40		ns
tWDD	WD Write Data Width Low	1/2		WCY

TABLE 4-8. FDC DISK DRIVE TIMING SPECIFICATION

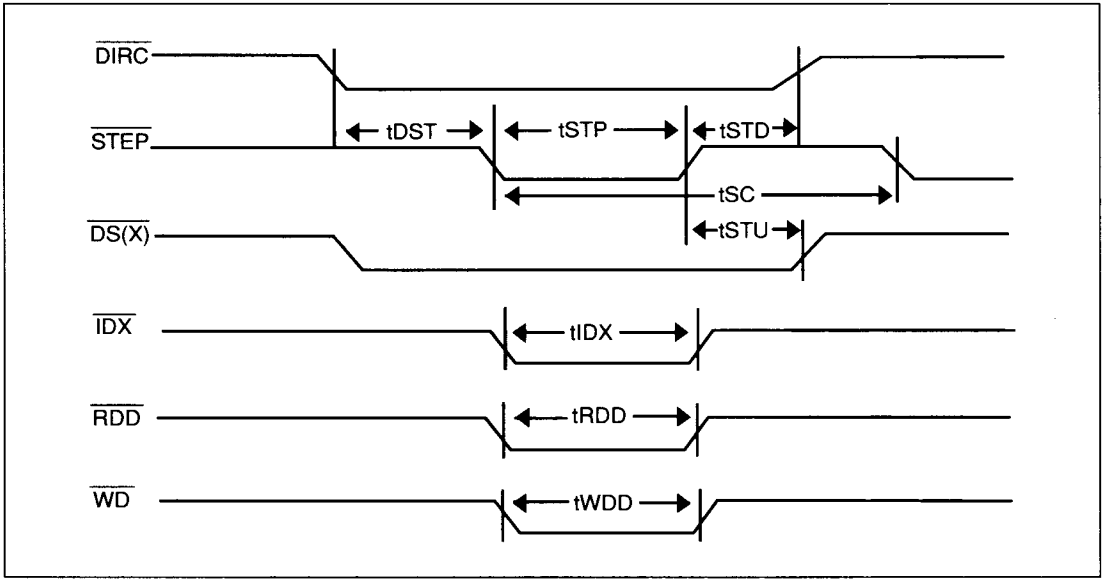


FIGURE 4-8. FDC DISK DRIVE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOR}$ Low	35		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOR}$ High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-9. RTC AND RAM READ TIMING SPECIFICATION

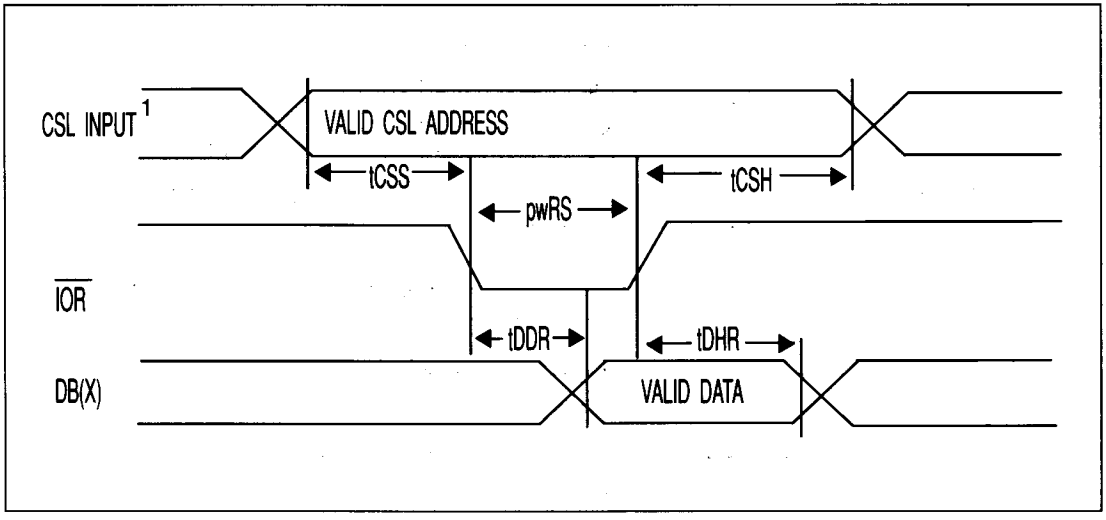


FIGURE 4-9. RTC AND RAM READ TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	35		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tDSW	Address or Data Setup Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 4-10. RTC AND RAM WRITE W/BALE TIMING SPECIFICATION

6

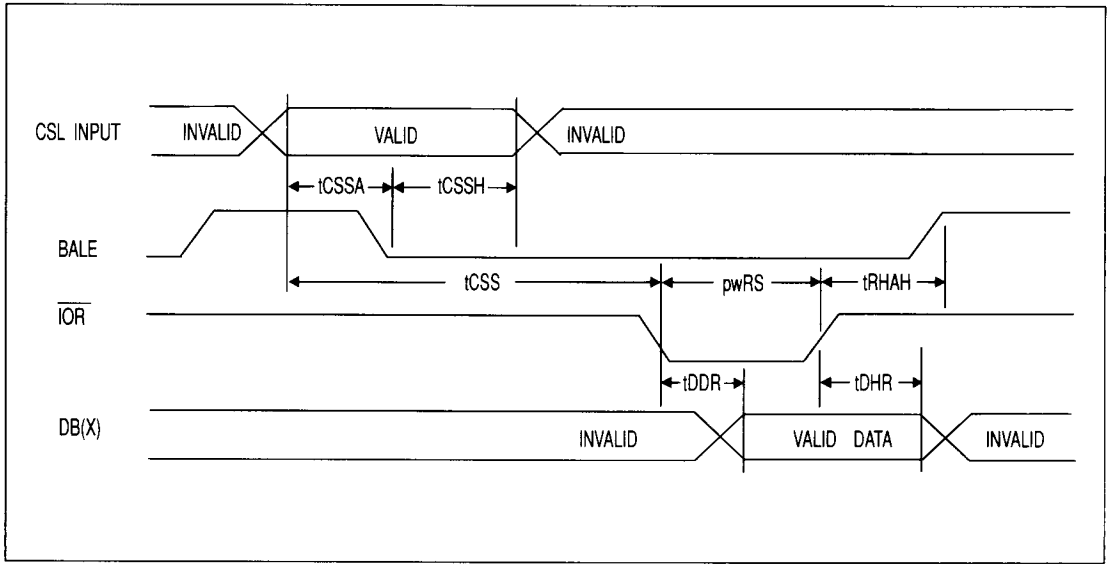


FIGURE 4-10. RTC AND RAM READ W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle $\overline{IOW}$ Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle $\overline{IOW}$ or $\overline{IOR}$ Low (not shown)	100		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IOW}$ Low	30		ns
pwWW	$\overline{IOW}$ Pulse Width	180		ns
tCSH	CSL Input Address[1] Hold Time from $\overline{IOW}$ High	10		ns
tDSW	Address or Data Set Up Time to $\overline{IOW}$ High	100		ns
tDHW	Address or Data Hold Time from $\overline{IOW}$ High	10		ns

TABLE 4-11. RTC AND RAM WRITE TIMING SPECIFICATION

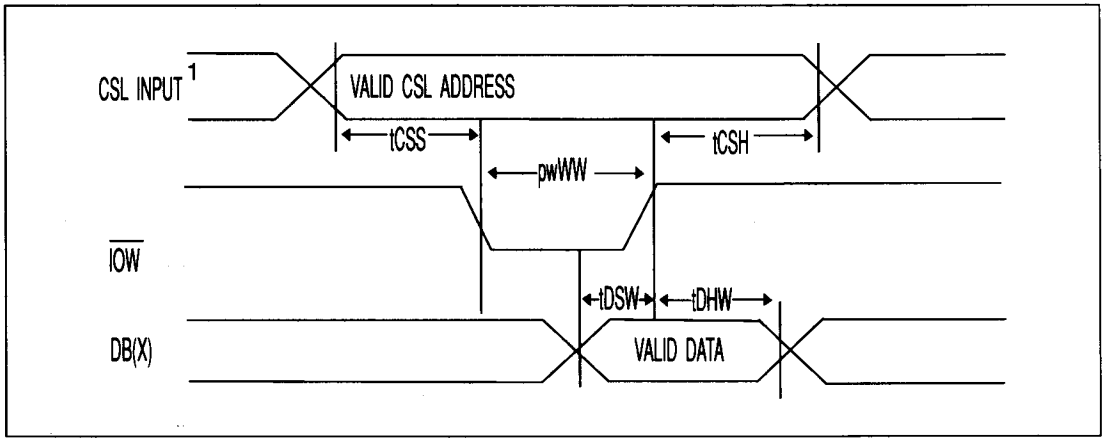


FIGURE 4-11. RTC AND RAM WRITE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tASD	Data Cycle $\overline{IOW}$ or $\overline{IOR}$ High to Address Cycle IOW Low (not shown)	100		ns
tASED	Address Cycle $\overline{IOW}$ High to Data Cycle IOW or IOR Low (not shown)	100		ns
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tcSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
pwRS	$\overline{IOR}$ Pulse Width	180		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tDDR	Data Access Time from $\overline{IOR}$ Low		175	ns
tDHR	DB(x) to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-12. RTC AND RAM READ W/BALE TIMING SPECIFICATION

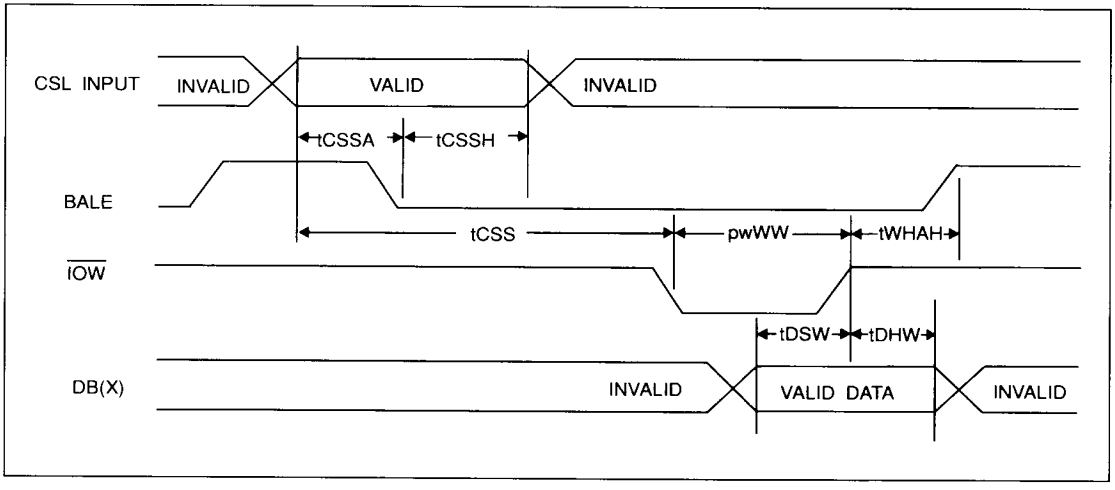


FIGURE 4-12. RTC AND RAM WRITE W/BALE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tRLIQ	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{IOR}}$ (Qualified by RECS)		2	µS
tRLIH	$\overline{\text{RTCIRQ}}$ Release from $\overline{\text{RESET}}$		2	µS

TABLE 4-13. RTCIRQ RELEASE TIMING SPECIFICATION

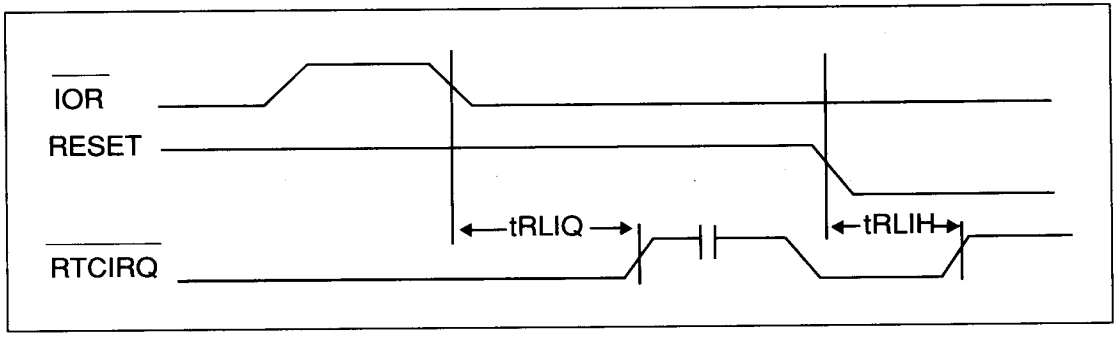


FIGURE 4-13. RTCIRQ RELEASE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tPRST	Power on Reset Width	200		ns
tRST	Reset Width	5		µS
tCA	Chip Access Delay from $\overline{\text{RESET}}$ High	32		MCY

TABLE 4-14. RESET TIMING SPECIFICATION

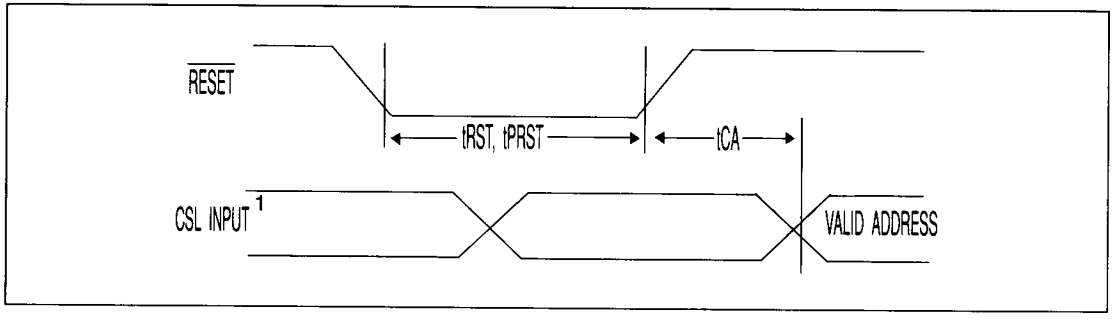


FIGURE 4-14. RESET TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tD7DR	D7 Access time from $\overline{IOR}$ low	0	20	ns
tD7D	Propagation Delay from IDED7 to DB7	0	20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-15. IDE INTERFACE TIMING (IDED7 TO DB7)

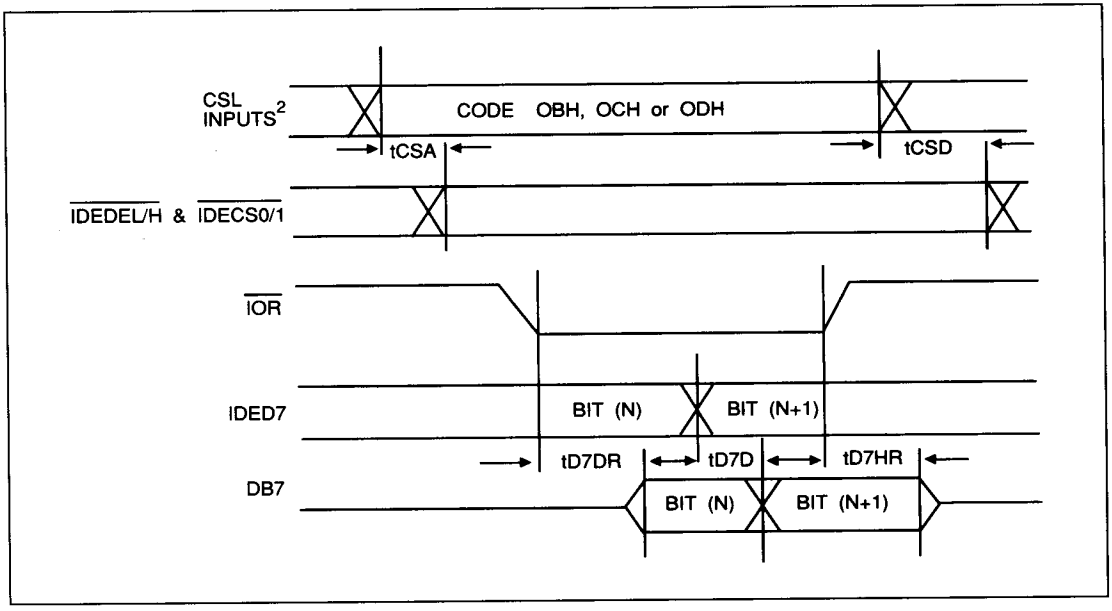


FIGURE 4-15. IDE INTERFACE TIMING DIAGRAM (IDED7 TO DB7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time from BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
tRHAH	$\overline{IOR}$ High to BALE High	10		ns
tD7DR	D7 Access Time from $\overline{IOR}$ Low	0	20	ns
tD7D	Propagation Delay from IDED7 to DB7	0	20	ns
tD7HR	DB7 to Float Delay from $\overline{IOR}$ High	10	80	ns

TABLE 4-16. IDE INTERFACE W/BALE TIMING (IDED7 TO DB7)

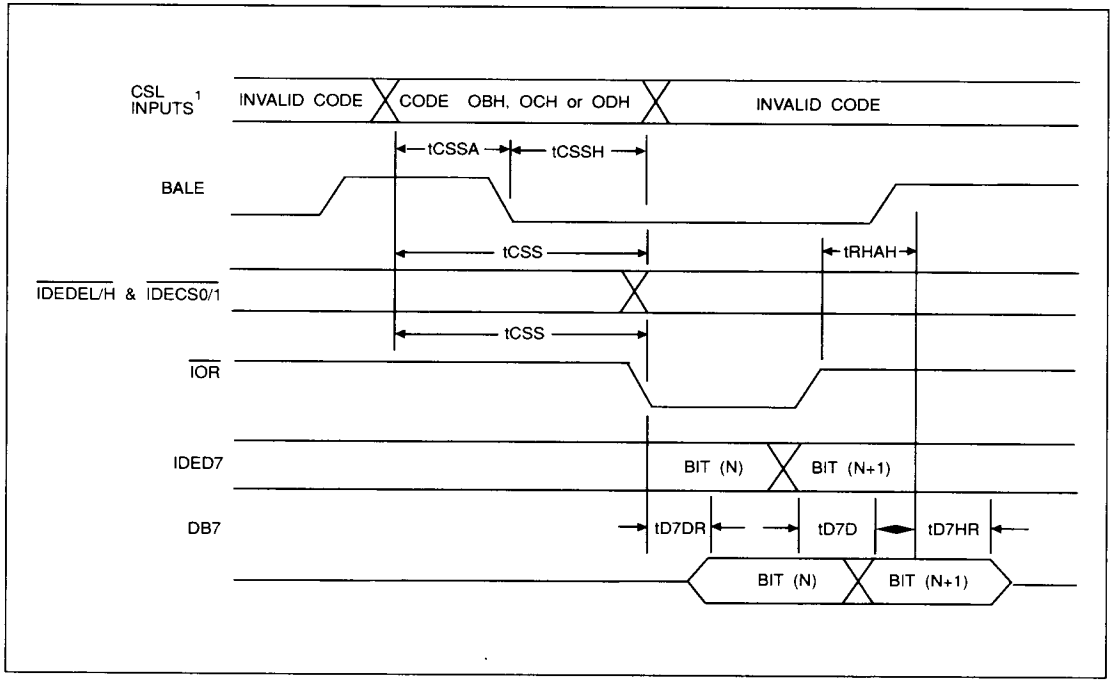


FIGURE 4-16. IDE INTERFACE W/BALE TIMING (IDED7 to DB7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input Valid to CSL Output Asserted		35	ns
tCSD	CSL Input Invalid to CSL Output De-Asserted		35	ns
tIDDR	IDED7 Access time from $\overline{IOW}$ low	0	20	ns
tIDD	Propagation Delay from DB7 to IDED7	0	40	ns
tIDHR	IDED7 to Float Delay from $\overline{IOR}$ high	20	160	ns

TABLE 4-17. IDE INTERFACE TIMING (DB7 TO IDED7)

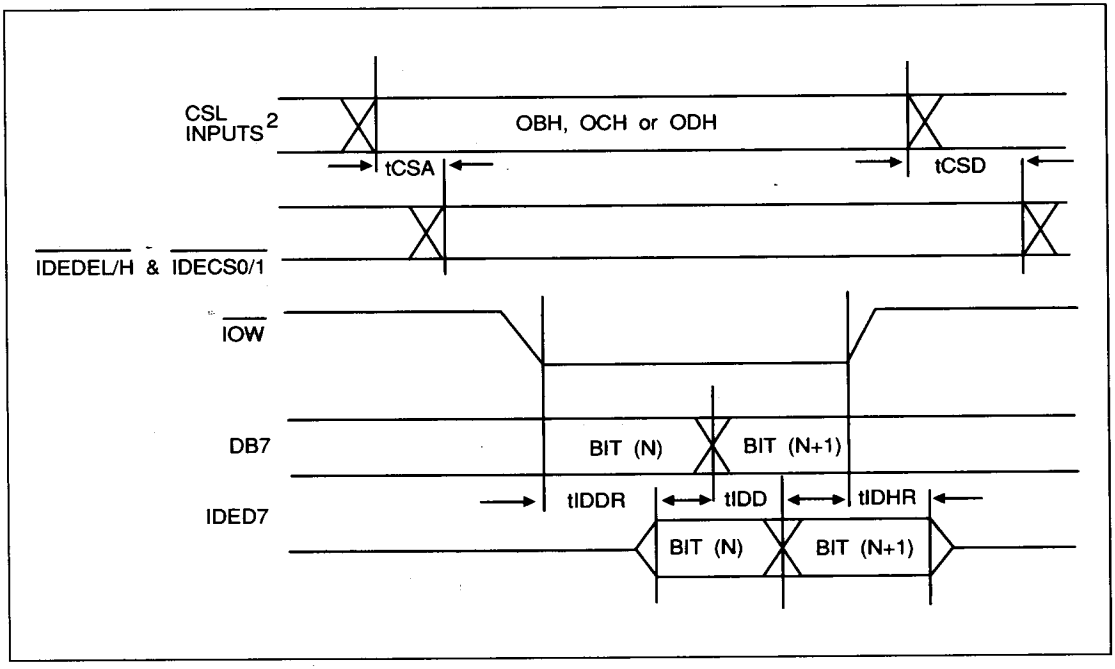


FIGURE 4-17. IDE INTERFACE TIMING (DB7 TO IDED7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[1] Set Up to BALE Low	10		ns
tCSSH	CSL Input Address[1] Hold Time From BALE Low	5		ns
tCSS	CSL Input Address[1] Set Up to $\overline{IO}$ Low	30		ns
tWHAH	$\overline{IOW}$ High to BALE High	10		ns
tIDDR	IDED7 Access time from $\overline{IOW}$ Low	0	20	ns
tIDHR	IDED7 to Float Delay from $\overline{IOR}$ High	20	160	ns

TABLE 4-18. IDE INTERFACE W/BALE TIMING (DB7 TO IDED7)

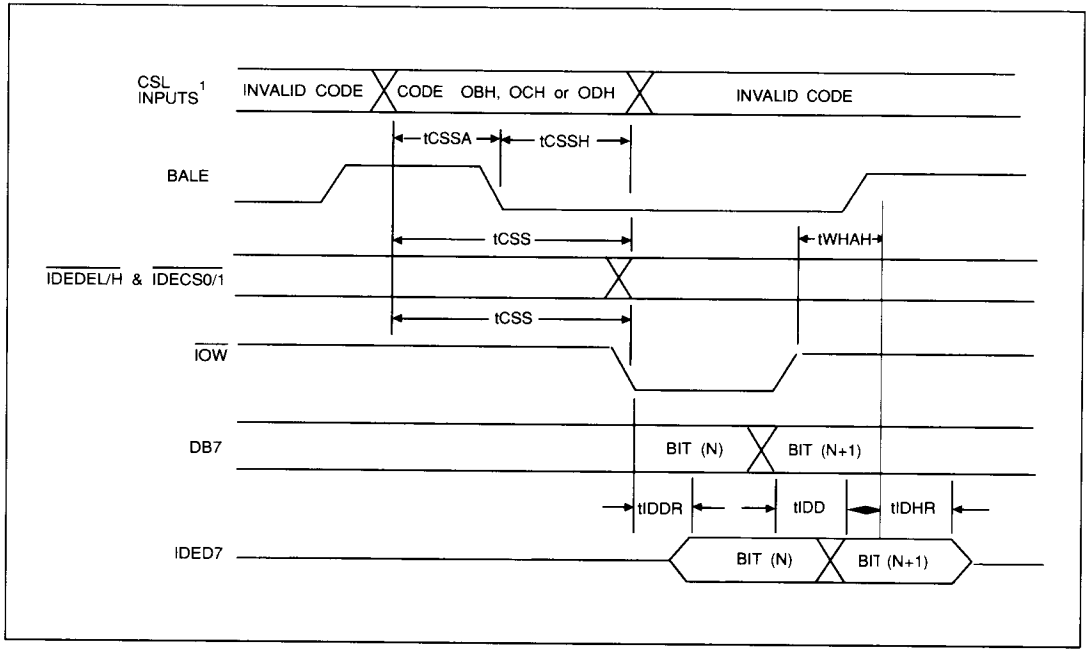


FIGURE 4-18. IDE INTERFACE W/BALE TIMING (DB7 to IDED7)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCWSS	CSL Input Valid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tCWSR	CSL Input Invalid and $\overline{IOW}$ Low to OSC Transition to Low	30		ns
tOSD	OSC Suspend Initiated to OSC Low Gap	60		µS
tOSL	OSC Low Gap	60		µS

TABLE 4-19. RESUME TO SUSPEND SUPPORT TIMING*

* Note: Code 15H can also be latched in with BALE as previously shown.

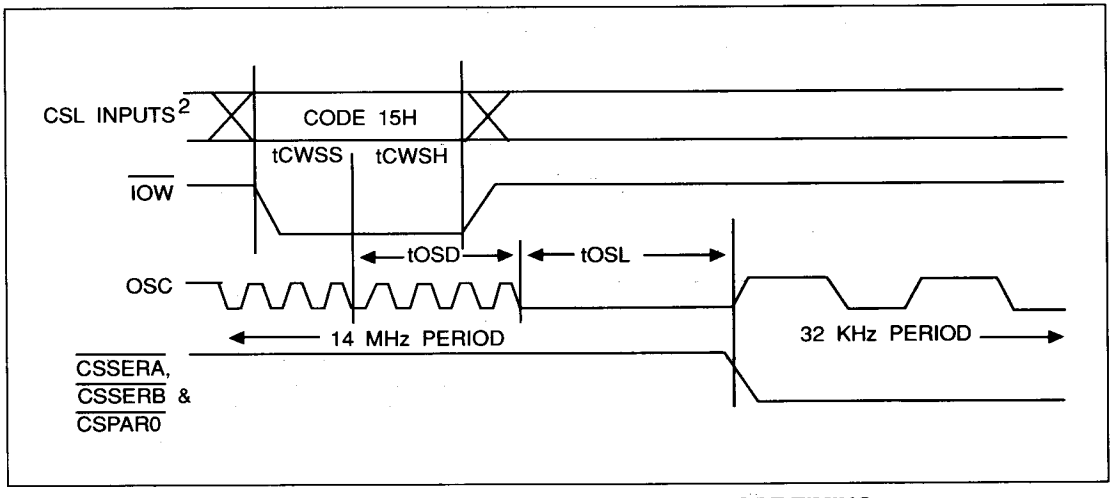


FIGURE 4-19. RESUME TO SUSPEND SUPPORT TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCRS	CSL Input Valid to OSC Transition to Low	30		ns
tCRH	CSL Input Invalid to OSC Transition to Low	30		ns
tCOR	CSL Output De-Assert to Resume WD76C30*	60	91	µs
tOTD	OSC Transition Delay (for XTAL warmup)*	500	501	ms

* CSL Code 16H is latched on the falling edge of OSC.

TABLE 4-20. SUSPEND TO RESUME SUPPORT TIMING

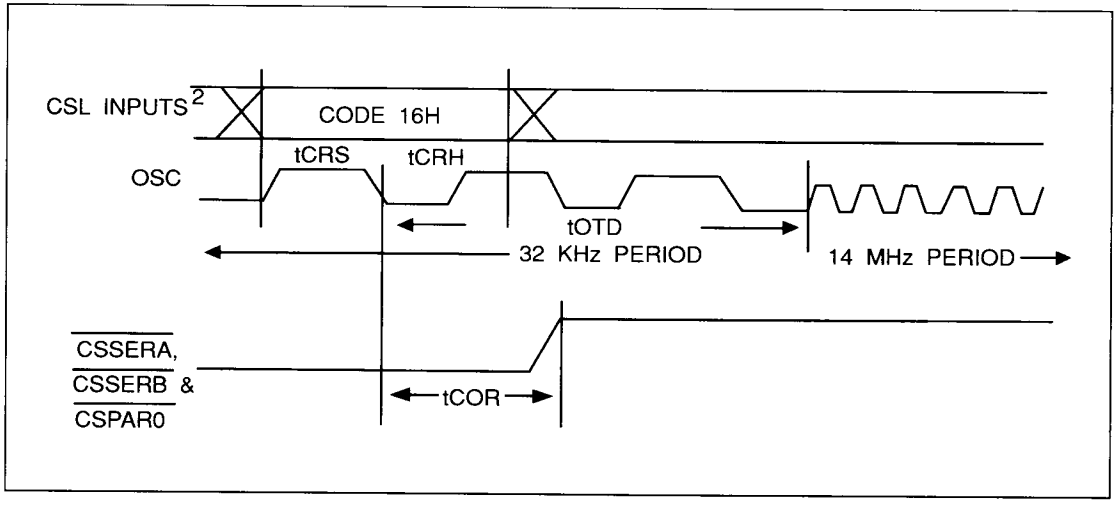


FIGURE 4-20. SUSPEND TO RESUME SUPPORT LOGIC

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSA	CSL Input[2] Valid to CSL Asserted		35	ns
tCSD	CSL Input[2] Invalid to CSL Output De-Asserted		35	ns
tCSH	CSL Input Address[2] Hold Time from $\overline{IOW}$ High	10		ns
tWLPH	$\overline{IOW}$ Low to PCUW0/1 High		35	ns
tWHPH	$\overline{IOW}$ High to PCUW0/1 Low		35	ns

TABLE 4-21. CHIP SELECT LOGIC DECODE TIMING SPECIFICATION

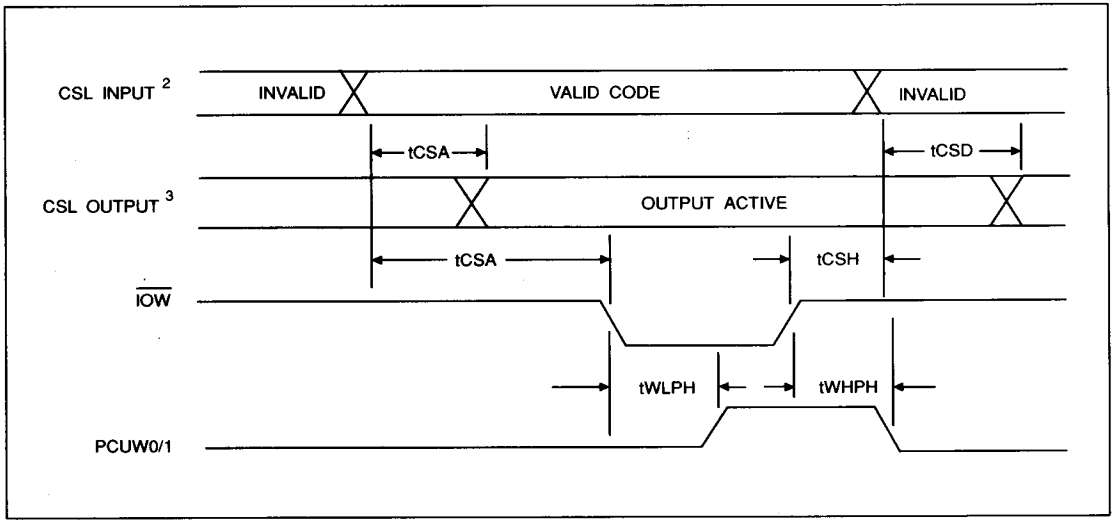


FIGURE 4-21. CHIP SELECT LOGIC DECODE TIMING DIAGRAM

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tCSSA	CSL Input Address[2] Set Up to BALE Low	10		ns
tCSSH	CSL Inpu Addresst[2] Hold Time from BALE Low	5		ns
tCSA	CSL Input Valid to Output[3]Asserted	35		ns

TABLE 4-22. CSL DECODE W/BALE TIMING SPECIFICATION

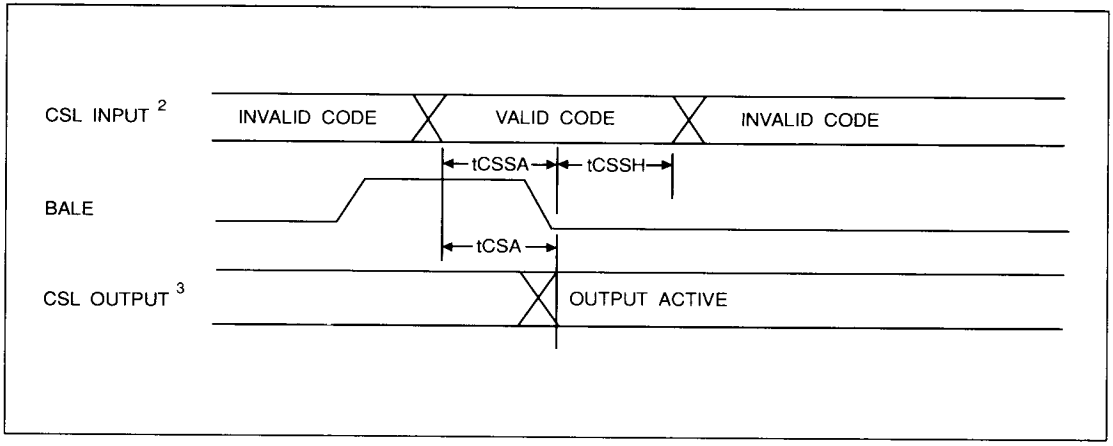


FIGURE 4-22. CHIP SELECT LOGIC DECODE W/BALE TIMING DIAGRAM

Notes

[1] The RTCALE and RTCCS are internal to the WD76C20 and are used by the RTC during I/O operations. The $\overline{CS}$, LDCR and LDOR are also internal to the WD76C20 and used by the FDC during I/O operations. CSL Inputs are decoded in Table 2-6 are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal. The general specification for generating the internal and external signals is presented in Table 4-21 and 4-22.

[2] CSL Inputs are decoded in Table 2-6 and are comprised of DPH, DPL, RA10, RA9 and RA8. All CSL Input Addresses are qualified by the CSEN signal as shown in Figure 4-21 and 4-22. Also included in this group is DACKEN which must be deasserted (logic=0) in order to allow the decoder to activate any signal other than TC, which is asserted (logic=1) when both DACKEN and CSEN are active.

[3] CSL outputs are control lines used both internally by the WD76C20 (FDC$\overline{CS}$, FDC $\overline{LDCR}$, FDC $\overline{LDOR}$, RTC $\overline{CS}$, and RTC AEN) and externally by other chips (IDEDENL, IDEDENH, CSIDE0, CSIDE1, CSSERA, $\overline{CSSERB}$, CSPAR0, ROMOE, 8042CS, NPCS, PCUW0, PCUW1, PROGCS, EMS and TC). For all but one case, only a single, decoded output is asserted at any given time and is unique as decoded in Table 2-6. Although not mentioned in Table 2-6, TC is asserted when both DACKEN and CSEN are active, as specified in Table 4-6.