

WESTERN DIGITAL CORP

54E D

9718228 0015236 724 WDC  
捷多邦, 专业PCB打样工厂, 24小时加急出货

T-SZ-38

*WD7625LP Address, Data,*

*Hard Disk Buffers and Power*

*Management Device*

 WESTERN DIGITAL

A



WESTERN DIGITAL CORP

54E D ■ 9718228 0015737 660 ■ WDC

T-52-38

Copyright © 1992 Western Digital Corporation  
All Rights Reserved

Information furnished by Western Digital Corporation is believed to be accurate and reliable. However, no responsibility is assumed by Western Digital Corporation for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Western Digital Corporation. Western Digital Corporation reserves the right to change specifications at any time without notice.

Western Digital, AutoSwitch, and Paradise are registered trademarks and CacheFlow, Caviar, FIT Lab, Hyperseek, Interarchitecture, PinScan, Piranha, SAM, Tidbit, and TrueShade are trademarks of Western Digital Corporation.

Other marks may be mentioned herein that belong to other companies.

**Western Digital Corporation**

Western Digital Plaza, 8105 Irvine Center Drive, Irvine, CA 92718

**For Service and Literature, call:**

(714) 932-4900

## TABLE OF CONTENTS

T-52-38

Section	Title	Page
1.0	INTRODUCTION . . . . .	1
	1.1 Document Scope . . . . .	1
	1.2 Address Buffer Features . . . . .	1
	1.3 Data Buffer Features . . . . .	1
	1.4 General Description . . . . .	1
2.0	ARCHITECTURE: ADDRESS BUFFER FUNCTION . . . . .	3
	2.1 AT Address Block . . . . .	3
	2.2 Power Management Input Multiplexer (PMGIN) . . . . .	3
	2.3 Power Management Control Register PMCR(0:15) . . . . .	4
	2.4 Suspend Resume Logic . . . . .	6
	2.5 WE Signal Buffering . . . . .	6
	2.6 Watchdog Timer . . . . .	6
	2.7 Chip Select Decoding for WD7625LP Data Buffer Function Registers . . . . .	6
	2.8 Power On Reset Generation From RSTSW Switch . . . . .	6
	2.9 Diagnostic Mode . . . . .	6
3.0	ARCHITECTURE: DATA BUFFER FUNCTION . . . . .	7
	3.1 AT Data Bus . . . . .	7
	3.2 DRQ Multiplexing and DACK Demultiplexing . . . . .	7
	3.3 SMEMR, SMEMW Signal Generation . . . . .	7
	3.4 IDE Data Bus Buffer Interface . . . . .	7
	3.5 General Purpose Registers . . . . .	7
	3.6 Mode Control Register . . . . .	9
	3.6.1 Input Control Signal . . . . .	9
4.0	STRAPPING OPTION INPUTS . . . . .	11
5.0	SIGNAL DESCRIPTION . . . . .	12
	5.1 Address Buffer Function, Mixed Mode Application . . . . .	12
	5.2 Address Buffer Function Signal Definition . . . . .	13
	5.3 Data Buffer Function, Mixed Mode Application . . . . .	18
	5.4 Data Buffer Function Signal Definition . . . . .	19
6.0	POWER SUPPLY MODES . . . . .	22
	6.1 Input Threshold Adjustment for Different Power Modes . . . . .	22
	6.2 Power Supply Consideration and System Power-Down Mode . . . . .	22



Section	Title	Page
7.0	DC ELECTRICAL SPECIFICATIONS . . . . .	23
7.1	Output Valid Times and Voltage Levels: Address Buffer Function . . . . .	23
7.2	Input Valid Times and Voltage Levels: Address Buffer Function . . . . .	24
7.3	Output Valid Times and Voltage Levels: Data Buffer Function . . . . .	25
7.4	Input Valid Voltage Levels and Setup Times: Data Buffer Function . . . . .	26
7.5	5.0 Volt Characteristics . . . . .	27
7.6	3.3 Volt Characteristics . . . . .	28
8.0	PACKAGE DIMENSIONS . . . . .	29
A.0	TEST METHODS	
A.1	Tristating the Outputs . . . . .	30
B.0	WD7625 PIN ORDER CROSS-REFERENCE . . . . .	31
C.0	INPUT THRESHOLD ADJUSTMENT . . . . .	36
D.0	I/O REQUIREMENTS . . . . .	37
D.1	Address Buffer Mode . . . . .	37
D.2	Data Buffer Mode . . . . .	40
E.0	SUSPEND/RESUME LOGIC SCHEMATICS . . . . .	42
F.0	REVISION HISTORY . . . . .	45
F.1	Initial Release x/x/92 . . . . .	45



## LIST OF ILLUSTRATIONS

T-52-38

Figure	Title	Page
2-1	WD7625LP Address Buffer Block Diagram . . . . .	5
3-1	WD7625LP Data Buffer Block Diagram . . . . .	8
5-1	WD7625LP 144-Pin Diagram . . . . .	12
5-2	WD7625LP 144-Pin Diagram . . . . .	18
8-1	WD7625LP Package Diagram . . . . .	29

## LIST OF TABLES

Table	Title	Page
2-1	Power Management Output Control Register PMCR(7:0) . . . . .	4
2-2	Power Management Output Control Register PMCR(15:8) . . . . .	4
2-3	Power Management Control (Combined) . . . . .	4
3-1	General Purpose Registers . . . . .	9
3-2	Mode Control Register Mode 1 and Mode 0 . . . . .	9
5-1	WD7625LP Pin Assignments (Address Buffer) . . . . .	12
5-2	Address Buffer Signal Description . . . . .	13
5-3	WD7625LP Pin Assignments (Data Buffer) . . . . .	18
5-4	Data Buffer Signal Description . . . . .	19
B-1	WD7625LP Pin Order Cross-Reference . . . . .	31
C-1	Input Threshold Adjustment . . . . .	36
D-1	I/O Requirements Address Buffer Mode . . . . .	37
D-2	I/O Requirements Data Buffer Mode . . . . .	40



**1.0 INTRODUCTION****1.1 DOCUMENT SCOPE**

This document describes the two separate functions: Address Buffer and Data Buffer available in the WD7625LP chip. A strapping input pin selects the Data Buffer Function when strapped low, otherwise it selects the Address Buffer Function.

**1.2 ADDRESS BUFFER FEATURES**

- Allows WD76C10A, WD7855, WD7710, and WD7910 based designs with WD7620/30 for laptop or notebook systems
- Will work in three different power supply modes:
  - 3.3V only
  - 5V only
  - Mix mode 3.3V and 5V
- Direct connect to AT Address Bus SA1:19 and LA17:23 with 24 mA drive
- Power Management Control (PMC) input MUX
- General purpose suspend/resume and power supply control logic
- Fifteen-bit Power Management Control (PMC) output register and control logic
- Low power request and resume signal delay simplify the design of the power supply
- Watchdog timer for system idle detection
- DRAM WE signal from WD7xC10 inversion and buffering
- $\overline{\text{RESIN}}$  output generation from reset switch (RSTSW)
- System Reset generation
- Chip select decoding for registers in the WD7625LP Data Buffer Function
- 144-pin SQFP package

**1.3 DATA BUFFER FEATURES**

- Allows WD76C10A, WD8110, WD7855, WD7710, and WD7910 based designs with WD7620/30 for laptop or notebook systems
- Will work in three different power supply modes:
  - 3.3V only
  - 5V only
  - Mix mode 3.3V and 5V
- Direct connection to AT data bus; 20K integrated pull-up for SD(0:7)
- Direct connection to IDE data bus
- Two general purpose 8-bit I/O registers:
  - Register A
  - Register B
- One general purpose 8-bit I/O Register C, with single bit set/reset control
- One general purpose 1-bit I/O Register Y0
- One 4-bit general purpose input only Register Z
- DRQ multiplexing plus 20K integrated pull-down
- DACK demultiplexing
- $\overline{\text{SMEMR}}$ ,  $\overline{\text{SMEMW}}$  signals plus 22K internal pull-up
- 144-pin SQFP package

**1.4 GENERAL DESCRIPTION**

The WD7625LP is a combination design which includes two separate functions: Address Buffer and Data Buffer in one chip. A strapping input pin selects the Data Buffer Function if it is strapped low; otherwise, it selects the Address Buffer Function. For designs that use both the data buffer and the address buffer functions, two WD7625LP devices are needed in the system.

In the Address Buffer Function, the WD7625LP is an address buffer and power management chip.

In the Data Buffer Function, the WD7625LP is a data buffer, IDE buffer and I/O register device for the WD7x00 16-bit chip sets.

**WD7625LP**

WESTERN DIGITAL CORP

54E D

When the WD7625LP functions in Address Buffer mode, it replaces 21 "glue"-logic devices in laptop designs with the WD76C20 and WD76C30.

CHIPS REPLACED	QUANTITY
74ACT573	4
74ACT244	3
74ACT151	1
74HC273	2
74ACT04	1
74HC74	2
74ACT04	1
74HC08	1
74ACT32	1
74ACT125	1
74HC04	1
74ACT14	1
74HC02	1
74HC4020	1
<b>TOTAL</b>	<b>21 ICS</b>

**INTRODUCTION**

■ 9718228 0015742 T28 ■ WDC

When the WD7625LP functions in the Data Buffer mode, it replaces 26 "glue"-logic devices in similar laptop designs.

CHIPS REPLACED	QUANTITY
74ACT245	9
74ACT373	5
74ACT244	4
74HC151	1
74ACT138	3
74ACT125	1
74ACT273	3
<b>TOTAL</b>	<b>26 ICS</b>



**2.0 ARCHITECTURE: ADDRESS BUFFER FUNCTION**

The following section describes the functions of the various internal blocks in the Address Buffer mode of the WD7625LP as a 144-pin device supporting 16-bit processors.

**2.1 AT ADDRESS BLOCK**

This block takes in A1:A23 from the processor and latches it internally with ALE and READY signals. MASTER, when high, drives the address on to SA1:SA19 and LA17:23. The buffers on the lines can drive 24 mA for compatibility with the AT address bus. When MASTER is low, the address from the AT bus is driven to A1:A23.

**2.2 POWER MANAGEMENT INPUT MULTIPLEXER (PMCIN) T-52-38**

This logic multiplexes the PMCIN signals with the help of MXCTL0:2 according to the following table.

MXCTL2:0			SIGNAL
0	0	0	TURBO
0	0	1	PROCPGD
0	1	0	LCL_REQ
0	1	1	RESUME
1	0	0	PMC(4)
1	0	1	SUSPREQ
1	1	0	PMC(6)
1	1	1	PMC(7)



**WD7625LP**

WESTERN DIGITAL CORP 54E D

**2.3 POWER MANAGEMENT CONTROL REGISTER PMCR(0:15)**

This is a 16-bit general purpose write only register for power management control. The PCUW0 control signal writes PMCR(0:7) and PCUW1 writes

**ARCHITECTURE: ADDRESS BUFFER FUNCTION**

9718228 0015744 8TO WDC  
 PMCR(8:15) bits. All bits (except Bit 0) of the PMCR are available on pins of the WD7625LP. A typical bit assignment for the PMCR register is shown in the tables below.

**T-52-38**

7	6	5	4	3	2	1	0
FULLPDN	PMCR6	PROCPDN	PMCR4	PMCR3	BLEN	LCDEN	Not Used
				LCLACK			

**TABLE 2-1. POWER MGMTMENT OUTPUT CONTROL REGISTER PMCR(7:0)**

15	14	13	12	11	10	9	8
PMCR15	PMCR14	PMCR13	IDEON	PMCR11	PMCR10	PMCR9	PMCR8
			PMCR12				

**TABLE 2-2. POWER MGMTMENT OUTPUT CONTROL REGISTER PMCR(15:8)**

PMC PIN	WD7X10 SIGNAL	S/W CTRL	WD7625 SIGNAL	INITIAL STATE
0	CPU Clk Driver Enable	N	N/A*	N/A
1	LCD Enable	opt./timer	LCDEN	L
2	Backlight Enable	opt./timer	BLEN	H**
3	LCL_ACK	N	LCL_ACK	L
4	LCL_ATN	N	PMCR4	L
5	Processor Power Down	N	PROCPDN	L
6	Gate A20	N	PMCR6	L
7	Full Power Down	N	FULLPDN	L
8	User Defined	Y	PMCR8	L
9	User Defined	Y	VGADN	H**
10	User Defined	Y	PMCR10	L
11	User Defined	Y	PMCR11	L
12	User Defined	Y	IDEON	L
13	User Defined	Y	PMCR13	L
14	User Defined	Y	PMCR14	L
15	User Defined	Y	PMCR15	L

**TABLE 2-3. POWER MANAGEMENT CONTROL (COMBINED)**

\* The 7x10 supports a hardware strap option in place of DRQ4 on the DRQ input multiplexer. This selects whether the CPUCLK pin on the 7x10 is an input or output. If configured as an input, PCMR0(CPU Clock Driver Enable) can be used to change the output mode. PMCR0 tristates the external clock oscillator. In practice, however, no design ever configured CPUCLK as an input. Therefore support for this option was dropped in the WD7625LP so that the PMCR0 pin could be used for other purposes. Thus, PMCR0 is not brought out to a pin in this device.

\*\* Note that these outputs have opposite initial polarity from the previous discrete implementation.



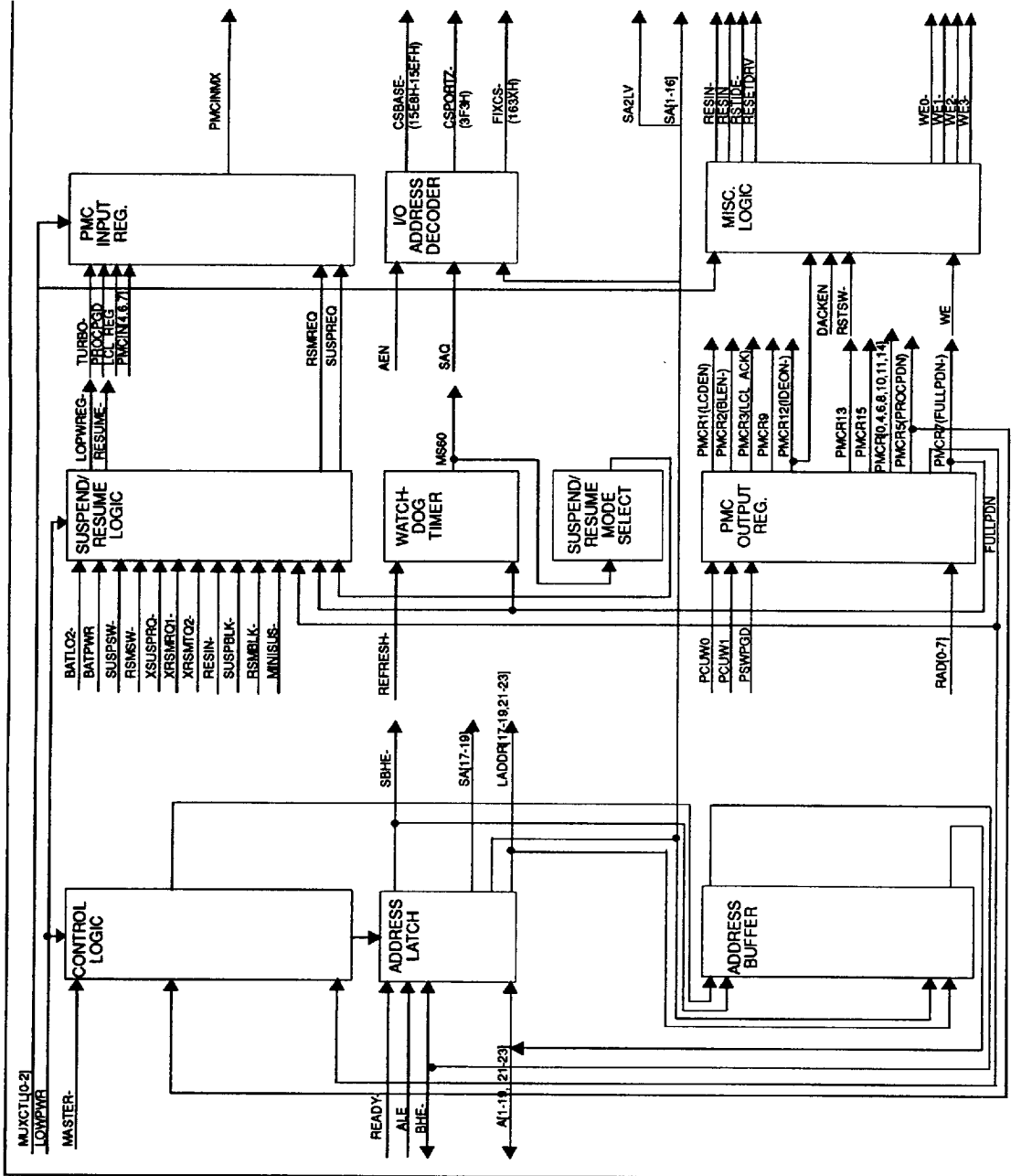


FIGURE 2-1. WD7625LP ADDRESS BUFFER BLOCK DIAGRAM

**WD7625LP**

WESTERN DIGITAL CORP

54E D

**ARCHITECTURE: ADDRESS BUFFER FUNCTION**

9718228 0015746 673 WDC

**2.4 SUSPEND/RESUME LOGIC**

The suspend/resume logic supports two modes of the circuit. The two modes differ in the way the Suspend/Resume switch is used. One mode allows the switch to be used as a momentary switch to generate Suspend and Resume requests. The other mode allows a two position single-pole, double-throw switch to be used to indicate a lid open or closed condition. The circuits provide all signals necessary for automatically generating suspend/resume requests depending upon signals from the battery and also generate Low Power Request signals to put the power supply in low power mode. See the block diagrams of both modes. The Strap input option generates the signal SRMODESEL which selects one of the two modes.

For a power supply which does not provide a LOWPWR output pin, this input pin to the WD7625LP needs to be tied to ground.

**2.5 WE SIGNAL BUFFERING**

The WD7625LP takes in an active high WE signal from the WD7610A and drives four active low write enable signals for the DRAM banks. WE0, WE1, WE2 and WE3 are designed to drive high capacitance loads of 150 pf. Each can handle two banks of DRAMs.

**2.6 WATCHDOG TIMER**

The watchdog timer is used to detect system inactivity. It is clocked with a refresh signal and generates a 120 millisecond elapsed signal which can be connected to an unused PMCIN mux input. During suspend, this watchdog timer is halted.

The watchdog timer signal is only need with the WD76C10A and similar devices. The WD7855 and new devices do not require a watchdog timer.

**2.7 CHIP SELECT DECODING FOR WD7625LP DATA BUFFER FUNCTION REGISTERS**

The chip select decoding generates a chip select base I/O address for the general purpose registers in the WD7625LP Data Buffer Function. The CSBASE (15E8H to 15EFH) is further decoded inside the WD7625LP Data Buffer Function along with SA0, SA1, SA2. The CSPORTZ is another fixed chip select (03F3H) for the register in the WD7625LP Data Buffer Function. FIXCS is decoded for the address range of 1630H to 163FH.

**2.8 POWER ON RESET GENERATION FROM RSTSW SWITCH**

The RSTSW signal has a Schmitt trigger input on the Reset Switch and generates all the active low and active high resets needed in the system.

**2.9 DIAGNOSTIC MODE**

If PMCR[15:8] is set to AA, 55, and AA in coincidence with three reads or writes at address 9872H, the WD7625LP Address Buffer Function is set to diagnostic mode. In this mode eight internal signals can be read at output pin PMCIN as shown in the following table.

MXCTL2:0			SIGNAL
0	0	0	RSMCLK
0	0	1	SUSPCLK
0	1	0	RSUSPRQ
0	1	1	RSMREQ
1	0	0	SUSPCLR
1	0	1	RSMCLR
1	1	0	SCAN
1	1	1	LOWPREQ

See the appendix for further testing information.

Note: the diggnostic mode is for in-house testing only.



## ARCHITECTURE: DATA BUFFER FUNCTION

WESTERN DIGITAL CORP

54E D ■ 9718228 0015747 50T ■ WDC

**3.0 ARCHITECTURE: DATA BUFFER FUNCTION**

The following section describes the functions of the various internal blocks in the Data Buffer Function of the WD7625LP as a 144-pin device supporting 16-bit processors.

**3.1 AT DATA BUS**

This block takes in D0:15 from the processor and connects it to the SD0:15 AT data bus, the IDE data bus, and the other general purpose registers internally. The buffers on the SD0:15 lines can drive 24 mA for compatibility with an AT address bus. The low order byte SD0:7 has an internal pull-up.

**3.2 DRQ MULTIPLEXING AND DACK DEMULTIPLEXING**

The WD7625LP Data Buffer Function multiplexes the DRQ signals onto DRQIN with MXCTL0:2 signals. Together with the DACKEN signal, the MXCTL0:2 signals are demultiplexed onto the DACK0:3 DACK5:7 signals. The following tables show the multiplexer assignments.

MXCTL2:0			DRQIN SIGNAL
0	0	0	DRQ0
0	0	1	DRQ1
0	1	0	DRQ2
0	1	1	DRQ3
1	0	0	Logic Low
1	0	1	DRQ5
1	1	0	DRQ6
1	1	1	DRQ7

MXCTL2:0			DACK SIGNAL
0	0	0	DACK0
0	0	1	DACK1
0	1	0	DACK2
0	1	1	DACK3
1	0	0	NA
1	0	1	DACK5
1	1	0	DACK6
1	1	1	DACK7

**3.3 SMEMR, SMEMW SIGNAL GENERATION**

This logic takes in LOWMEG, MEMR, and MEMW signals. Whenever LOWMEG is low, either SMEMR or SMEMW is driven low depending upon the MEMR or the MEMW signals. The SMEMR and SMEMW signals support a 24 mA drive and can be directly connected to an AT bus.

**3.4 IDE DATA BUS BUFFER INTERFACE**

The IDE data buffer connects the CPU data bus to the IDE data bus and is controlled by the IDE DENL and IDE DENH signals. IDE Bit 7 is muxing with the Disk Change signal of the floppy controller inside the WD7621 and is accessible through bit SD7.

**3.5 GENERAL PURPOSE REGISTERS**

There are four general purpose registers in the WD7625LP Data Buffer Function. Three of them, Register A, Register B, and Register C are 8-bit I/O registers. Register C also has an individual Set/Reset control. Register Y is a 1-bit I/O register.

Register Z is a 4-bit input only register.

There is a mode control register which selects different modes for A and B ports. The mode control register is described in the next section.



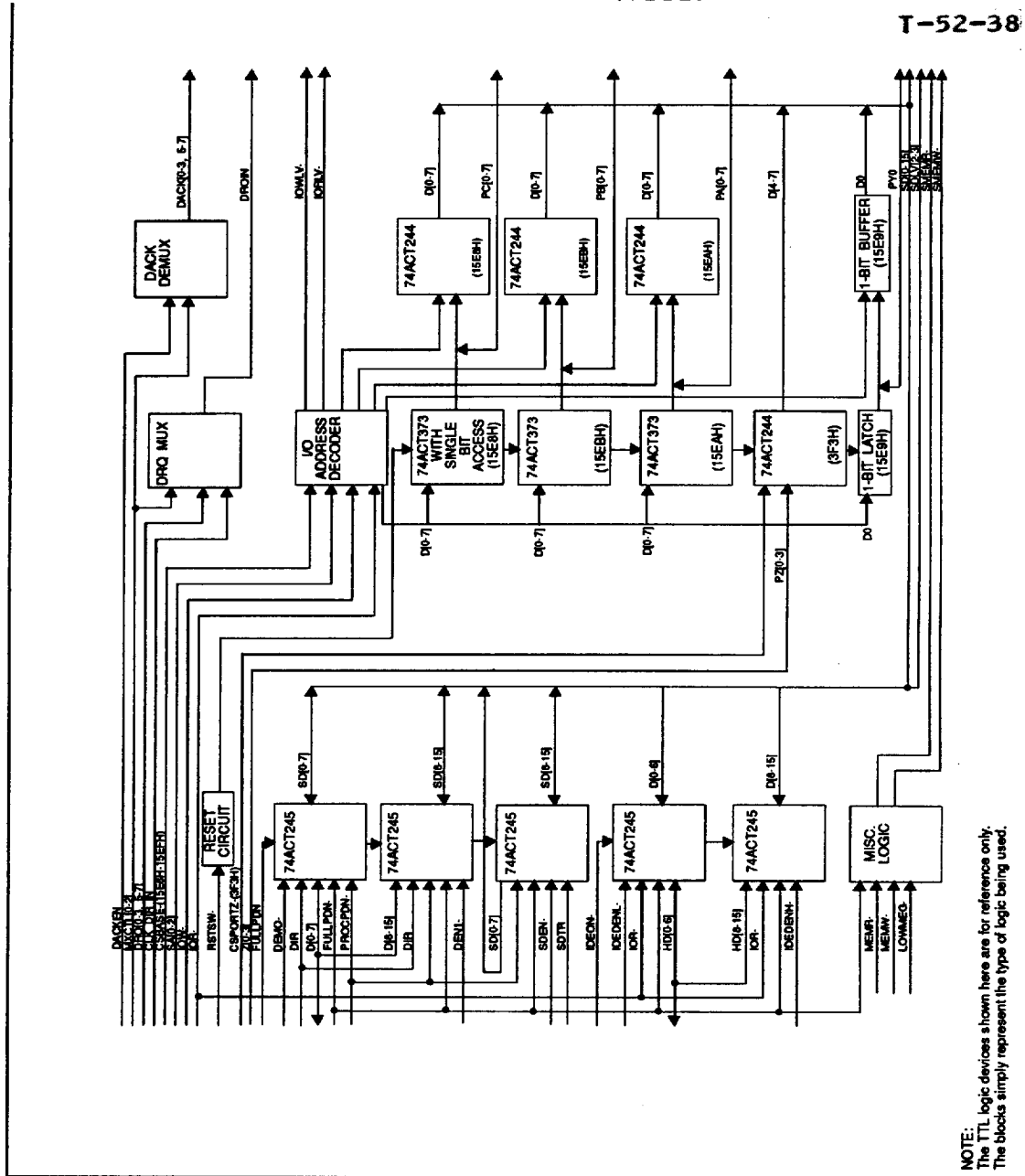


FIGURE 3-1. WD7625LP DATA BUFFER FUNCTION BLOCK DIAGRAM

NOTE:  
The TTL logic devices shown here are for reference only.  
The blocks simply represent the type of logic being used.



WESTERN DIGITAL CORP

54E D ■ 9718228 0015749 382 ■ WDC

REGISTER	CSBASE	SA2	SA1	SA0
Mode Control Write Only (15EC)	0	1	0	0
Bit Set/Reset Control-Register C (15ED)	0	1	0	1
Reserved	0	1	1	0
Reserved	0	1	1	1
Register Y Read/Write (15E9)	0	0	0	1
Register A Read / Write (15EA)	0	0	1	0
Register B Read / Write (15EB)	0	0	1	1
Register C Read / Write (15E8)	0	0	0	0

TABLE 3-1. GENERAL PURPOSE REGISTERS

Port Z address is fixed at 03F3H.

### 3.6 MODE CONTROL REGISTER

MOD1	MOD0	L1H3	T1	DIR Y	DIR C	DIR B	DIR A
------	------	------	----	-------	-------	-------	-------

Bit T1 is the test bit used for fault coverage testing only. Always set this bit to zero when writing this register.

**MODE 0:** Simple Input/Output mode. All registers A, B, C, and Y are in normal read/write mode and the port pins can be programmed as input or output pins with DIR Y, DIR C, DIR B, and DIR A control bits in the control register. The outputs on the ports are latched and driven onto the pins continuously. The inputs are not latched and directly come from the input pins of the port.

**MODE 1:** In this mode, Port A (address 15EA) can be programmed as a strobed input or output mode. This configuration provides a means of transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In this mode Port A uses four lines from Port C PC(0:3) for handshaking.

**L1H3:** This bit serves the same function as the primary input pin 141 FSAD in the Address Buffer mode. It is used to control the buffer strength of the SD output buffers. On power up reset, this bit is cleared to logic 0, which reduces the SD output buffers to approximately 3/5ths of their maximum strength. By setting this bit to logic 1, the full buffer strength will be achieved. This method of buffer strength setting is very useful in controlling ground bounce and signals overshooting in minimum loaded laptop systems.

#### 3.6.1 Input Control Signal

**STB:** Strobe Input: A low on this input loads data into an input latch. STBA (Port C, Bit 0) and STBB (Port C, Bit 4) are bits defined for Port A and Port B.

**IBF:** Input buffer full: A high on this output indicates that the data has been loaded into the input latch. IBF is set when the STB input is low and is reset by the rising edge of the IOR signal on the same port. IBFA (Port C, Bit 1) and IBFB (Port C, Bit 5).

MOD 1	MOD 0	MOD #	CONDITION
0	0	Mode 0	Normal Mode
0	1	Mode 1	Strobed Input or Output Port A
1	0	Mode 2	Strobed Input or Output Port B
1	1	Mode 3	Both Port A and Port B are Strobed I or O

TABLE 3-2. MODE CONTROL REGISTER MODE 1 AND MODE 0



**OB̄F:** Output buffer full: The  $\overline{\text{OB}}\text{F}$  output goes low to indicate that the CPU has written data to the port. The  $\overline{\text{OB}}\text{F}$  flip-flop is set low by the  $\overline{\text{IOW}}$  signal to the port and is set high when the  $\overline{\text{ACK}}$  input is low.  $\overline{\text{OBFA}}$  (Port C, Bit 2) and  $\overline{\text{OBFB}}$  (Port C, Bit 6).

**ACK:** Acknowledge input: A low on this input means that data from the port has been accepted by the device.  $\overline{\text{ACKA}}$  (Port C, Bit 3) and  $\overline{\text{ACKB}}$  (Port C, Bit 7).

During Mode 1: The Port C bits are as defined above and the DIR C bit in the control word is applicable to the upper nibble only. A read on Port C reflects the following

I/O	I/O	I/O	I/O	$\overline{\text{ACKA}}$	$\overline{\text{OBFA}}$	IBFA	$\overline{\text{STBA}}$
-----	-----	-----	-----	--------------------------	--------------------------	------	--------------------------

**MODE 2:** In this mode, Port B (address 15EB) can be programmed as a strobed input or output mode. This configuration provides a means of transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In this mode Port B uses four lines from Port C PC(4:7) for handshaking.

During Mode 2: The Port C bits are as defined above and the DIR C bit in the control word affects only the lower nibble. A read on Port C reflects the following

$\overline{\text{ACKB}}$	$\overline{\text{OBFB}}$	IBFB	$\overline{\text{STBB}}$	I/O	I/O	I/O	I/O
--------------------------	--------------------------	------	--------------------------	-----	-----	-----	-----

**MODE 3:** Both Port A and Port B are programmed for strobed I/O mode and all bits in Port C are used for control signals for both ports as defined in Mode 1 and Mode 2.

$\overline{\text{ACKB}}$	$\overline{\text{OBFB}}$	IBFB	$\overline{\text{STBB}}$	$\overline{\text{ACKA}}$	$\overline{\text{OBFA}}$	IBFA	$\overline{\text{STBA}}$
--------------------------	--------------------------	------	--------------------------	--------------------------	--------------------------	------	--------------------------

**Port Y** (address 15E9) always operates in Mode 0 regardless of bits MOD0 and MOD1 in the Mode Control Register. The system will read in Port Y0 through data bits D0. A "0" at DIR Y indicates that Port Y is in input mode.

9718228 0015750 0T4 WDC  
The following table shows the direction control bits in mode control. T-52-38

C	B	A	PORT C	PORT B	PORT A
0	0	0	Input	Input	Input
0	0	1	Input	Input	Output
0	1	0	Input	Output	Input
0	1	1	Input	Output	Output
1	0	0	Output	Input	Input
1	0	1	Output	Input	Output
1	1	0	Output	Output	Input
1	1	1	Output	Output	Output

#### BIT SET/RESET CONTROL FOR PORT C:

There are two ways of programming Port C's bits. One is normal read/write where all eight bits of Port C are written by writing to the port Base address.

The Port C bits can also be written one bit at a time by writing to the port Base + 5 address. The following is the data format for port Base + 5 address:

X	X	X	X	Data B*	BA2	BA1	BA0
---	---	---	---	---------	-----	-----	-----

\*DATA B is the data being written to a bit as addressed by BA2:0.

If DATA B = 1, the bit is set. If DATA B = 0 the bit is reset.

During Mode 0, all bits 0:7 of Port C can be used for the Bit Set/Reset Function. During Mode 1 or Mode 2, only those bits which are not used for control signals are available for this function.



**4.0 STRAPPING OPTION INPUTS**

T-52-38

The WD7625LP operates in two different functions and with up to three voltage supply modes. Therefore it is necessary to select the function in which the chip operates and to provide information to the input/output buffers for the appropriate threshold adjustments required because of the different VDD values.

The WD7625LP has six strapping options. Three of the options are mode specific:

- Two of the options are for the Address Buffer Function mode only. These two options select:
  - the Suspend/Resume mode required
  - the buffer strength of the SA and LA buses
- Another option is for the Data Buffer Function mode only. This option adjusts the threshold of the hard disk I/O buffers along with the voltage supplied to the IDE.

- The other three options are:<sup>1</sup>
  - Function Address/Data Buffer mode select
  - 3.3V only mode
  - 5 V only mode

All strapping inputs except the buffer strength select are monitored during power-up reset, and are latched when reset goes away. The strapping input for the buffer strength select is dynamic. If any strapping pin is left unconnected, the input will evaluate high due to an internal pull-up device. The internal pull-up is only active during Reset except for the buffer strength strap.

The table below illustrates all the allowed settings for the strapping signals.

<sup>1</sup> Driving the 3.3 V only and 5 V only straps both low is an illegal combination. The WD7625LP assumes a mixed voltage scenario when both of these straps are allow to float to high.

The 3.3 V only mode is not allowed with a 5 V hard disk supply.

To select logic low (0), a 5K to 15K external pull-down resistor is required for each strapping input.

SIGNAL PINS	LOGIC STATE LOW (0)	LOGIC STATE HIGH (1)
Pin 67 (CSBASE)	All VDDs are 3.3V	Mixed mode supply, if pin 66 is high
Pin 66 (CSPORTZ)	All VDDs are 5V	Mixed mode supply, if pin 67 is high
Pin 63 (SA2LV/IORLV)	Select Data Buffer Function	Select Address Buffer Function
Pin 70 (SD2LV) (Data Buffer mode only)	VDDHD is 3.3V	VDDHD is 5V
Pin 141 (FSAD) (Address Buffer mode only)	Select full strength of SA and LA buffers	Select 3/5 strength of SA and LA buffers
Pin 113 (MS120) (Address Buffer mode only)	Use momentary switch type for suspend - resume	Use lid switch type for suspend - resume



**WD7625LP**

WESTERN DIGITAL CORP

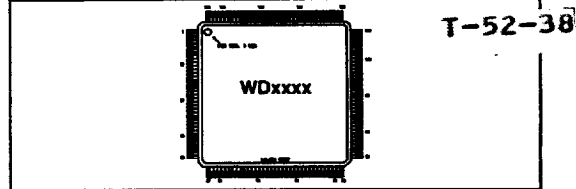
54E D

9718228 0015752 977 WDC

**5.0 SIGNAL DESCRIPTION**
**5.1 ADDRESS BUFFER FUNCTION, MIXED MODE APPLICATION**

In 5V or 3.3V only applications all VDD5 and VDD3 signals are tied to the same power supply plane. In mixed mode applications two different kinds of power supply pins, VDD3 and VDD5 are used. The normal signal pins stay unaffected.

## SIGNAL DESCRIPTION


**FIGURE 5-1. 144-PIN DIAGRAM**

Signals = 122 VDD5 = 3 VDD3 = 7 GND = 12

PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-PMCR8	37-SA11	73-XRSMRQ1	109-A21
2-PMCR10	38-SA12	74-XRSMRQ2	110-A22
3-PMCR11	39-SA13	75-XRSMRQ3	111-A23
4-PMCR14	40-SA14	76-RSTSW	112-BHE
5-ALE	41-SA15	77-READY	113-MS120
6-WE	42-SA16	78-VSS	114-SUSPBLK
7-VSS	43-VSS	79-SUSPSW	115-RSMBLK
8-LCDEN	44-SA17	80-RSMSW	116-MINISUS
9-BLEN	45-SA18	81-MXCTL0	117-P5VPGD
10-LCL_ACK	46-SA19	82-MXCTL1	118-VDD5
11-VDD3	47-VDD5	83-MXCTL2	119-RAD0
12-PMCR9	48-SBHE	84-VDD3	120-VDD3
13-IDEON/PMCR12	49-VSS	85-DACKEN	121-RAD1
14-RSTIDE	50-RESET	86-RESIN	122-RAD2
15-VDD3	51-LA17	87-VSS	123-RAD3
16-WE0	52-LA18	88-A1	124-RAD4
17-WE1	53-LA19	89-A2	125-RAD5
18-WE2	54-LA21	90-A3	126-RAD6
19-WE3	55-LA22	91-A4	127-RAD7
20-PMCR13	56-LA23	92-A5	128-PCUW0
21-PMCR15	57-VSS	93-A6	129-PCUW1
22-PROCPDN	58-SA0	94-A7	130-TURBO
23-RESIN	59-MASTER	95-A8	131-VSS
24-VSS	60-AEN	96-A9	132-PROCPGD
25-SA1	61-REFRESH	97-VDD3	133-LCL_REQ
26-SA2	62-VSS	98-A10	134-PMCIN4
27-SA3	63-SA2LV	99-A11	135-PMCIN6
28-SA4	64-LOWPREQ	100-A12	136-PMCIN7
29-SA5	65-PMCINMX	101-A13	137-LOWPWR
30-VSS	66-CSPORTZ	102-A14	138-RESUME
31-SA6	67-CSBASE	103-A15	139-FIXCS
32-VDD5	68-VDD3	104-A16	140-VSS
33-SA7	69-BATPWR	105-VSS	141-FSAD
34-SA8	70-BATLO2	106-A17	142-VDD3
35-SA9	71-FULLPDN	107-A18	143-PMCR4
36-SA10	72-XSUSRO	108-A19	144-PMCR6

**TABLE 5-1. WD7625LP PIN ASSIGNMENTS (ADDRESS BUFFER)**


PIN	MNEMONIC	I/O	DESCRIPTION
32, 47, 118	VDD5		5V power inputs.
68, 84, 120, 142, 11, 15	VDD3		3.3V power inputs.
24, 30, 43, 49, 57, 62, 78, 87, 105, 131, 140, 7	VSS		Ground pins.
85	DACKEN	I	<b>DACK Enable</b> DACK enable input.
130	TURBO	I	<b>TURBO</b> TURBO switch input. Connected to the PMCIN multiplexer Bit 0.
132	PROCPGD	I	<b>Processor Power Good</b> Processor Power Good signal indicating that power has been applied to the CPU and it has reached acceptable levels. Connected to the PMCIN multiplexer Bit 1.
133	LCL_REQ	I	<b>Local Access Request</b> Local Access Request from Keyboard controller. Connected to PMCIN mux Bit 2.
134 135 136	PMCIN4 PMCIN6 PMCIN7	I	<b>Power Management Control Inputs 4, 6, and 7</b> General Purpose input for the PMCIN multiplexer connected to bits 4, 6, and 7.
113	MS120	I/O	<b>120 Millisecond Watchdog Timer Strobe</b> Output for the watchdog timer MS120 signal. At power-up, this pin is an input whose state determines whether a lid switch type or a momentary switch type will activate the internal suspend/resume circuitry. See Strapping Options Inputs section for details.
65	PMCINMX	O	<b>Power Management Control Input Multiplexed</b> This is the output of the PMCIN signals multiplexed with MXCTL0:2. Goes directly to the PMCIN pin of the WD7610.
67	CSBASE	I/O	<b>Chip Select Base</b> The active low Base Chip Select for the general purpose R/W registers of the WD7625LP Data Buffer Function. At Reset, this pin is an input whose state determines whether the chip will operate in a 3.3V system or mixed mode. See Strapping Options Inputs section for details.

TABLE 5-2. ADDRESS BUFFER SIGNAL DESCRIPTION

PIN	MNEMONIC	I/O	DESCRIPTION
66	CSPORTZ	O	<b>Chip Select Port Z</b> Active chip selects for read only Port Z in the WD7625LP Data Buffer Function. At power on reset, this pin is an input whose state determines whether the chip will operate in a 5V system or mixed mode. See Strapping Options Inputs section for details
8 9 10 143 22 144 71 1 12 2 3 13 20 4 21	LCDEN BLEN LCL_ACK/ PMCR3 PMCR4 PROCPDN PMCR6 FULLPDN PMCR8 PMCR9 PMCR10 PMCR11 IDEON/ PMCR12 PMCR13 PMCR14 PMCR15	O	<b>Power Management Control Register Outputs</b> These are general purpose outputs of the Power Management Control Register (PMCR[0:15]). All the bits of the PMCR are available on the pins of the WD7625LP. Since the clock direction is always tied low internally, the output to PMCR0 for OSC control is omitted. LCDEN is the output for PMCR1;  RSTIDE (pin 14) output is gated by PMCR12/IDEON.
128 129	PCUW0 PCUW1	I	<b>Power Control Unit Write Strobe 0 and 1</b> Control signal to clock PMCR Register Bits 0:7 and 8:15 as generated by the WD76C20ALV.
112 88-96, 98-104, 106-111	BHE A1-19 A21-23	I/O	<b>Bus High Enable</b> <b>CPU Address 1 to 19</b> <b>CPU Address 21 to 23</b> Input from the CPU or DMA when MASTER is high. The CPU address bus A1:19, A21:23 and BHE are directly connected to these pins. The address bus is latched and output onto LA17:23 and SA1:19.
48 25-29, 31, 33-42	SBHE SA1-16	I/O	<b>System Bus High Enable</b> <b>System Address 1 to 16</b> Output to AT address bus when MASTER is high. A1:19, A21:23 and BHE are latched internally with ALE and driven onto these pins.
44-46	SA17-19	O	<b>System Address 17 to 19</b> Output AT address bus in non-master mode.

TABLE 5-2. ADDRESS BUFFER SIGNAL DESCRIPTION (CONTINUED)



PIN	MNEMONIC	I/O	DESCRIPTION
51-53, 54-56	LA17-19 LA21-23	I/O	<b>Early Address 17 to 19</b> <b>Early Address 21 to 23</b> Output when <b>MASTER</b> is high. A17-A19 and A21-23 are latched with <b>READY</b> signal when low. If <b>MASTER</b> is low, LA17:19, LA21:23 are input and are driven onto A17:19, A21:23.
77 149 59	<b>READY</b> <b>ALE</b> <b>MASTER</b>	I	<b>Ready</b> <b>Address Latch Enable</b> <b>Master</b> Control Signals for latching and output enable for latches for the AT Address Bus.
80	<b>RSMSW</b>	I	<b>Resume Switch</b> Resume switch input.
72 73 74 75	<b>XSPREQ</b> <b>XRSMRQ1</b> <b>XRSMRQ2</b> <b>XRSMRQ3</b>	I	<b>External Suspend Request</b> <b>External Resume Request</b> External suspend request and external resume request. These pins are used in the Suspend/Resume circuit.
114 115	<b>SUSPBLK</b> <b>RSMBLK</b>	I	<b>Suspend Request Circuit Block</b> <b>Resume Request Circuit Block</b> These general purpose signals are used in the suspend request circuit to block a suspend request or a resume request from the external circuit, if required.
64	<b>LOWPREQ</b>	I	<b>Low Power Request</b> Active low output from the suspend resume circuit requesting the power supply to go into low power mode.
69 70	<b>BATPWR</b> <b>BATLO2</b>	I	<b>Battery Power</b> <b>Battery Power Low</b> Inputs to the Suspend/Resume circuitry from the power supply indicating when battery power is being used and if the battery power is low.
81 82 83	<b>MXCTL0</b> <b>MXCTL1</b> <b>MXCTL2</b>	I	<b>Multiplexer Control 0, 1 and 2</b> PMCIN multiplexer control inputs.
116	<b>MINISUS</b>	I	<b>Mini Suspend</b> When active enables resume request flip-flop signal. A toggle also clears the Suspend/Resume D-flip-flops.
16 17 18 19	<b>WE0</b> <b>WE1</b> <b>WE2</b> <b>WE3</b>	O O O O	<b>Write Enable 0, 1, 2 and 3</b> Active low buffered DRAM Write signal. One signal for each bank. Each can drive 150 pf.
117	<b>P5VPGD</b>	I	<b>Power to 5V Power Good</b> Indicates that power to the 5V power bus is stable.

TABLE 5-2. ADDRESS BUFFER SIGNAL DESCRIPTION (CONTINUED)

PIN	MNEMONIC	I/O	DESCRIPTION
119 121-127	RAD0:7	I	<b>RAM Address Bus</b> RAD0:7 input bus for writing into the PMCR Register.
6	WE	I	<b>Write Enable</b> Active high WE signal from the WD76C10A for DRAM write. Generates WE0:3.
23 84	RESIN RESIN	O	<b>System Reset Output</b> Active low RESIN and active high RESIN power on reset signals. Generated from the RSTSW input signal.
14	RSTIDE	O	<b>Reset IDE</b> Open drain Reset IDE signal; it is tristated when PMCR12/IDEON is a one. Must only be pulled up to the lower voltage of a mixed mode setup to avoid latchup.
76	RSTSW	I	<b>Reset Switch</b> Active low Schmitt trigger input for generating power on reset signals.
50	RESET	O	<b>Reset Drive</b> AT bus active high reset.
58	SA0	I	<b>System Address 0</b> SA0 input for address decoding.
139	FIXCS	O	<b>External Chip Select</b> I/O address chip select for address 1630H to 163FH.
137	LOWPWR	I	<b>Low Power</b> Indicates to the system address buffer and suspend resume logic that the system power modules are in low power mode. For a system that does not provide this signal, this pin needs to be tied to ground; otherwise, the internal delay circuit for the system resume will not work properly.
61	REFRESH	I	<b>Refresh</b> System refresh signal. It is used by the watchdog timer for system idle detection.
60	AEN	I	<b>Address Enable</b> System AEN signal. Used in address decode of internal address registers.
63	SA2LV	I/O	<b>System Address 2 Low Voltage</b> 3.3V SA2 address output interface with the H8-330. At RESET, this pin is an input whose state determines whether the chip operates in Address Buffer Function or Data Buffer Function. See Strapping Options Inputs section for details.

TABLE 5-2. ADDRESS BUFFER SIGNAL DESCRIPTION (CONTINUED)



PIN	MNEMONIC	I/O	DESCRIPTION	T-52-38
138	RESUME	O	<b>Resume</b> Output indicating that the system is in resume mode. It is used to wake-up the keyboard controller on resume. Reflects the current state of the PCU input 3.	
79	SUSPSW	I	<b>Suspend Switch</b> Suspend switch input.	
141	FSAD	I	<b>Full Strength Address Buffer Control</b> This input is used to drive the SA and the LA output buffers to 3/5 strength or full strength. If this pin is floating, the internal pull-up will make it logic 1, which will select the 3/5 strength mode. If it is being pulled down externally through a 15K resistor, the full strength mode is selected.	

TABLE 5-2. ADDRESS BUFFER SIGNAL DESCRIPTION (CONTINUED)

**WD7625LP**

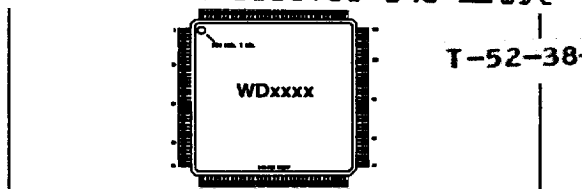
WESTERN DIGITAL CORP

54E D

9718228 0015758 395 WDC

**5.3 DATA BUFFER FUNCTION, MIXED MODE APPLICATION**

 Signals = 122 VSS = 12 VDD5V = 4  
 VDD3V = 4 VDDHD = 2

**SIGNAL DESCRIPTION**

**FIGURE 5-2. 144-PIN DIAGRAM**

PIN-NAME	PIN-NAME	PIN-NAME	PIN-NAME
1-HD3	37-SD10	73-DEN0	109-PA3
2-HD4	38-SD11	74-DEN1	110-PA4
3-HD5	39-SD12	75-SDEN	111-PA5
4-HD6	40-SD13	76-RESIN	112-PA6
5-HD8	41-SD14	77-SDTR	113-PA7
6-HD9	42-SD15	78-VSS	114-PZ0
7-VSS	43-VSS	79-IDEENL	115-PZ1
8-HD10	44-DACK1	80-IDEENH	116-PZ2
9-HD11	45-DACK2	81-MXCTL0	117-PZ3
10-HD12	46-DACK3	82-MXCTL1	118-VDD5
11-VDDHD	47-VDD5	83-MXCTL2	119-PB0
12-HD13	48-DRQ3	84-VDD3	120-VDD3
13-HD14	49-VSS	85-DACKEN	121-PB1
14-HD15	50-SMEMW	86-DTR	122-PB2
15-VDD5	51-DRQ0	87-VSS	123-PB3
16-DACK0	52-DRQ1	88-D0	124-PB4
17-DACK5	53-DRQ2	89-D1	125-PB5
18-DACK6	54-DRQ5	90-D2	126-PB6
19-DACK7	55-DRQ6	91-D3	127-PB7
20-SA0	56-DRQ7	92-D4	128-PC0
21-SA1	57-VSS	93-D5	129-PC1
22-SA2	58-IOR	94-D6	130-PC2
23-SMEMR	59-IOW	95-D7	131-VSS
24-VSS	60-MEMR	96-D8	132-PC3
25-SD0	61-MEMW	97-VDD3	133-PC4
26-SD1	62-VSS	98-D9	134-PC5
27-SD2	63-IORLV	99-D10	135-PC6
28-SD3	64-IOWLV	100-D11	136-PC7
29-SD4	65-DRQIN	101-D12	137-PY0
30-VSS	66-CSPORTZ	102-D13	138-IDEON
31-SD5	67-CSBASE	103-D14	139-PROCPDN
32-VDD5	68-VDD3	104-D15	140-VSS
33-SD6	69-SDLV2	105-VSS	141-HD0
34-SD7	70-SDLV3	106-PA0	142-VDDHD
35-SD8	71-FULLPDN	107-PA1	143-HD1
36-SD9	72-LOWMEG	108-PA2	144-HD2

**TABLE 5-3. WD7625LP PIN ASSIGNMENTS (DATA BUFFER)**


WESTERN DIGITAL CORP

54E D

9718228 0015759 221 WDC

5.4 DATA BUFFER FUNCTION SIGNAL  
DEFINITION

T-52-38

PIN	MNEMONIC	I/O	DESCRIPTION
25-29 31 33-42	SD(0:15)	I/O	<b>System Data Bus</b> 16-bit AT data bus.
71	FULLPDN	I	<b>Full Power Down</b> Full Power Down signal from the PMCR Register. Used to isolate input pads from input pins and control programmable pull-down resistors.
70 71	SD2LV SD3LV	O I/O	<b>Low Voltage SD2, SD3</b> These are 3V translated outputs for the Video Clock Generator chip. At power on, SD3LV is an input whose state determines whether the hard disk runs at 3.3V or 5V.
73 74 86	DEN0 DEN1 DTR	I	<b>Data Bus Enable 0</b> <b>Data Bus Enable 1</b> <b>Direction Control</b> Data Enable and Direction control signals for an AT data bus.
75 77	SDEN SDTR	I	<b>Swap Data Enable</b> <b>Swap Direction</b> Swap data enable and swap direction signals for an AT data bus.
88-96 98-104	D(0:15)	I/O	<b>Data Bus</b> 16-bit CPU data bus.
141 143-144 1-6 8-10 12-14	HD(0:6) HD(8:15)	I/O	<b>Hard Disk Data Bus</b> 15-bit IDE data bus.
79 80	IDEENL IDEENH	I	<b>IDE Low Byte Enable</b> <b>IDE High Byte Enable</b> IDE data bus enable control signals.
51 52 53 48 54 55 56	DRQ0 DRQ1 DRQ2 DRQ3 DRQ5 DRQ6 DRQ7	I I I I I I I	<b>DMA Requests (0-3, 5:7)</b> DRQ inputs, to be multiplexed onto DRQIN. These signals have internal pull-down.
65	DRQIN	O	<b>Multiplexed DRQ</b> This outputs the multiplexed DRQ0:7.

TABLE 5-4. DATA BUFFER SIGNAL DESCRIPTION





PIN	MNEMONIC	I/O	DESCRIPTION
81 82 83	MXCTL0 MXCTL1 MXCTL2	I	<b>Multiplexer Control 0, 1 and 2</b> Control signals for Multiplexing and Demultiplexing of DRQ signals and DACK signals.
128-130 132-136	PC(0:7)	I/O	<b>General Purpose Port C</b> Signals from the general purpose read write 8-bit register (address 15E8). These bits can be set/reset individually.
106-113	PA(0:7)	I/O	<b>General Purpose Port A</b> 8-bit general purpose R/W register (address 15EA).
119 102-127	PB(0:7)	I/O	<b>General Purpose Port B</b> 8-bit general purpose R/W register (address 15EB).
114-117	PZ(0:3)	I	<b>Register Z</b> 4-bit input only register inputs (address 3F3, bits 4-7).
137	PY0	I/O	<b>Register Y0</b> 1-bit general purpose R/W register (address 15E9, bit 0).
138	IDEON	I	<b>IDE Power On</b> Input indicating that the IDE has power on. This signal is used to tristate the IDE buffers during IDE power down. If this signal is not used to indicate IDE power on, then this pin should be pulled low.
139	PROCPDN	I	<b>Processor Power Down</b> Input indicating that the processor is powered down. This signal when active will tristate and isolate the D bus.
67 20 21 22	$\overline{\text{CSBASE}}$ SA0 SA1 SA2	I	<b>Chip Select Base</b> <b>System Address 0, 1 and 2</b> Fully decoded chip selects for general purpose registers in the Data Buffer Function. $\overline{\text{CSBASE}}$ is a base chip select and all internal registers are decoded with SA0, SA1, and SA2. At power on, $\overline{\text{CSBASE}}$ is an input whose state determines whether the WD7625LP operates in 3.3V mode or mixed voltage mode. See Strapping Options Inputs section for details.
66	$\overline{\text{CSPORTZ}}$	I	<b>Chip Select Port Z</b> $\overline{\text{CSPORTZ}}$ is chip select for Port Z. At power on, $\overline{\text{CSPORTZ}}$ is an input whose state determines whether the WD7625LP runs in a 5V system. See Strapping Options Inputs section for details.
72 60 61	$\overline{\text{LOWMEG}}$ MEMR MEMW	I	<b>First Megabyte</b> <b>Memory Read</b> <b>Memory Write</b> Inputs for generating $\overline{\text{SMEMR}}$ , $\overline{\text{SMEMW}}$ .
23 50	$\overline{\text{SMEMR}}$ $\overline{\text{SMEMW}}$	O	<b>System Memory Read</b> <b>System Memory Write</b> Active low memory control signals of the AT bus.

TABLE 5-4. DATA BUFFER SIGNAL DESCRIPTION (CONTINUED)



PIN	MNEMONIC	I/O	DESCRIPTION
76	$\overline{\text{RESIN}}$	I	<b>Reset Input</b> Active low power on reset input. This input buffer has a Schmitt trigger input.
58 59	$\overline{\text{IOR}}$ $\overline{\text{IOW}}$	I	<b>I/O Read</b> <b>I/O Write</b> AT bus IO read and write signals.
64 63	$\overline{\text{IOWLV}}$ $\overline{\text{IORLV}}$	O I/O	<b>I/O Write Low Voltage</b> <b>I/O Read Low Voltage</b> 3.3V translated $\overline{\text{IOW}}$ , $\overline{\text{IOR}}$ . At power on, $\overline{\text{IORLV}}$ is an input whose state determines whether the WD7625LP operates in Address Buffer or Data Buffer mode.
85	DACKEN	I	<b>DACK Enable</b> DACKEN input, together with MXCTL0:2 demultiplexes the DACK.
16 44-46 17-18 19	$\overline{\text{DACK0}}$ $\overline{\text{DACK1:3}}$ $\overline{\text{DACK5:6}}$ $\overline{\text{DACK7}}$	O O	<b>DACK0-DACK7 Outputs</b> DACK0 through DACK7 outputs.
24, 30, 53, 49, 58, 62, 78, 87, 105, 131, 140, 7	VSS		Ground inputs.
30, 47, 118, 15	VDD5		4 pins.
68, 84, 97, 120	VDD3		4 pins. In 5V mode the VDD3 are tied to the 5V supply.
141, 11	VDDHD		2 pins. These are connected to the 5V or 3.3V supply depending on whether the IDE subsystem is running at 5V or 3.3V.

TABLE 5-4. DATA BUFFER SIGNAL DESCRIPTION (CONTINUED)

## 6.0 POWER SUPPLY MODES

The WD7625LP is design to operate in three different power supply modes:

- 3.3V
- 5V
- 3.3/5V mix mode

In the laptop design mix mode environment the WD7625LP still operates properly when the 5V supply is switched to 3.3V in suspend mode.

In mixed mode, all supply pins must be connected to the correct supply. In single power supply mode, all supply pins either connect to 5V or 3.3V.

### 6.1 INPUT THRESHOLD ADJUSTMENT FOR DIFFERENT POWER MODES

Input thresholds are automatically compensated through 3.3V and 5V strap option decode logic. If neither a 3.3V nor a 5V strap is active, then the mixed mode adjustments are made. The strap op-

tion pin settings and the connections to the power supplies must agree; otherwise errors can result.

### 6.2 POWER SUPPLY CONSIDERATION AND SYSTEM POWER-DOWN MODE

The core of the WD7625LP will run at the higher (5V) VDD in a mixed mode for better performance. The signals coming from the 3.3 volt subsystem are received by the 3.3 volt buffers inside the WD7625LP and signals going out to the 3.3 volt system are translated to the 3.3 volt buffers. During system power-down mode, the A1:15 and D0:15 buses are isolated from the IO pads and inputs to the chip core are forced inactive. Similarly the IDE data bus HD(0:6,8:15) is isolated. The output buses SA1:19, LA17:23, SD0:15 and other output signals are tristated. The WD7625LP chip is always powered up with both 3.3 volt and 5 volt supplies in mixed mode. In suspend, the 5 volt supply can drop to 3.3 volts without any negative effect to the WD7625LV's operation.



**7.0 DC ELECTRICAL SPECIFICATIONS****7.1 OUTPUT VALID TIMES AND VOLTAGE LEVELS: ADDRESS BUFFER FUNCTION**

T-52-38

The signal voltage levels in the following tables illustrate the voltage levels in mixed mode.

SIGNAL	REFERENCE	CAPLOAD	I <sub>OL</sub> +I <sub>OH</sub>	VOLTAGE	DELAY
SA1:19 SBHE SA2LV	ALE falling edge	200 pf	+24 mA -3 mA ±2 mA	5V 3.3V	40 ns
LA17:23	READY low	200 pf	+24 mA -3 mA	5V	40 ns
A1:23 BHE	SA1:16, LA17:23	100 pf	+4 mA -1 mA	3.3V	35 ns
PMCR(1:15)	PCUW0 PCUW1	50 pf	+2 mA -2 mA	3.3V	25 ns
PMCINMX	MXCTL0:2	50 pf	+2 mA -2 mA	3.3V	25 ns
FIXCS CSBASE26 CSPORTZ	A1:15, SA0, AEN	50 pf	+2 mA -2 mA	3.3V	30 ns
RSTIDE	MXCTL0:2 DACKEN IDEON	200 pf	+12 mA -3 mA	5V	40 ns
RESIN RESIN	RSTSW	50 pf	+2 mA -2 mA	3.3V	40 ns
LOWPREQ	FULLPDN	50 pf	+2 mA -2 mA	3.3V	40 ns
WE0 WE1 WE2 WE3	WE	150 pf	+8 mA -2 mA	3.3V	25 ns
MS60	REFRESH	50 pf	+2 mA -2 mA	3.3V	NA
RESET	MXCTL0:2 DACKEN	200 pf	+24 mA -3 mA	5V	40 ns

1. SA1:19 switch simultaneously

2. LA17:19 LA21:23 switch simultaneously. Skew between LA switching and SA bus switching is at least 31.5 ns.

3. Signal group PMCR[1:15] above denotes the output signals of the PMC registers. See section 2.3 for more information about these signals.

7.2 INPUT VALID TIMES AND VOLTAGE  
LEVELS: ADDRESS BUFFER  
FUNCTION

T-52-38

SIGNAL	REFERENCE	I <sub>H</sub> /I <sub>L</sub>	VOLTAGE	TERMINATION	SETUP/HOLD
A1:16	ALE falling	+10 $\mu$ A -10 $\mu$ A	3.3V	None	10/5 ns
A17:23	READY	$\pm$ 10 $\mu$ A	3.3V	None	10/5 ns
TURBO PROCPGD LCL_REQ PMCIN(4) PMCIN(6) PMCIN(7)	MXCTL0	+10 $\mu$ A -10 $\mu$ A	3.3V	Turbo: 50K Pull-up	
PCUW0 PCUW1		+10 $\mu$ A -10 $\mu$ A	3.3V	None	
READY ALE		+10 $\mu$ A -10 $\mu$ A	3.3V	None	
MASTER REFRESH AEN		+10 $\mu$ A -10 $\mu$ A	5.0V		
RSMSW SUSPSW XSUSPREQ XRSMREQ BATPWR BATLO2 MXCTL0:2 P5VPGD SUSPBLK RSMBLK MINISUS		+10 $\mu$ A -10 $\mu$ A	3.3V	50K pull-up 50K pull-up 50K pull-up 50K pull-up None None None None 50K pull-up 50K pull-up None	
RAD0:7	PCUW0 PCUW1	+10 $\mu$ A -10 $\mu$ A	3.3V	None	10/5 ns
WE		+10 $\mu$ A -10 $\mu$ A	3.3V	None	
RSTSW LOWPWR		+10 $\mu$ A -10 $\mu$ A	3.3V	50K pull-up 50K pull-down	
DACKEN		+10 $\mu$ A -10 $\mu$ A	3.3V	None	
SA0		+10 $\mu$ A -10 $\mu$ A	5.0V	None	



7.3 OUTPUT VALID TIMES AND VOLTAGE LEVELS: DATA BUFFER FUNCTION

T-52-38

SIGNAL	REFERENCE	CAPLOAD	I <sub>OL</sub> +I <sub>OH</sub>	VOLTAGE	DELAY (NS)
SD(0:15)	D0:15	200 pf	+24 mA -3 mA	5 V	40 ns
	$\overline{DEN0}$ $\overline{DEN1}$				40 ns
D(0:15)	SD(0:15)	100 pf	+4 mA -2 mA	3.3V	40 ns
HD(0:6) HD(8:15)	D(0:15)	200 pf	+12 mA -3 mA	5 V	40 ns
SD2LV SD3LV	D2,D3	50 pf	+2 mA -2 mA	3.3V	40 ns
DRQIN	MXCTL0:2 DRQ0:7	50 pf	+2 mA -2 mA	3.3V	25 ns
$\overline{SMEMR}$	$\overline{MEMR}$	200 pf	+24 mA -3 mA	5V	30 ns
$\overline{SMEMW}$	$\overline{MEMW}$	200 pf	+24 mA -3 mA	5V	30 ns
$\overline{DACK0:3}$ $\overline{DACK5:7}$	DACKEN	50 pf	+2 mA -2 mA	5V	25 ns
$\overline{IOWLV}$	$\overline{IOW}$	50 pf	+2 mA -2 mA	3.3V	30 ns
$\overline{IORLV}$	$\overline{IOR}$	50 pf	+2 mA -2 ma	3.3V	30 ns
Port A(0:7) Port B(0:7) Port C(0:7) Port Y0	$\overline{IOW}$ Rising Edge	50 pf	+2 mA -2 mA	3.3V	40 ns

1. SD(0:15) switch simultaneously
2.  $\overline{SMEMR}$ ,  $\overline{SMEMW}$ . Only one of these two signals is active at a time and is skewed from the address at least 30 ns

7.4 INPUT VALID VOLTAGE LEVELS AND  
SETUP TIMES: DATA BUFFER  
FUNCTION

T-52-38

SIGNAL	REFERENCE	I <sub>H</sub> /I <sub>L</sub>	TERMINATION	VOLTAGE	SETUP/HOLD
DEN0 DEN1 DTR		10 $\mu$ A	None	3.3V	
SDEN SDTR		10 $\mu$ A	None	3.3V	
DRQ0:3 DRQ5:7		+100 $\mu$ A -100 $\mu$ A	20K pull-down	5 V	
IDEDENL IDEDENH			None	3.3V	
HD(0:6) HD(8:15)			None	5V	
MXCTL(0:2)		+10 $\mu$ A -10 $\mu$ A		3.3V	
TOR TOW			50K pull-up	5V	
MEMR MEMW			50K pull-up	5V	
LOWMEG			None	3.3V	
Port A(0:7) B(0:7) C(0:7)			None	3.3V	
Y0 Z(0:3)			None	3.3V	
CSBASE CSPORTZ	TOR/TOW Rising edge		None	3.3V	10/5 ns
DACKEN			None	3.3V	
SD(0:15)			20K pull-up	5V	
IDEON FULLPDN PROCPDN			None	3.3V	
SA(0:2)	TOR/TOW Rising edge		None	5V	10/5 ns
D0:15	TOW Rising edge		None	3.3V	10/5 ns



## DC ELECTRICAL SPECIFICATIONS

WD7625LP

WESTERN DIGITAL CORP

54E D ■ 9718228 0015767 3T8 ■ WDC

## 7.5 5.0 VOLT CHARACTERISTICS

T-52-38

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
I <sub>IH</sub>	Input leakage high	---	.01	10	μA	V <sub>IN</sub> =V <sub>DD</sub> , V <sub>DD</sub> =5.5V
I <sub>IL</sub>	Input leakage low (no pull-up) 40K pull-up	-10	.01		μA	V <sub>IN</sub> =V <sub>SS</sub> , V <sub>DD</sub> =5.5V
		-325	-160	-40	μA	
I <sub>OZ</sub>	Output leakage (no pull-up)	-10	.01	10	μA	V <sub>IN</sub> =V <sub>DD</sub> or V <sub>SS</sub> , V <sub>DD</sub> =5.5V
V <sub>IL</sub>	Input voltage low	-0.6	---	0.8	V	
V <sub>IH</sub>	Input voltage high	2.0	---	5.5	V	
V <sub>OL</sub>	Output voltage low	---	0.2	0.4	V	V <sub>OL</sub> =as rated, V <sub>DD</sub> =4.5V
V <sub>OH</sub>	Output voltage high	2.4	V <sub>DD</sub> -0.2	---	V	V <sub>OH</sub> =as rated, V <sub>DD</sub> =4.5V





**WD7625LP**

DC ELECTRICAL SPECIFICATIONS

WESTERN DIGITAL CORP

54E D ■ 9718228 0015768 234 ■ WDC

7.6 3.3 VOLT CHARACTERISTICS

T-52-38

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
$I_{IH}$	Input leakage high	---	.01	10	$\mu A$	$V_{IN}=V_{DD}$ , $V_{DD}=3.6V$
$I_{IL}$	Input leakage low (no pull-up) 40K pull-up	-10	.01		$\mu A$	$V_{IN}=V_{SS}$ , $V_{DD}=3.6V$
		-200	-60	-10	$\mu A$	
$I_{OZ}$	Output leakage (no pull-up)	-10	.01	10	$\mu A$	$V_{IN}=V_{DD}$ or $V_{SS}$ , $V_{DD}=3.6V$
$V_{IL}$	Input voltage low	-0.6	---	0.8	V	
$V_{IH}$	Input voltage high	2.0	---	$V_{CC}+0.3$	V	
$V_{OL}$	Output voltage low	---	0.2	0.4	V	$V_{OL}$ =as rated, $V_{DD}=3.0V$
$V_{OH}$	Output voltage high	2.4	$V_{DD}-0.2$	---	V	$V_{OH}$ =as rated, $V_{DD}=3.0V$



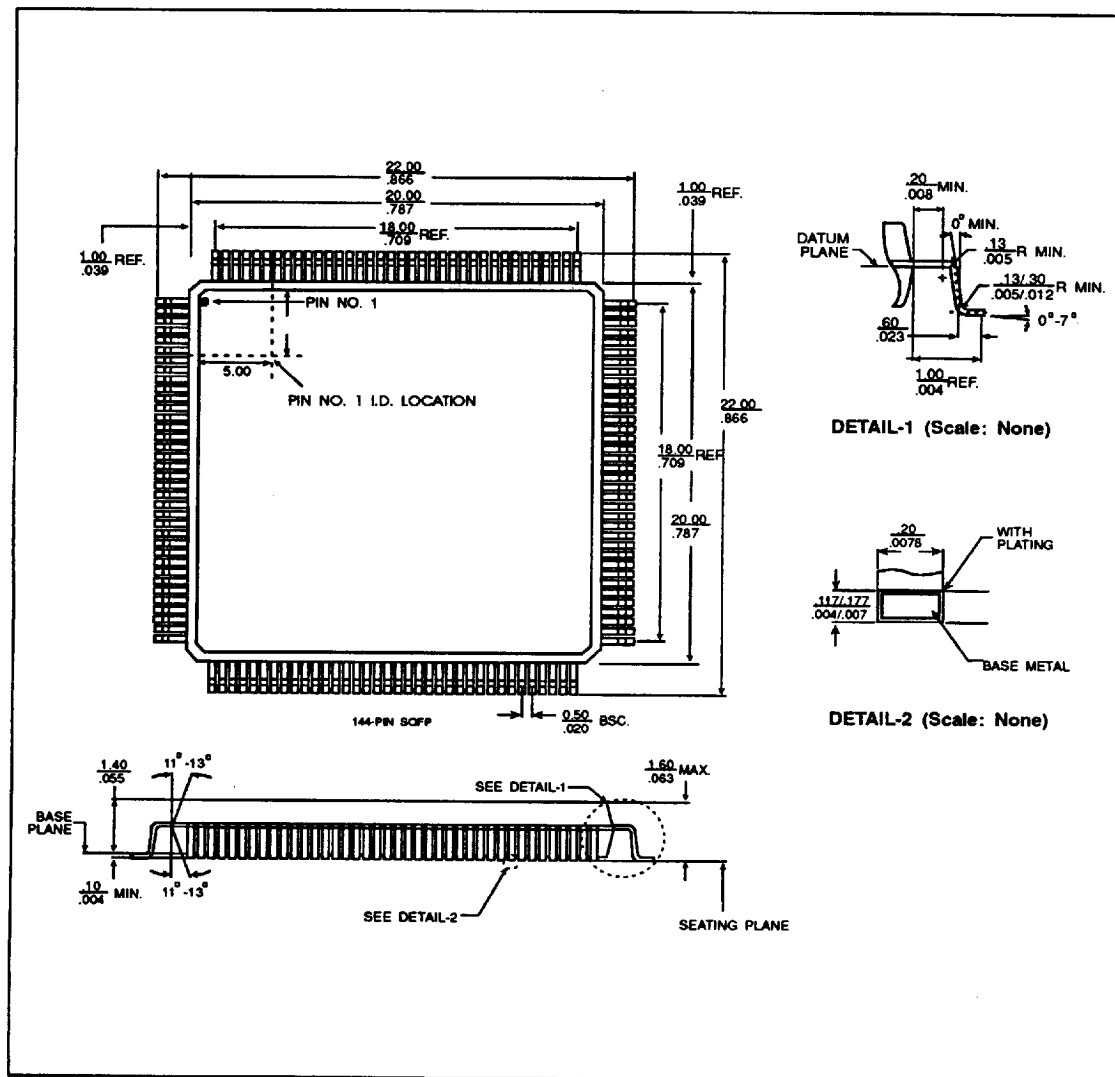


FIGURE 8-1. WD7625LP PACKAGE DIAGRAM

**A.0 TEST METHODS**

The test methods used for the WD7625LP consist of tristating the outputs and I/O mapping.

If all three pins 81-83 are low and the two pins 122, 124 are high and a low to high transition of pin 76 occurs then the WD7625LP is set in the I/O Mapping Mode. In this mode all inputs including bidirectional signals are multiplexed onto output pins. This mode is useful in production test environments to ensure that all pins are properly soldered onto the printed circuit board without short or open circuits.

**A.1 TRISTATING THE OUTPUTS****T-52-38**

If all four pins 81 - 83, and 122 are all low and pin 124 is high and a low to high transition of pin 86 occurs, the WD7625LP is put in a tristate mode where all outputs are tristated for board testing.

In this mode all the pull-ups at the output buffers can be turned off for leakage current testing by bringing pin 128 to low.



## B.0 WD7625 PIN ORDER CROSS-REFERENCE

T-52-38

PIN	MODE		I/O TYPE		VOLTAGE BUS		PU/PD	
	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
1	PMCR8	HD3	O	I/O	VDD3	VHD		
2	PMCR10	HD4	O	I/O	VDD3	VHD		
3	PMCR11	HD5	O	I/O	VDD3	VHD		
4	PMCR14	HD6	O	I/O	VDD3	VHD		
5	ALE	HD8	I	I/O	VDD3	VHD		
6	WE	HD9	I	I/O	VDD3	VHD		
7	VSS	VSS	---	---	---	---		
8	LCDEN	HD10	O	I/O	VDD3	VHD		
9	BLÉN	HD11	O	I/O	VDD3	VHD		
10	LCL_ACK	HD12	O	I/O	VDD3	VHD		
11	VDD3	VHD	---	---	---	---		
12	PMCR9	HD13	O	I/O	VDD3	VHD		
13	IDEON/ PMCR12	HD14	O	I/O	VDD3	VHD		
14	RSTIDE	HD15	OD	I/O	VDD3*	VHD	OD	
15	VDD3	VDD5	---	---	---	---		
16	WE0	DACK0	O	O	VDD3	VDD5		
17	WE1	DACK5	O	O	VDD3	VDD5		
18	WE2	DACK6	O	O	VDD3	VDD5		
19	WE3	DACK7	O	O	VDD3	VDD5		
20	PMCR13	SA0	O	I	VDD3	VDD5		
21	PMCR15	SA1	O	I	VDD3	VDD5		
22	PROCPDN	SA2	O	I	VDD3	VDD5		
23	RESIN	SMEMR	O	O	VDD3	VDD5		50K PU
24	VSS	VSS	---	---	---	---		
25	SA1	SD0	I/O	I/O	VDD5	VDD5		20K PU
26	SA2	SD1	I/O	I/O	VDD5	VDD5		20K PU
27	SA3	SD2	I/O	I/O	VDD5	VDD5		20K PU
28	SA4	SD3	I/O	I/O	VDD5	VDD5		20K PU
29	SA5	SD4	I/O	I/O	VDD5	VDD5		20K PU
30	VSS	VSS	---	---	---	---		
31	SA6	SD5	I/O	I/O	VDD5	VDD5		20K PU
32	VDD5	VDD5	---	---	---	---		
33	SA7	SD6	I/O	I/O	VDD5	VDD5		20K PU
34	SA8	SD7	I/O	I/O	VDD5	VDD5		20K PU

TABLE B-1. WD7625LP PIN ORDER CROSS REFERENCE

\* Pull-up for this pin must be tied to the lowest VDD to prevent latchup.



## WD7625LP

## WD7625 PIN ORDER CROSS-REFERENCE

WESTERN DIGITAL CORP

54E D ■ 9718228 0015772 765 ■ WDC

PIN	MODE		I/O TYPE		VOLTAGE BUS		PU/PD	
	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
35	SA9	SD8	I/O	I/O	VDD5	VDD5		
36	SA10	SD9	I/O	I/O	VDD5	VDD5		
37	SA11	SD10	I/O	I/O	VDD5	VDD5		
38	SA12	SD11	I/O	I/O	VDD5	VDD5		
39	SA13	SD12	I/O	I/O	VDD5	VDD5		
40	SA14	SD13	I/O	I/O	VDD5	VDD5		
41	SA15	SD14	I/O	I/O	VDD5	VDD5		
42	SA16	SD15	I/O	I/O	VDD5	VDD5		
43	VSS	VSS	---	---	---	---		
44	SA17	DACK1	O	O	VDD5	VDD5		
45	SA18	DACK2	O	O	VDD5	VDD5		
46	SA19	DACK3	O	O	VDD5	VDD5		
47	VDD5	VDD5	---	---	---	---		
48	SBHE	DRQ3	I/O	I	VDD5	VDD5		20K PD
49	VSS	VSS	---	---	---	---		
50	RESET	SMEW	O	O	VDD5	VDD5		50K PU
51	LA17	DRQ0	I/O	I	VDD5	VDD5		20K PD
52	LA18	DRQ1	I/O	I	VDD5	VDD5		20K PD
53	LA19	DRQ2	I/O	I	VDD5	VDD5		20K PD
54	LA21	DRQ5	I/O	I	VDD5	VDD5		20K PD
55	LA22	DRQ6	I/O	I	VDD5	VDD5		20K PD
56	LA23	DRQ7	I/O	I	VDD5	VDD5		20K PD
57	VSS	VSS	---	---	---	---		
58	SA0	IOR	I	I	VDD5	VDD5		50K PU
59	MASTER	IOW	I	I	VDD5	VDD5		50K PU
60	AEN	MEMR	I	I	VDD5	VDD5		50K PU
61	REFRESH	MEMW	I	I	VDD5	VDD5		50K PU
62	VSS	VSS	---	---	---	---		
63	SA2LV 25/26 Strap	IORLV 25/26 Strap	I/O	I/O	VDD3	VDD3	50K PU SO	50K PU SO
64	LOWPREC	IOWLV	O	O	VDD3	VDD3		
65	PMCINMX	DRQIN	O	O	VDD3	VDD3		

TABLE B-1. WD7625LP PIN ORDER CROSS REFERENCE (CONTINUED)



WESTERN DIGITAL CORP

54E D ■ 9718228 0015773 6T1 ■ WDC

PIN	MODE		I/O TYPE		VOLTAGE BUS		PU/PD	
	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
66	CSPORTZ 5V Only Strap	CSPORTZ 5V Only Strap	I/O	I	VDD3	VDD3	50K PU SO	50K PU SO
67	CSBASE 3V only Strap	CSBASE 3V only Strap	I/O	I	VDD3	VDD3	50K PU SO	50K PU SO
68	VDD3	VDD3	---	---	---	---		
69	BATPWR	SD2LV	I	O	VDD3	VDD3		
70	BATLO2	SD3LV 5V HD Strap	I	I/O	VDD3	VDD3		50K PU SO
71	FULLPDN	FULLPDN	O	I	VDD3	VDD3		
72	XSUSRQ	LOWMEG	I	I	VDD3	VDD3	50K PU	
73	XRSMRQ1	DEN0	I	I	VDD3	VDD3	50K PU	
74	XRSMRQ2	DEN1	I	I	VDD3	VDD3	50K PU	
75	XRSMRQ3	SDEN	I	I	VDD3	VDD3	50K PU	
76	RSTSW	RESIN	I	I	VDD3	VDD3		
77	READY	SDTR	I	I	VDD3	VDD3		
78	VSS	VSS	---	---	---	---		
79	SUSPSW	IDEENL	I	I	VDD3	VDD3	50K PU	
80	RSMSW	IDEENH	I	I	VDD3	VDD3	50K PU	
81	MXCTL0	MXCTL0	I	I	VDD3	VDD3		
82	MXCTL1	MXCTL1	I	I	VDD3	VDD3		
83	MXCTL2	MXCTL2	I	I	VDD3	VDD3		
84	VDD3	VDD3	---	---	---	---		
85	DACKEN	DACKEN	I	I	VDD3	VDD3		
86	RESIN	DTR	O	I	VDD3	VDD3		
87	VSS	VSS	---	---	---	---		
88	A1	D0	I/O	I/O	VDD3	VDD3		
89	A2	D1	I/O	I/O	VDD3	VDD3		
90	A3	D2	I/O	I/O	VDD3	VDD3		
91	A4	D3	I/O	I/O	VDD3	VDD3		
92	A5	D4	I/O	I/O	VDD3	VDD3		
93	A6	D5	I/O	I/O	VDD3	VDD3		
94	A7	D6	I/O	I/O	VDD3	VDD3		

TABLE B-1. WD7625LP PIN ORDER CROSS REFERENCE (CONTINUED)



WD7625LP

WD7625 PIN ORDER CROSS-REFERENCE

WESTERN DIGITAL CORP

54E D ■ 9718228 0015774 538 ■ WDC

PIN	MODE		I/O TYPE		VOLTAGE BUS		PU/PD	
	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
95	A8	D7	I/O	I/O	VDD3	VDD3		
96	A9	D8	I/O	I/O	VDD3	VDD3		
97	VDD3	VDD3	---	---	---	---		
98	A10	D9	I/O	I/O	VDD3	VDD3		
99	A11	D10	I/O	I/O	VDD3	VDD3		
100	A12	D11	I/O	I/O	VDD3	VDD3		
101	A13	D12	I/O	I/O	VDD3	VDD3		
102	A14	D13	I/O	I/O	VDD3	VDD3		
103	A15	D14	I/O	I/O	VDD3	VDD3		
104	A16	D15	I/O	I/O	VDD3	VDD3		
105	VSS	VSS	---	---	---	---		
106	A17	PA0	I/O	I/O	VDD3	VDD3		
107	A18	PA1	I/O	I/O	VDD3	VDD3		
108	A19	PA2	I/O	I/O	VDD3	VDD3		
109	A21	PA3	I/O	I/O	VDD3	VDD3		
110	A22	PA4	I/O	I/O	VDD3	VDD3		
111	A23	PA5	I/O	I/O	VDD3	VDD3		
112	BHE	PA6	I/O	I/O	VDD3	VDD3		
113	MS120 Sus/Res select	PA7	I/O	I/O	VDD3	VDD3	50K PU SO	
114	SUSPBLK	PZ0	I	I	VDD3	VDD3		
115	RSMBLK	PZ1	I	I	VDD3	VDD3		
116	MINISUS	PZ2	I	I	VDD3	VDD3		
117	P5VPGD	PZ3	I	I	VDD3	VDD3		
118	VDD5	VDD5	---	---	---	---		
119	RAD0	PB0	I	I/O	VDD3	VDD3		
120	VDD3	VDD3	---	---	---	---		
121	RAD1	PB1	I	I/O	VDD3	VDD3		
122	RAD2	PB2	I	I/O	VDD3	VDD3		
123	RAD3	PB3	I	I/O	VDD3	VDD3		
124	RAD4	PB4	I	I/O	VDD3	VDD3		
125	RAD5	PB5	I	I/O	VDD3	VDD3		
126	RAD6	PB6	I	I/O	VDD3	VDD3		
127	RAD7	PB7	I	I/O	VDD3	VDD3		
128	PCUW0	PC0	I	I/O	VDD3	VDD3		

TABLE B-1. WD7625LP PIN ORDER CROSS REFERENCE (CONTINUED)



T-52-38

WD7625LP

WD7625 PIN ORDER CROSS-REFERENCE

WESTERN DIGITAL CORP

54E D ■ 9718228 0015775 474 ■ WDC

PIN	MODE		I/O TYPE		VOLTAGE BUS		PU/PD	
	ADDR	DATA	ADDR	DATA	ADDR	DATA	ADDR	DATA
129	PCUW1	PC1	I	I/O	VDD3	VDD3		
130	TURBO	PC2	I	I/O	VDD3	VDD3	50K PU	
131	VSS	VSS	---	---	---	---		
132	PROCPGD	PC3	I	I/O	VDD3	VDD3		
133	LCL REQ	PC4	I	I/O	VDD3	VDD3		
134	PMCIN4	PC5	I	I/O	VDD3	VDD3		
135	PMCIN6	PC6	I	I/O	VDD3	VDD3		
136	PMCIN7	PC7	I	I/O	VDD3	VDD3		
137	LOWPWR	PY0	I	I/O	VDD3	VDD3	50K PD	
138	RESUME	IDEON	O	I	VDD3	VDD3		
139	FIXCS	PROCPDN	O	I	VDD3	VDD3		
140	VSS	VSS	---	---	---	---		
141	FSAD	HD0	I	I/O	VDD3	VHD		
142	VDD3	VHD	---	---	---	---		
143	PMCR4	HD1	O	I/O	VDD3	VHD		
144	PMCR6	HD2	O	I/O	VDD3	VHD		

TABLE B-1. WD7625LP PIN ORDER CROSS REFERENCE (CONTINUED)





WD7625LP  
 WESTERN DIGITAL CORP 54E D ■ 9718228 0015776 300 ■ WDC  
**C.0 INPUT THRESHOLD ADJUSTMENT**

The table below illustrates some possible strapping options and the corresponding input threshold adjustments required.

Driving the 3 volt only and 5 volt only straps both low is an illegal combination. The WD7625LP as-

sumes a mixed voltage mode when both of these straps are allowed to float high.

The WD7625LP also does not accommodate a 3 volt only mode when it is attached to a 5 volt hard disk drive's power supply.

STRAPPING OPTION COMBINATIONS			ADDRESS MODE INPUT THRESHOLD ADJUSTMENT		DATA BUFFER MODE INPUT THRESHOLD ADJUSTMENT		
3V ONLY ACTIVE LOW	5V ONLY ACTIVE LOW	HD5/3 1=5V	3V BUS	5V BUS	3V BUS	5V BUS	HD BUS
0	1	0	3V	3V	3V	3V	3V
1	0	0	5V	5V	5V	5V	3V
1	0	1	5V	5V	5V	5V	5V
1	1	0	3V	5V	3V	5V	3V
1	1	1	3V	5V	3V	5V	5V

TABLE C-1. INPUT THRESHOLD ADJUSTMENT



WESTERN DIGITAL CORP

54E D ■ 9718228 0015777 247 ■ WDC

**D.0 I/O REQUIREMENTS****D.1 ADDRESS BUFFER MODE**

The table below indicates the voltages applied to or expected from the WD7625LP pins in a typical mixed voltage (3.3V/5V) laptop design.

The voltages listed for output pins are the requested levels that those pins should drive out,

not levels that might be applied to those pins from other sources.

Voltages listed for bidirectional pins (i.e., the system data bus) may indicate input or output levels.

See the notes at the end of the table.

DESCRIPTION	SIGNAL NAME	I/O	OPERATING MODE	
			NORMAL	SUSPEND
ADDRESS BUS INTERFACE <sup>1</sup>	A(1:19, 21:23)	I/O	0-3.3V	0V/Z <sup>2,3</sup>
	SA(1:2)	I/O	0-V <sub>CCAT</sub>	0V or Z/Z <sup>4</sup>
	SA(3:16)	I/O	0-V <sub>CCAT</sub>	0V or Z/Z <sup>4</sup>
	SA(17:19)	O	0-V <sub>CCAT</sub>	Z <sup>5</sup>
	SA2LV	O	0-3.3V	0-3.3V
	LA(17:19, 21:23)	I/O	0-V <sub>CCAT</sub>	0V or Z/Z <sup>4</sup>
	BHE	I/O	0-3.3V	0V/Z <sup>2,3</sup>
	SBHE	I/O	0-V <sub>CCAT</sub>	0V or Z/Z <sup>4</sup>
	ALE	I	0-3.3V	Z
	READY	I	0-3.3V	0V <sup>2,3</sup>
	MASTER	I	0-V <sub>CCAT</sub>	0V or V <sub>CCAT</sub> <sup>5</sup>
SUSPEND/RESUME	SUSPSW, RSMSW	I	0-3.3V	0-3.3V
	XSUSPRQ, SUSPBLK, XRSMRQ1, XRSMRQ2, XRSMRQ3, RSMBLK, MINISUS	I	0-3.3V	0-3.3V
	BATPWR, BATLO <sup>2</sup> , LOWPWR	I	0-3.3V	0-3.3V
	LOPWREQ	O	0-3.3V	0-3.3V

**TABLE D-1. I/O REQUIREMENTS ADDRESS BUFFER MODE**

<sup>1</sup> Power distribution to the AT bus is system dependent. Power to the AT bus connectors may be 5V or 3.3V and it can be switched off or left on during suspend. The AT bus interface power pin (V<sub>CCAT</sub>) is connected to 5V or 3.3V respectively. During suspend, if V<sub>CCAT</sub> is normally 5V, it can remain at 5V or drop to ~3.0V. If V<sub>CCAT</sub> is normally 3.3V, it remains at that voltage during suspend. V<sub>CCAT</sub> will never switch off to 0V under any circumstances.

<sup>2</sup> This signal is connected to a device that is powered down during suspend. The output buffer (if O or I/O) for this signal should be tristated. The input buffer (if I or I/O) should be disabled and internally forced to an inactive state.

<sup>3</sup> This signal is connected to the processor and/or coprocessor which are powered down during processor powerdown. The output buffer (if O or I/O) for this signal should be tristated and the input buffer (if I or I/O) should be disabled and internally forced to an inactive state during processor powerdown.

<sup>4</sup> This signal is connected to a device that is powered down or tristated during suspend. The output buffer (if O or I/O) for this signal should be tristated. The input buffer (if I or I/O) should be disabled and internally forced to an inactive state.

WD7625LP  
WESTERN DIGITAL CORP

54E D ■ 9718228 0015778 183 ■ WDC

DESCRIPTION	SIGNAL NAME	I/O	OPERATING MODE	
			NORMAL	SUSPEND
POWER MANAGEMENT	RAD(0:7)	I	0-3.3V	0-3.3V
	PCUW0, PCUW1	I	0-3.3V	0-3.3V
	P5VPGD	I	0-3.3V	0-3.3V
	LCDEN, BLEN, LCL_ACK, IDEON, PROCPDN, FULLPDN	O	0-3.3V	0-3.3V
	PMCR (0, 4, 6, 8, 9, 10, 11, 12, 13, 14, 15)	O	0-3.3V	0-3.3V
	TURBO, PROCPGD, LCL_REQ	I	0-3.3V	0-3.3V
	PMCIN (4, 6, 7)	I	0-3.3V	0-3.3V
	PMCINMX	O	0-3.3V	0-3.3V
	MXCTL0-MXCTL2	I	0-3.3V	0-3.3V

TABLE D-1. I/O REQUIREMENTS ADDRESS BUFFER MODE (CONTINUED)



## I/O REQUIREMENTS

WESTERN DIGITAL CORP

54E D

9718228 0015779 01T WDC

DESCRIPTION	SIGNAL NAME	I/O	OPERATING MODE	
			NORMAL	SUSPEND
I/O ADDRESS DECODE	AEN	I	0-V <sub>CCAT</sub>	0V or Z <sup>5</sup>
	SA0	I	0-V <sub>CCAT</sub>	0V or Z <sup>4</sup>
	CSBASE, CSPORTZ	O	0-3.3V	0-3.3V
	FIXCS	O	0-3.3V	Z <sup>5</sup>
MISCELLANEOUS	REFRESH, MS120/SRMODESEL	I I/O	0-V <sub>CCAT</sub> 0-3.3V	0-V <sub>CCAT</sub> <sup>6</sup> 0-3.3V
	RSTSW	I	0-3.3V	0-3.3V
	RESET	O	0-V <sub>CCAT</sub>	0-V <sub>CCAT</sub> <sup>6</sup>
	RESIN, RESIN	O	0-3.3V	0-3.3V
	RSTIDE	OD	0-3.3V or 5V <sup>7</sup>	Z <sup>2,8</sup>
	WE	I	0-3.3V	0-3.3V
	WE0, WE1, WE2, WE3	O	0-3.3V	0-3.3V
	FSAD	I	0-3.3V	0-3.3V
POWER	VDD3	NA	3.3V	3.3V
	VDD5	NA	5V	0V <sup>9</sup>
	V <sub>CCAT</sub>	NA	3.3V/5V <sup>1</sup>	3.0V/3.3V/5V <sup>10</sup>

TABLE D-1. I/O REQUIREMENTS ADDRESS MODE (CONTINUED)

5 This signal is connected to a device that can be powered down during suspend. The output buffer (if O or I/O) for this signal should be tristated. The input buffer (if I or I/O) should be disabled and internally forced to an inactive state.

6 The AT bus interface power pin (V<sub>CCAT</sub>) can drop from 5V to ~3.0V during suspend. See note 1.

7 This signal has an open drain output and can be connected to a 3.3V or 5V drive. It is pulled up externally to 3.3V or 5V.

8 This signal is connected to a device that can be powered down at times other than suspend (the IDE drive can be powered off during normal system operation).

9 If necessary, the system can be designed so that the 5V power net drops to ~3.0V during suspend instead of 0V. See note 1.

10 If necessary for systems where this pin is connected to 5V, the system can be designed so that the 5V power net drops to ~3.0V during suspend instead of to 0V. See note 1.

WD7625LP  
WESTERN DIGITAL CORP

54E D ■ 9718228 0015780 831 ■ WDC

## D.2 DATA BUFFER MODE

The table below indicates the voltages applied to or expected from the WD7625LP pins in a typical mixed voltage (3.3V/5V) laptop design.

The voltages listed for output pins are the requested levels that those pins should drive out,

not levels that might be applied to those pins from other sources.

Voltages listed for bidirectional pins (i.e., the system data bus) may indicate input or output levels.

See the notes at the end of the table.

DESCRIPTION	SIGNAL NAME	I/O	OPERATING MODE	
			NORMAL	SUSPEND
AT BUS INTERFACE <sup>1</sup>	SD(0:15)	I/O	0-V <sub>CCAT</sub>	0V or Z <sup>2</sup>
	DRQ(0:3, 5:7)	I	0-V <sub>CCAT</sub>	0-V <sub>CCAT</sub> <sup>3</sup>
	DACK(0:3, 5:7)	O	0-V <sub>CCAT</sub>	Z <sup>3</sup>
	SA(0:2)	I	0-V <sub>CCAT</sub>	0V or Z <sup>2</sup>
	IOR, IOW	I	0-V <sub>CCAT</sub>	0V or Z <sup>2</sup>
	MEMR, MEMW	I	0-V <sub>CCAT</sub>	0V or Z <sup>2</sup>
	SMEMR, SMEMW	O	0-V <sub>CCAT</sub>	Z <sup>3</sup>
	RESIN	I	0-V <sub>CCAT</sub>	0-V <sub>CCAT</sub> <sup>4</sup>
	IORLV, IOWLV	O	0-3.3V	Z <sup>3</sup>
DATA BUS INTERFACE	D(0:15)	I/O	0-3.3V	0V/Z <sup>5,6</sup>
	SDLV(2:3)	O	0-3.3V	Z <sup>3</sup>
	DEN0, DEN1, DTR, SDEN, SDTR	I	0-3.3V	Z
IDE INTERFACE	HD(0:6, 8:15)	I/O	0-V <sub>CCIDE</sub> <sup>7</sup>	0V/Z <sup>5</sup>
	IDEDENL	I	0-3.3V	Z
	IDEDENH	I	0-3.3V	Z

TABLE D-2. I/O REQUIREMENTS DATA BUFFER MODE

1 Power distribution to the AT bus is system dependent. Power to the AT bus connectors may be 5V or 3.3V and it can be switched off or left on during suspend. The AT bus interface power pin (V<sub>CCAT</sub>) is connected to 5V or 3.3V respectively. During suspend, if V<sub>CCAT</sub> is normally 5V, it can remain at 5V or drop to ~3.0V. If V<sub>CCAT</sub> is normally 3.3V, it remains at that voltage during suspend. V<sub>CCAT</sub> will never switch off to 0V under any circumstances.

2 This signal is connected to a device that is powered down or tristated during suspend. The output buffer (if O or I/O) for this signal should be tristated. The input buffer (if I or I/O) should be disabled and internally forced to an inactive state.

3 This signal is connected to a device that can be powered down during suspend. The output buffer (if O or I/O) for this signal should be tristated. The input buffer (if I or I/O) should be disabled and internally forced to an inactive state.

4 The AT bus interface power pin (V<sub>CCAT</sub>) can drop from 5V to ~3.0V during suspend. See note 1.

5 This signal is connected to a device that can be powered down during suspend. The output buffer (if O or I/O) for this signal should be tristated. The input buffer (if I or I/O) should be disabled and internally forced to an inactive state.

6 This signal is connected to the processor and/or coprocessor which are powered down during processor powerdown. The output buffer (if O or I/O) for this signal should be tristated and the input buffer (if I or I/O) should be disabled and internally forced to an inactive state during processor powerdown.

7 This signal can be connected to a 3.3V or 5V drive. It is capable of driving and receiving 3.3V or 5V levels accordingly while maintaining TTL compatibility.



## I/O REQUIREMENTS

T-52-38

WD7625LP

WESTERN DIGITAL CORP 54E D ■ 9718228 0015781 778 ■ WDC

DESCRIPTION	SIGNAL NAME	I/O	OPERATING MODE	
			NORMAL	SUSPEND
I/O REGISTERS	PA(0:7)	I/O	0-3.3V	0-3.3V
	PB(0:7)	I/O	0-3.3V	0-3.3V
	PC(0:7)	I/O	0-3.3V	0-3.3V
	PZ(0:3)	I	0-3.3V	0-3.3V
	CSBASE, CSPORTZ	I	0-3.3V	0-3.3V
DMA INTERFACE	DACKEN	I	0-3.3V	0-3.3V
	MXCTL(0:2)	I	0-3.3V	0-3.3V
	DRQIN	O	0-3.3V	0-3.3V
MISCELLANEOUS	LOWMEG	I	0-3.3V	0-3.3V
	FULLPDN	I	0-3.3V	0-3.3V
POWER	VDD3	NA	3.3V	---
	VDD5	NA	5V	0V <sup>8</sup>
	VccAT	NA	3.3V/5V <sup>1</sup>	3.0V/3.3V/5V <sup>9</sup>

TABLE D-2. I/O REQUIREMENTS DATA BUFFER MODE (CONTINUED)

<sup>8</sup> If necessary, the system can be designed so that the 5V power net drops to ~3.0V during suspend instead of 0V. See note 1.

<sup>9</sup> If necessary for systems where this pin is connected to 5V, the system can be designed so that the 5V power net drops to ~3.0V during suspend instead of to 0V. See note 1.



WD7625LP

SUSPEND/RESUME LOGIC SCHEMATICS

WESTERN DIGITAL CORP

54E D

9718228

0015782

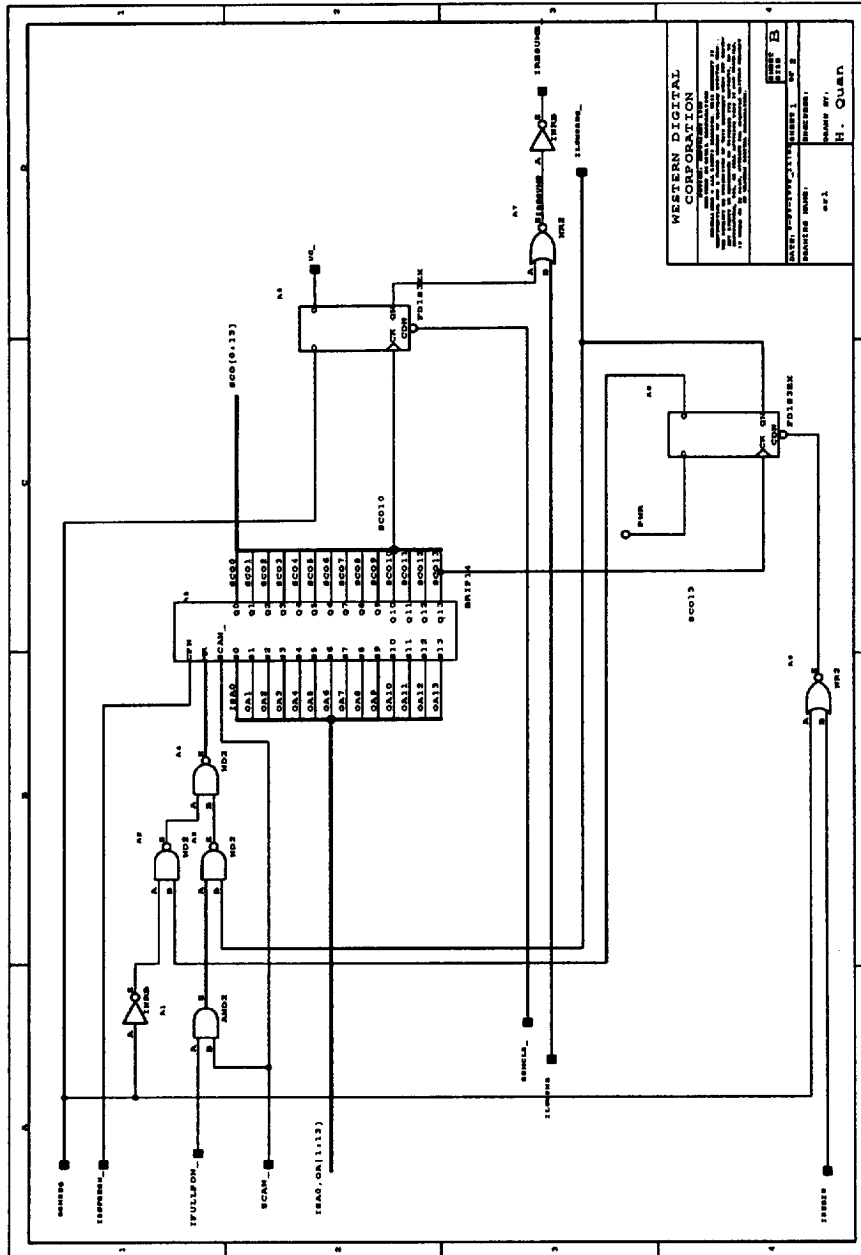
604

WDC

E.0 SUSPEND/RESUME LOGIC SCHEMATICS

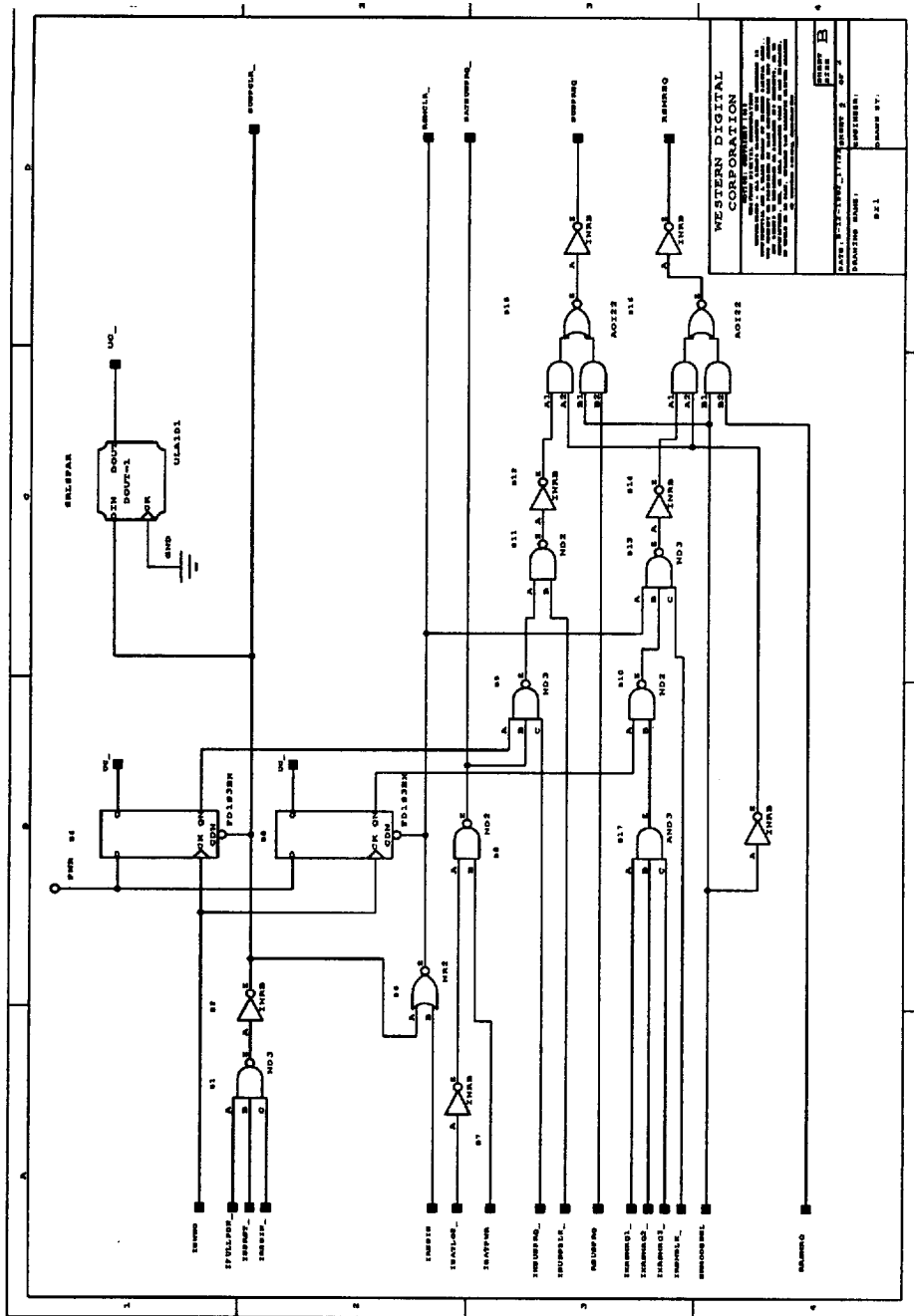
T-52-38

The following three diagrams illustrate the suspend/resume logic.



WESTERN DIGITAL CORPORATION  
DATE: 10/15/75  
DRAWN BY: H. GUAN  
CHECKED BY: H. GUAN  
REVISIONS:  
REV. 1: 10/15/75  
REV. 2: 10/15/75  
REV. 3: 10/15/75  
REV. 4: 10/15/75  
REV. 5: 10/15/75  
REV. 6: 10/15/75  
REV. 7: 10/15/75  
REV. 8: 10/15/75  
REV. 9: 10/15/75  
REV. 10: 10/15/75  
REV. 11: 10/15/75  
REV. 12: 10/15/75  
REV. 13: 10/15/75  
REV. 14: 10/15/75  
REV. 15: 10/15/75  
REV. 16: 10/15/75  
REV. 17: 10/15/75  
REV. 18: 10/15/75  
REV. 19: 10/15/75  
REV. 20: 10/15/75  
REV. 21: 10/15/75  
REV. 22: 10/15/75  
REV. 23: 10/15/75  
REV. 24: 10/15/75  
REV. 25: 10/15/75  
REV. 26: 10/15/75  
REV. 27: 10/15/75  
REV. 28: 10/15/75  
REV. 29: 10/15/75  
REV. 30: 10/15/75  
REV. 31: 10/15/75  
REV. 32: 10/15/75  
REV. 33: 10/15/75  
REV. 34: 10/15/75  
REV. 35: 10/15/75  
REV. 36: 10/15/75  
REV. 37: 10/15/75  
REV. 38: 10/15/75  
REV. 39: 10/15/75  
REV. 40: 10/15/75  
REV. 41: 10/15/75  
REV. 42: 10/15/75  
REV. 43: 10/15/75  
REV. 44: 10/15/75  
REV. 45: 10/15/75  
REV. 46: 10/15/75  
REV. 47: 10/15/75  
REV. 48: 10/15/75  
REV. 49: 10/15/75  
REV. 50: 10/15/75  
REV. 51: 10/15/75  
REV. 52: 10/15/75  
REV. 53: 10/15/75  
REV. 54: 10/15/75  
REV. 55: 10/15/75  
REV. 56: 10/15/75  
REV. 57: 10/15/75  
REV. 58: 10/15/75  
REV. 59: 10/15/75  
REV. 60: 10/15/75  
REV. 61: 10/15/75  
REV. 62: 10/15/75  
REV. 63: 10/15/75  
REV. 64: 10/15/75  
REV. 65: 10/15/75  
REV. 66: 10/15/75  
REV. 67: 10/15/75  
REV. 68: 10/15/75  
REV. 69: 10/15/75  
REV. 70: 10/15/75  
REV. 71: 10/15/75  
REV. 72: 10/15/75  
REV. 73: 10/15/75  
REV. 74: 10/15/75  
REV. 75: 10/15/75  
REV. 76: 10/15/75  
REV. 77: 10/15/75  
REV. 78: 10/15/75  
REV. 79: 10/15/75  
REV. 80: 10/15/75  
REV. 81: 10/15/75  
REV. 82: 10/15/75  
REV. 83: 10/15/75  
REV. 84: 10/15/75  
REV. 85: 10/15/75  
REV. 86: 10/15/75  
REV. 87: 10/15/75  
REV. 88: 10/15/75  
REV. 89: 10/15/75  
REV. 90: 10/15/75  
REV. 91: 10/15/75  
REV. 92: 10/15/75  
REV. 93: 10/15/75  
REV. 94: 10/15/75  
REV. 95: 10/15/75  
REV. 96: 10/15/75  
REV. 97: 10/15/75  
REV. 98: 10/15/75  
REV. 99: 10/15/75  
REV. 100: 10/15/75







WD7625LP

SUSPEND/RESUME LOGIC SCHEMATICS

WESTERN DIGITAL CORP

54E D ■ 9718228 0015784 487 ■ WDC

T-52-38

