W89C10

Winbond

DATA COMPRESSION COPROCESSOR

Advanced Information

GENERAL DESCRIPTION

The Winbond W89C10 is a single-chip data-compression processor that offers high compression, high performance, reliability and ease-of-design. It minimizes data-storage requirements and network bandwidth bottlenecks, by compressing a file or data stream to typically one-half or less of its original size. The Winbond W89C10 allows designers to offer faster, more manageable data-file manipulation and storage capabilities to desktop products.

The processor implements the PKzip-Implode/Explode data compression/decompression algorithm. It provides high compression ratio, ratio between original and compressed data. The compression ratio can vary from one to more than ten times, depending on the file type and file content. For examples, the average ratio is 1.2 - 2.1 for binary file and 2.8 - 4.8 for ASCII file. It also features user-controllable compression ratio and speed.

The W89C10 supports either a PC/AT bus or generic bus interface for 16-bit data transfers. It also supports either low cost single chip 64Kx16 DRAM or high speed SRAMs. A special power-down mode may be enabled for power sensitive applications.

FEATURES

- **Process** Winbond advanced 1.2um SPDM CMOS
- **Package** 100 pins PQFP
- **Source code** 8-bits data, accessed as 16-bits
- **Zip code** Encoded data, accessed as 16-bits
- **Decompression speed** Up to 2MB/sec (Uncompressed data size)
- **Compression speed** Up to 0.2MB/sec
- **Local memory size** 64K x 16bits for up to 32KB sliding dictionary
- **Operating frequency** 25MHz

APPLICATIONS

- DOS transparent hard disk compression
- Hardware accelerator for PKzip included application softwares
- SCSI host bus adapters
- Motherboards of desk top and notebook PCs
- High speed data communication systems
- Mass storage devices
- Embedded controllers

PIN DESCRIPTIONS

[1] Host Bus control

SYMBOL	TYPE	PIN NO	NAME AND FUNCTION
SD(15:0)	I/O	32-39 92-95 86-89	System Data Bus
LA(23:17)	I	1-3 97-100	ISA Additional Address Lines
SA(16:0)	I	11-15 18-29	System Address Bus
-SBHE(-CS)	I	8	-SBHE for ISA; -CS for Generic Bus
-SMEMW	I	10	System Write
-SMEMR	I	9	System Read
BALE	I	7	ISA Bus Address Latch Enable
IOCHRDY	O	31	Ready Signal for Host Access
-MEMCS16	O	5	ISA 16 Bits Memory Access Indicator
IRQ	O	96	Interrupt Request to Host
RESET	I	42	System Reset
-CSOUT	O	6	Chip Select Output to Enable External Bus Drivers

[2] Local memory control

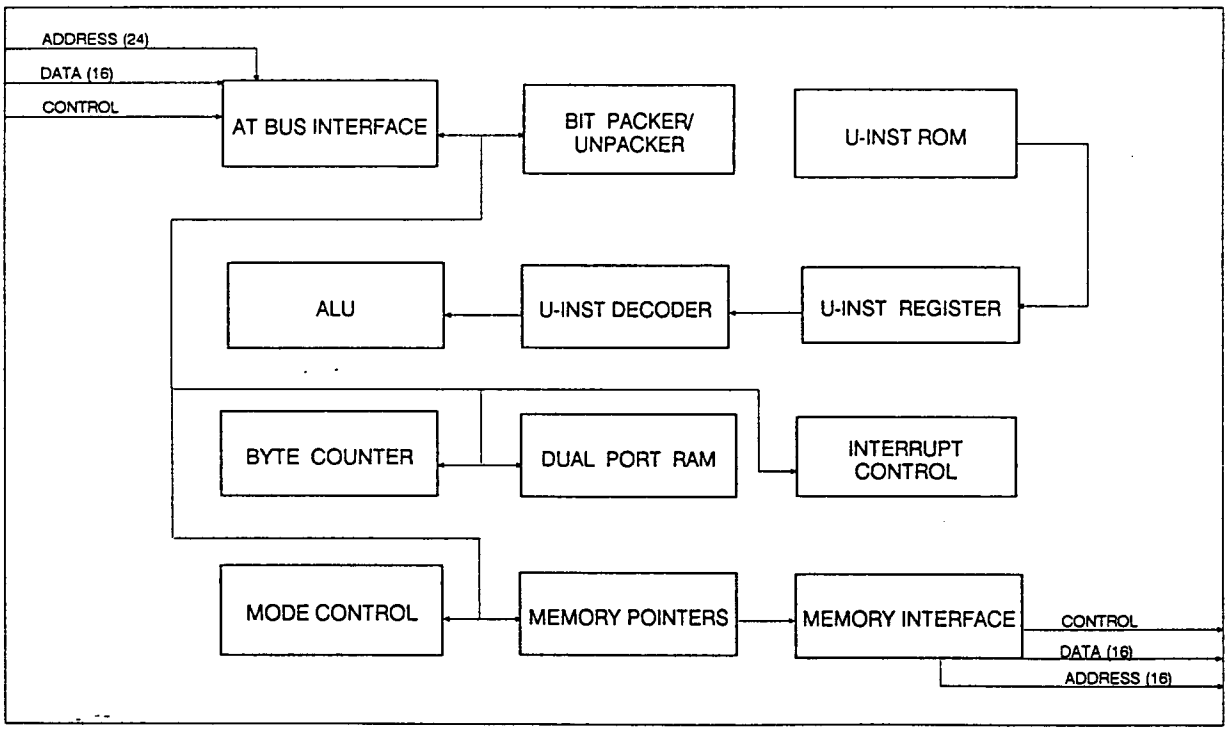
SYMBOL	TYPE	PIN NO	NAME AND FUNCTION
MD(15:0)	I/O	43-50 75-82	Local Memory Data Bus
MA(15:0)	O	53-68	Local Memory Word-Address Bus
-LMCSL	O	70	Local Memory Low Byte Chip Select
-LMCSH	O	69	Local Memory High Byte Chip Select
-LMWR	O	71	Write Control of Local Memory Access

-LMRD	O	72	Read Control of Local Memory Access
-LMAS	O	74	Address strobe of Local Memory Access

[3] Others

SYMBOL	TYPE	PIN NO	NAME AND FUNCTION
CLK	I	83	25MHz Clock Input
TEST	I	84	Test Mode; NC for Normal Operation
ISA	I	85	High for ISA; Low for Generic Bus
V_{SS}		4,16,30 40,51, 73,90	System Ground: 0 Volts
V_{DD}		17,41, 52,91	System Power: 5 Volts

BLOCK DIAGRAM



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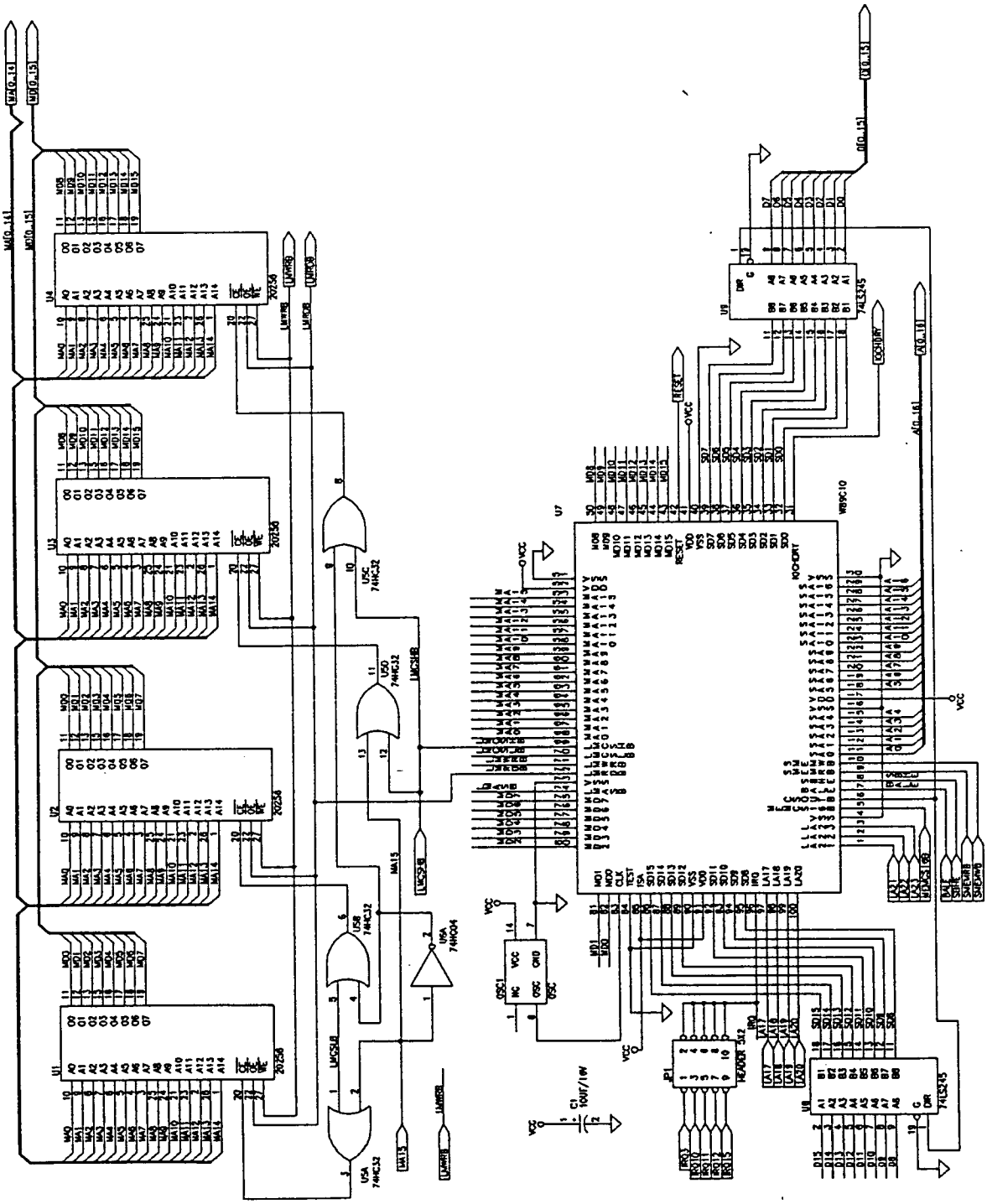
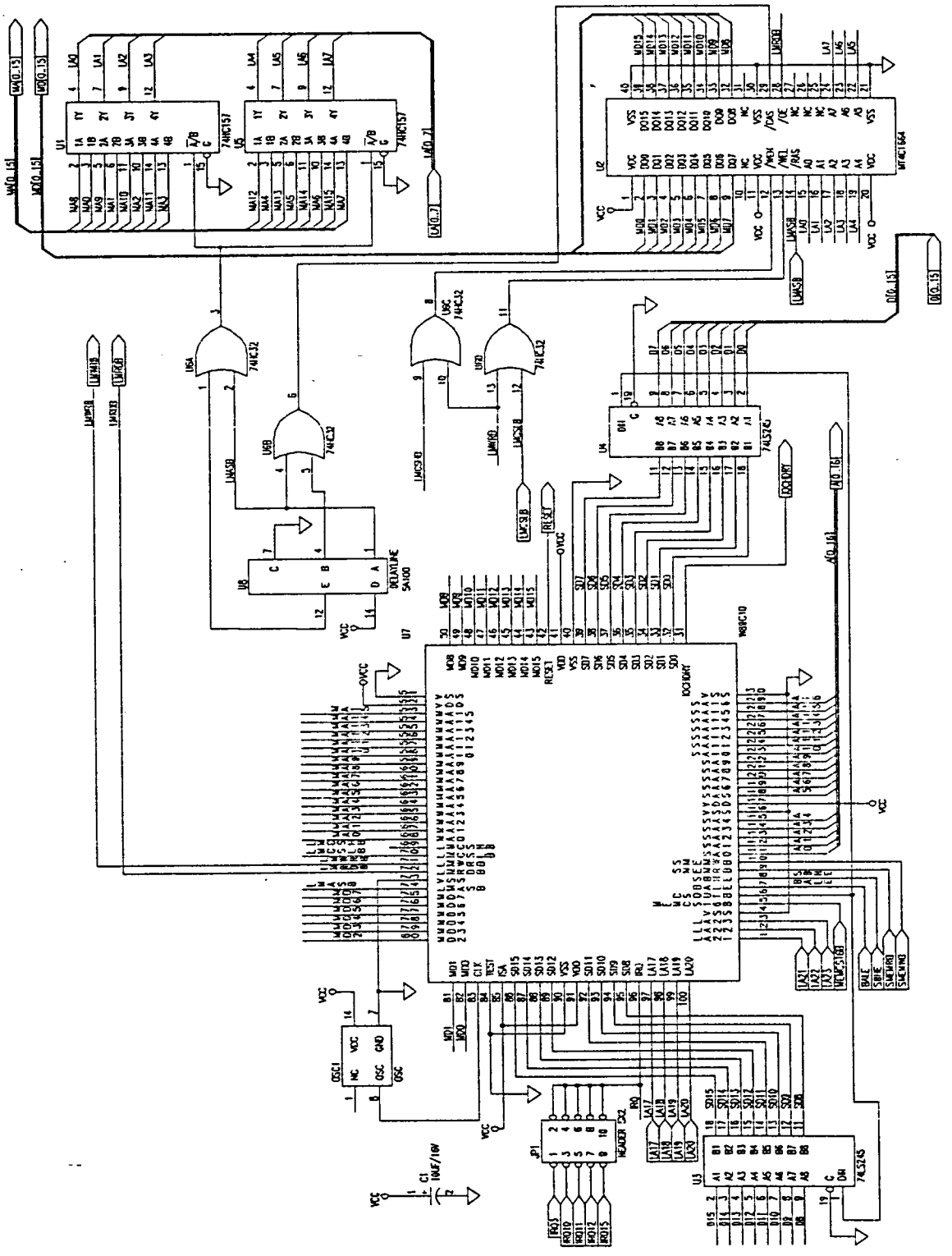
Revision A

APPLICATION CIRCUITS





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