

W83176R-716



DDR BUFFER FOR SIS CHIPSET

W83176R-716

Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
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5					
6					
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LIFE SUPPORT APPLICATIONS

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1.0 GENERAL DESCRIPTION

The W83176R-716 is a 2.5V D.D.R. Clock buffer designed for SiS chipset. W83176R-716 can support 2 D.D.R. DRAM DIMMs. W83176R-716 can be incorporated with W83194BR-640/740 which is the step-less clock with free programmable CPU/AGP/PCI freq. outputs.

The W83176R-716 provides I²C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-716 accepts a pair reference clock as its input and runs on 2.5V supply.

2.0 PRODUCT FEATURES

- Zero-delay clock outputs
- Feedback pins for synchronous
- Supports 2 D.D.R. DIMMs
- One pairs of additional outputs for feedback
- Low Skew outputs (< 100ps)
- Supports 266MHz D.D.R. SDRAM
- I²C 2-Wire serial interface and I²C read back
- 28-pin SSOP package



3.0 PIN CONFIGURATION

CLKC0	1 ●	28	GND
CLKT0	2	27	CLKC5
VDD	3	26	CLKT5
CLKT1	4	25	CLKC4
CLKC1	5	24	CLKT4
GND	6	23	VDD
SDCLK	7	22	SDATA
Buffer_INT	8	21	NC
NC	9	20	FB_INT
VDDA	10	19	FB_OUTT
GND	11	18	NC
VDD	12	17	CLKT3
CLKT2	13	16	CLKC3
CLKC2	14	15	GND

4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Internal 120kΩ pull-up



4.1 Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CLKC[5:0]	1,5,14,16,25,27	OUT	Complementary Clocks of differential pair outputs
CLKT[5:0]	2,4,13,17,24,26	OUT	True Clocks of differential pair outputs
SDATA	22	I/O	Serial data of I ² C 2-wire control interface
SDCLK	7	IN	Serial clock of I ² C 2-wire control interface
Buffer_INT	8	IN	True reference clock input
NC	9, 18, 20	IN	Not connected
FB_OUTT	19	OUT	True Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
FB_INC	21	IN	Complementary Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INC to eliminate phase error.

4.2 Power Pins

SYMBOL	PIN	FUNCTION
GND	6,11,15,28	Ground
VDD	3,12,23	Power Supply 2.5V
AVDD	10	Analog power supply, 2.5V



5.1 Register 0 : Control Register (1 = active, 0 = inactive)

Bit	@PowerUp	Pin	Description
7	1	1,2	CLKC0,CLKT0(Active / Inactive)
6	1	4,5	CLKC1,CLKT1(Active / Inactive)
5	1	13,14	CLKC2,CLKT2(Active / Inactive)
4	1	16,17	CLKC3,CLKT3(Active / Inactive)
3	1	24,25	CLKC4,CLKT4(Active / Inactive)
2	1	26,27	CLKC5,CLKT5(Active / Inactive)
1	1	-	Reserved
0	1	-	Reserved

5.2 Register 1: Reserved Register (default = 1)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved (Skew Control ??)
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	-	Reserved
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

5.3 Register 2: Reserved Register (default = 1)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	-	Reserved
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved



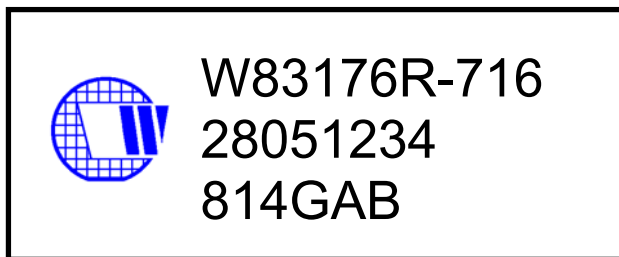
5.4 Register 3: Reserved Register (default = 1)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	-	Reserved
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

6.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83176R-716	28 PIN SSOP	Commercial, 0°C to +70°C

7.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83176R-716

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code

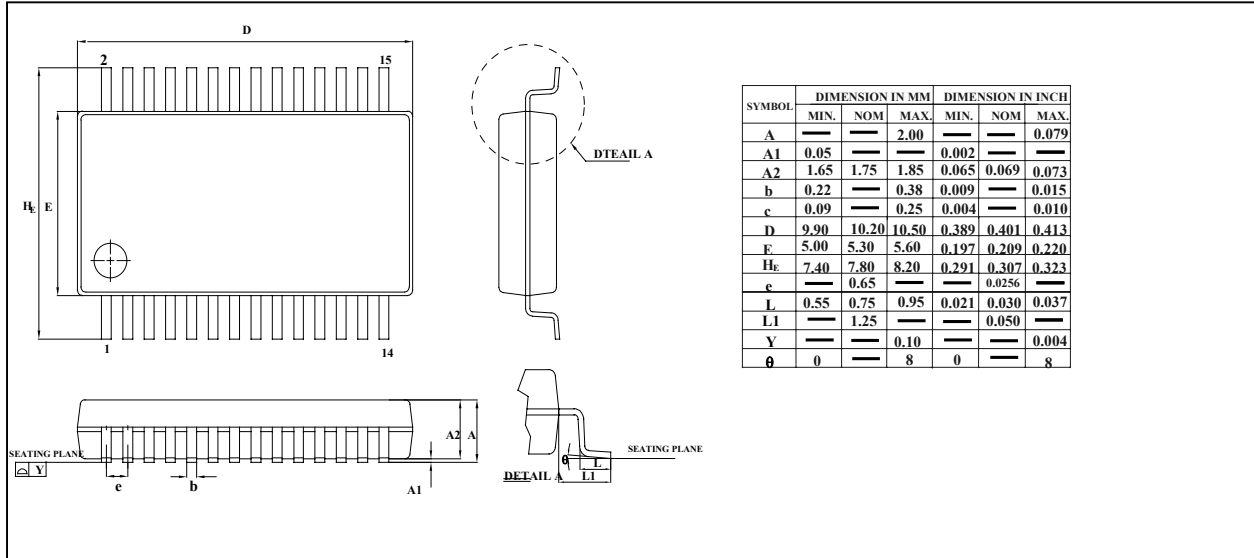
B: IC revision

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8.0 PACKAGE DRAWING AND DIMENSIONS

28pin 209mil



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