Winbond Electronics Corp.

DDR BUFFER FOR SIS CHIPSET

W83176R-705

Data Sheet Revision History

	Pages	Dates	Version	Version On Web	Main Contents
1	n.a.			n.a.	All of the versions before 0.50 are for internal use.
2	n.a.	02/Apr	1.0	1.0	Change version and version on web site to 1.0
3					
4					
5					
6					
7					
8					
9					
10					

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.

Publication Release Date: April. 2002
Revision 1.0

1.0 GENERAL DESCRIPTION

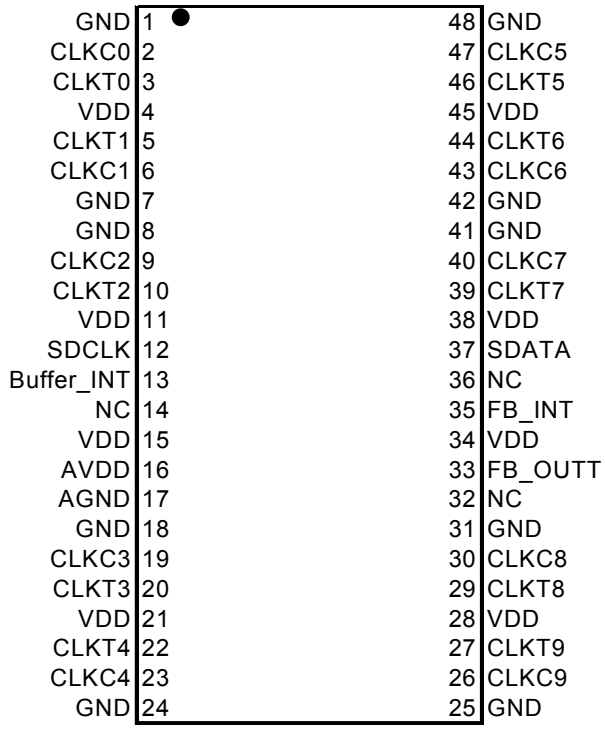
The W83176R-705 is a 2.5V Zero-delay D.D.R. Clock buffer designed for SiS chipset. W83176R-705 can support 3 D.D.R. DRAM DIMMs. W83176R-705 can be incorporated with W83194BR-640/740 which is the step-less clock with free programmable CPU/AGP/PCI freq. outputs.

The W83176R-705 provides I^2C serial bus interface to program the registers to enable or disable each clock outputs. The W83176R-705 accepts a pair reference clock as its input and runs on 2.5V supply.

2.0 PRODUCT FEATURES

- Zero-delay clock outputs
- Feedback pins for synchronous
- Supports up to 3 D.D.R. DIMMs
- One pairs of additional outputs for feedback
- Low Skew outputs (< 100ps)
- Supports 266MHz D.D.R. SDRAM
- I^2C 2-Wire serial interface and I^2C read back
- 48-pin SSOP package

3.0 PIN CONFIGURATION



4.0 PIN DESCRIPTION

IN - Input

OUT - Output

I/O - Bi-directional Pin

- Internal 120kΩ pull-up

4.1 Clock Outputs

SYMBOL	PIN	I/O	FUNCTION
CLKC[9:0]	26,30,40,43,47 ,23,19,9,6,2	OUT	Complementory Clocks of differential pair outputs
CLKT[9:0]	27,29,39,44,46 ,22,20,10,5,3	OUT	True Clocks of differential pair outputs
SDATA	37	I/O	Serial data of I^2C 2-wire control interface
SDCLK	12	IN	Serial clock of I^2C 2-wire control interface
Buffer_INT	13	IN	True reference clock input
NC	14, 32,36	IN	Not connected
FB_OUTT	33	OUT	True Feedback output, dedicated for external feedback. It switches at the same frequency as the CLK. This output must be wired to FB_INT.
FB_INT	35	IN	True Feedback input, provides feedback signal to the internal PLL for synchronization with CLK_INT to eliminate phase error.

4.2 Power Pins

SYMBOL	PIN	FUNCTION
GND	1,7,8,18,24,25,31,41, 42,48	Ground
VDD	4,11,21,28,34,38,45, 15	Power Supply 2.5V
AVDD	16	Analog power supply, 2.5V
AGND	17	Analog ground

5.1 Register 0 : Control Register (1 = active, 0 = inactive)

Bit	@PowerUp	Pin	Description
7	1	2,3	CLKC0,CLKT0(Active / Inactive)
6	1	6,5	CLKC1,CLKT1(Active / Inactive)
5	1	9,10	CLKC2,CLKT2(Active / Inactive)
4	1	19,20	CLKC3,CLKT3(Active / Inactive)
3	1	23,22	CLKC4,CLKT4(Active / Inactive)
2	1	47,46	CLKC5,CLKT5(Active / Inactive)
1	1	43,44	CLKC6,CLKT6(Active / Inactive)
0	1	40,39	CLKC7,CLKT7(Active / Inactive)

5.2 Register 1: Control Register (1 = active, 0 = inactive)

Bit	@PowerUp	Pin	Description
7	1	30,29	CLKC8,CLKT8(Active / Inactive)
6	1	26,27	CLKC9,CLKT9(Active / Inactive)
5	1	-	Reserved
4	1	-	Reserved
3	1	-	Reserved
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

5.3 Register 2: Reserved Register (default =1)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	-	Reserved
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

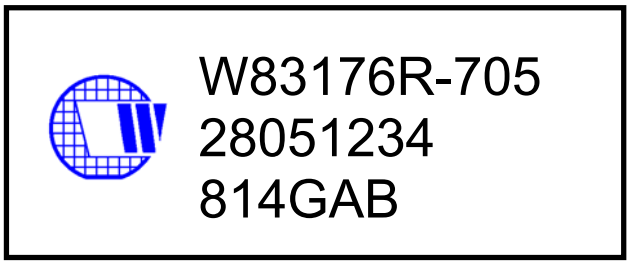
5.4 Register 3: : Reserved Register (default =1)

Bit	@PowerUp	Pin	Description
7	1	-	Reserved
6	1	-	Reserved
5	1	-	Reserved
4	1	-	Reserved
3	1	-	Reserved
2	1	-	Reserved
1	1	-	Reserved
0	1	-	Reserved

6.0 ORDERING INFORMATION

Part Number	Package Type	Production Flow
W83176R-705	48 PIN SSOP	Commercial, 0°C to +70°C

7.0 HOW TO READ THE TOP MARKING



1st line: Winbond logo and the type number: W83176R-705

2nd line: Tracking code 2 8051234

2: wafers manufactured in Winbond FAB 2

8051234: wafer production series lot number

3rd line: Tracking code 814 G B B

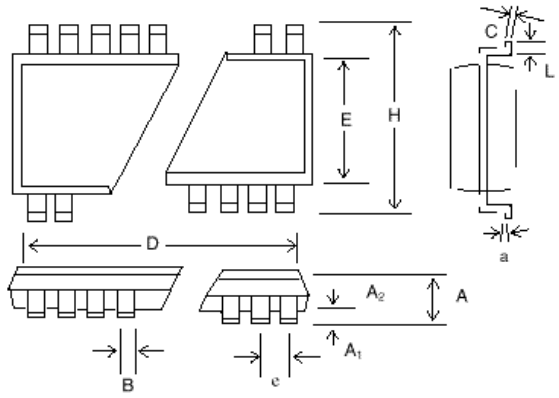
814: packages made in '98, week 14

G: assembly house ID; O means OSE, G means GR

A: Internal use code

B: IC revision

8.0 PACKAGE DRAWING AND DIMENSIONS



48 PIN SSOP OUTLINE DIMENSIONS

SYMBOL	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.110	0	0	2.79
A_1	0.008	0.012	0.016	0.20	0.30	0.41
A2	0.085	0.090	0.095	2.16	2.29	2.41
b	0.008	0.010	0.013	0.20	0.25	0.33
C	0.006	0.008	0.010	0.15	0.20	0.25
D	-	0.625	0.637	-	15.88	16.18
E	0.291	0.295	0.299	7.39	7.49	7.59
e	0.025 BSC			0.64 BSC		
H	0.395	0.408	0.420	10.03	10.36	10.67
L	0.025	0.030	0.040	0.64	0.76	1.02
a	0°	5°	8°	0°	5°	8°

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