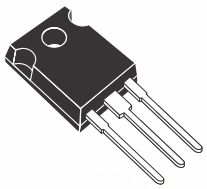
STW45NM60

N-channel 650V@Tjmax - 0.09Ω - 45A - TO-247 MDmesh™ Power MOSFET

General features

Type	V_{DSS} (@Tjmax)	$R_{DS(on)}$	I_D
STW45NM60	650V	< 0.11Ω	45A

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance
- Tight process control and high manufacturing yields

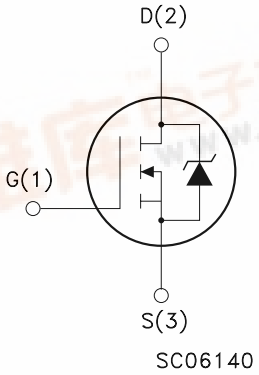


TO-247

Description

The MDmesh™ is a new revolutionary Power MOSFET technology that associates the multiple drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competitor's products.

Internal schematic diagram



Applications

- Switching application

Order codes

Part number	Marking	Package	Packaging
STW45NM60	W45NM60	TO-247	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate- source voltage	±30	V
I_D	Drain current (continuous) at T_C = 25°C	45	A
I_D	Drain current (continuous) at T_C = 100°C	28	A
I_{DM} (1)	Drain current (pulsed)	180	A
P_{TOT}	Total dissipation at T_C = 25°C	417	W
	Derating factor	3.33	W/°C
dv/dt (2)	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	–65 to 150	°C
T_j	Max. operating junction temperature	150	°C

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 45A$, di/dt ≤ 400A/µs, $V_{DD} \leq 80\%\ V_{(BR)DSS}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case	0.3	°C/W
Rthj-amb	Thermal resistance junction-amb	30	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	15	A
E_{AS}	Single pulse avalanche energy (starting T_j = 25 °C, $I_D = I_{AR}$, V_{DD} = 35 V)	850	mJ

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 250 µA, V_{GS} = 0	600			V
I_{DSS}	Zero gate voltage Drain current (V_{GS} = 0)	V_{DS} = Max rating V_{DS} = Max rating, T_C = 125 °C			10 100	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ±30V			±100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 22.5A		0.09	0.11	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} > $I_{D(on)}$ x $R_{DS(on)max}$, I_D= 22.5A		15		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} = 25V, f = 1 MHz, V_{GS} = 0		3800 1250 80		pF pF pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0V, V_{DS} = 0V to 480V		340		pF
R_G	Gate input resistance	f=1 MHz Gate DC Bias = 0 test signal level = 20mV open drain		1.4		Ω
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD} = 400V, I_D = 45A, V_{GS} = 10V *Figure 14*		96 31 43	134	nC nC nC

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on delay time Rise time	V_{DD} = 250V, I_D = 22.5A R_G = 4.7Ω V_{GS} = 10V *Figure 13*		30 20		ns ns
$t_{r(Voff)}$ t_f t_c	Off-voltage rise time Fall time Cross-over time	V_{DD} = 400V, I_D = 45A, R_G = 4.7Ω, V_{GS} = 10V *Figure 13*		16 23 40		ns ns ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)				45 180	A A
V_{SD} (1)	Forward on voltage	I_{SD} = 45A, V_{GS} = 0			1.5	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 45A, di/dt = 100A/µs, V_{DD} = 100 V, T_j = 25°C *Figure 15*		508 10 40		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 45A, di/dt = 100A/µs, V_{DD} = 100 V, T_j = 150°C *Figure 15*		650 14 43		ns µC A

1. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

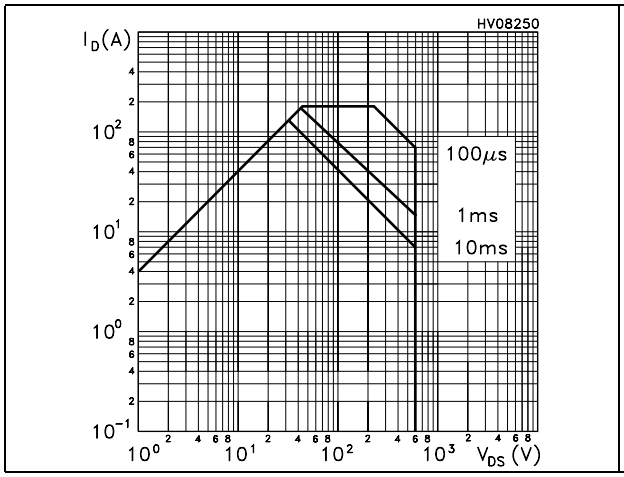


Figure 2. Thermal impedance

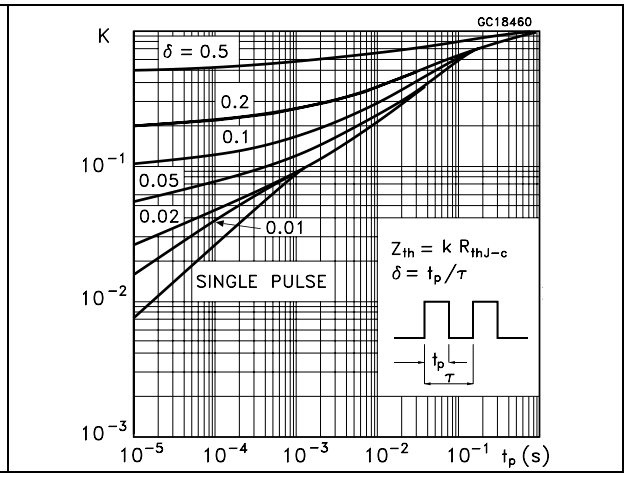


Figure 3. Output characteristics

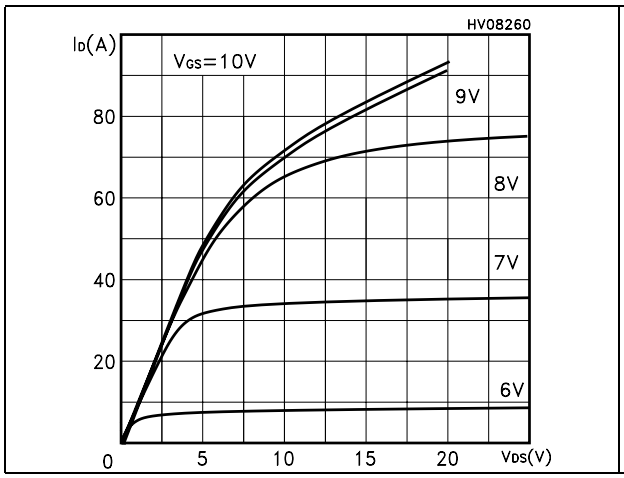


Figure 4. Transfer characteristics

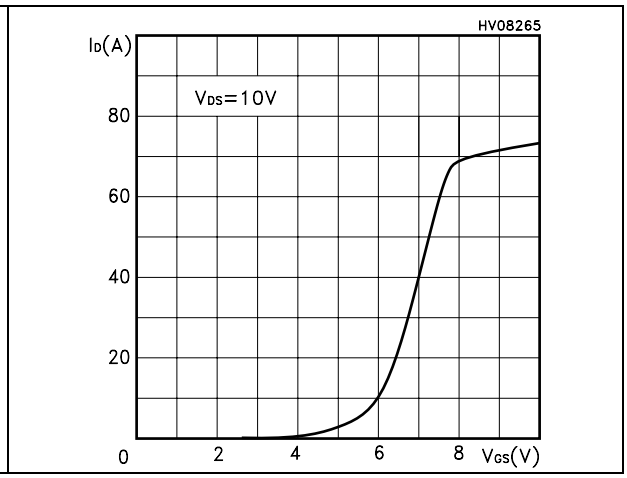


Figure 5. Transconductance

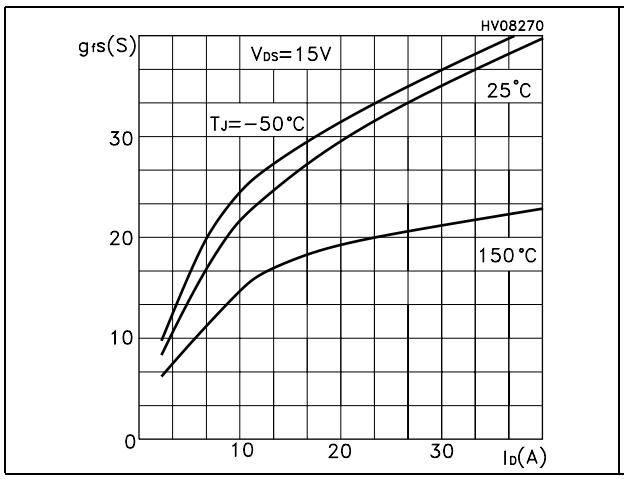


Figure 6. Static-drain source on resistance

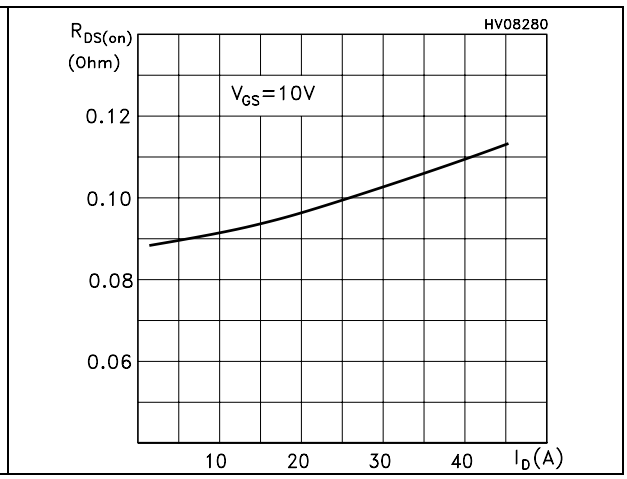


Figure 7. Gate charge vs gate-source voltage

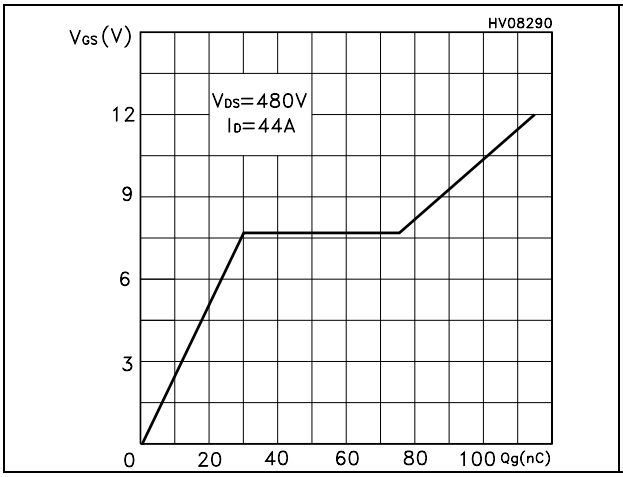


Figure 8. Capacitance variations

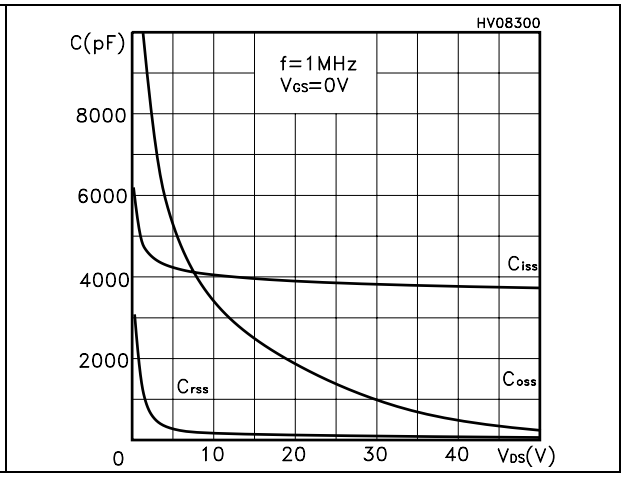


Figure 9. Normalized gate threshold voltage vs temperature

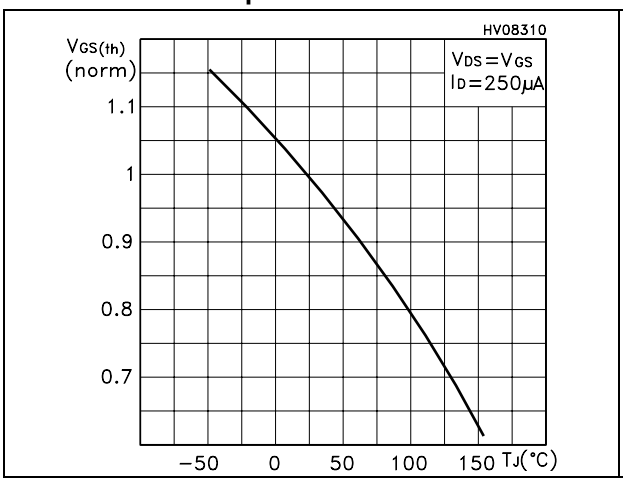


Figure 10. Normalized on resistance vs temperature

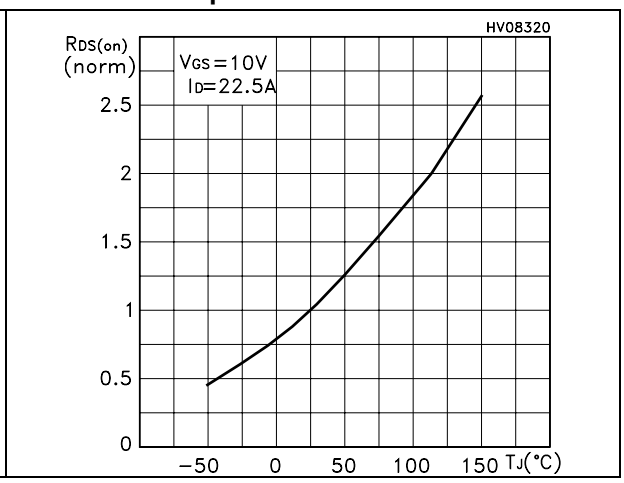


Figure 11. Source-drain diode forward characteristics

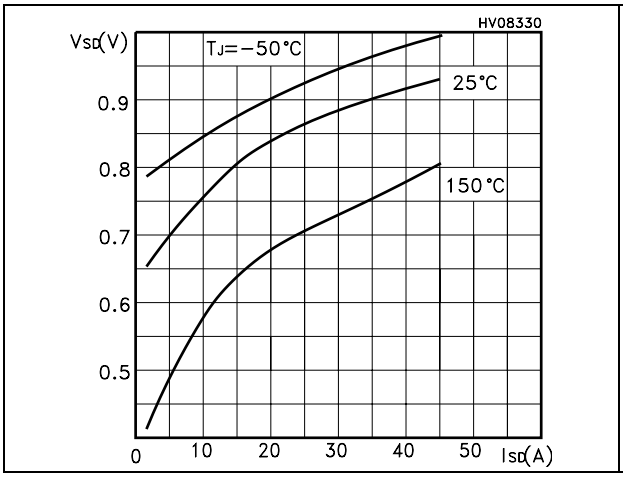
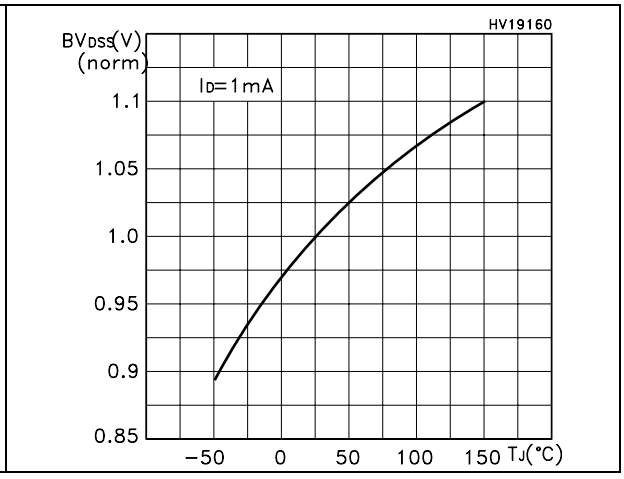


Figure 12. Normalized BV_{DSS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

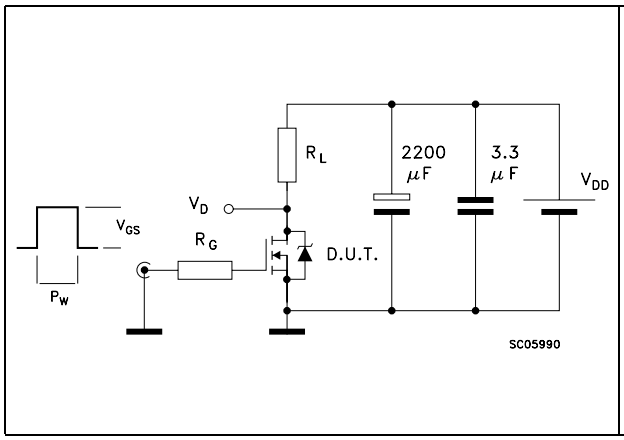


Figure 14. Gate charge test circuit

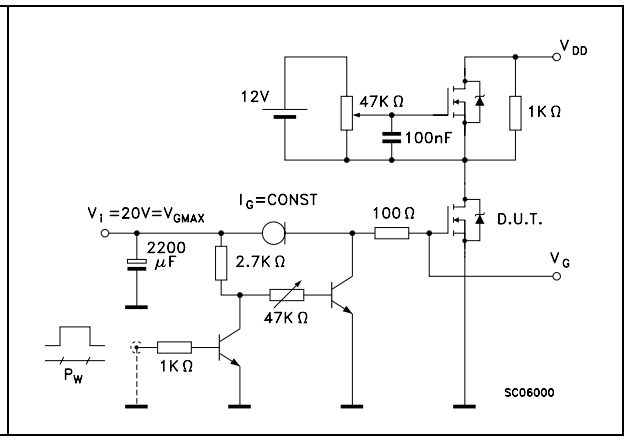


Figure 15. Test circuit for inductive load switching and diode recovery times

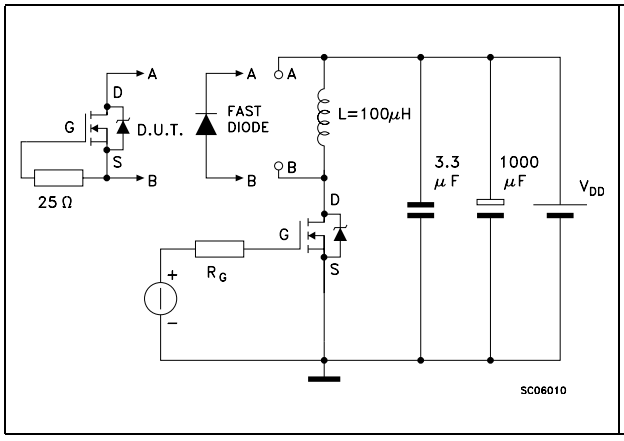


Figure 16. Unclamped inductive load test circuit

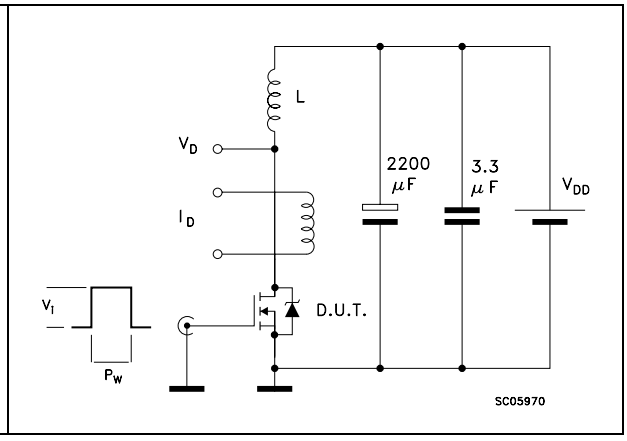


Figure 17. Unclamped inductive waveform

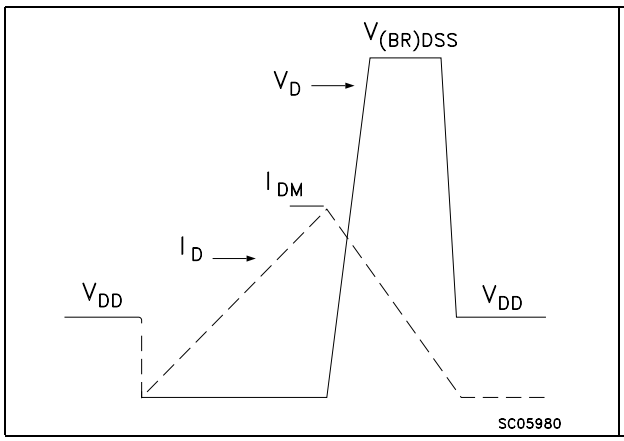
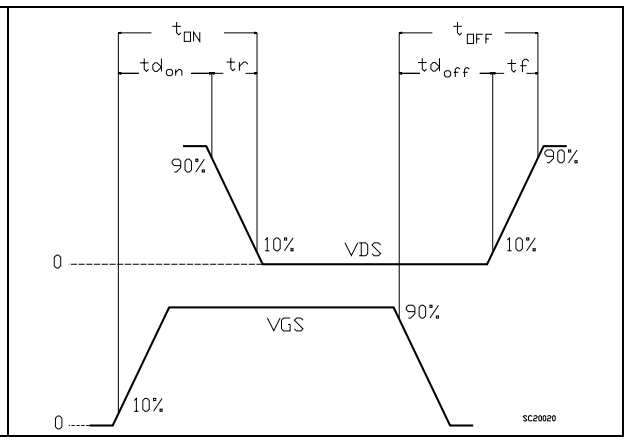


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : *www.st.com*

5 Revision history

Table 8. Revision history

Date	Revision	Changes
05-Mar-2005	5	Complete document with curves
16-May-2006	6	The document has been reformatted
18-Dec-2006	7	Updates curves:*Figure 1.*, *Figure 4.* and *Figure 6.*

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