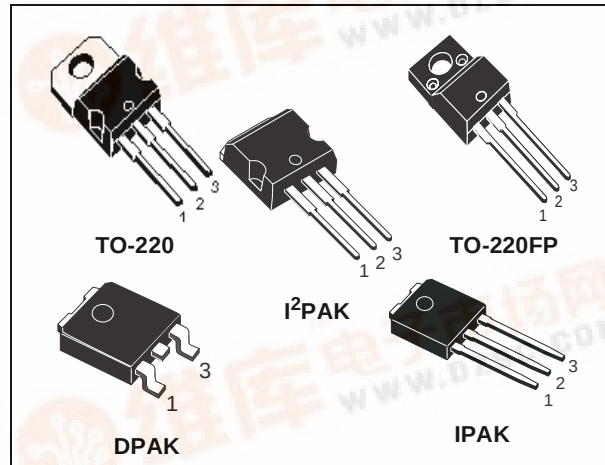




STB5NK50Z-1 - STP5NK50ZFP STP5NK50Z - STD5NK50Z - STD5NK50Z-1 N-CHANNEL 500V-1.22Ω-4.4A TO-220/FP/DPAK/IPAK/I²PAK Zener-Protected SuperMESH™ Power MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D	P _w
STP5NK50Z	500 V	< 1.5 Ω	4.4 A	70 W
STP5NK50ZFP	500 V	< 1.5 Ω	4.4 A	25 W
STD5NK50Z	500 V	< 1.5 Ω	4.4 A	70 W
STD5NK50Z-1	500 V	< 1.5 Ω	4.4 A	70 W
STB5NK50Z-1	500 V	< 1.5 Ω	4.4 A	70 W

- TYPICAL R_{DS(on)} = 1.22 Ω
- EXTREMELY HIGH dv/dt CAPABILITY
- 100% AVALANCHE TESTED
- GATE CHARGE MINIMIZED
- VERY LOW INTRINSIC CAPACITANCES
- VERY GOOD MANUFACTURING REPEATABILITY



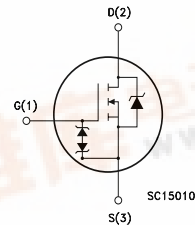
DESCRIPTION

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

APPLICATIONS

- HIGH CURRENT, HIGH SPEED SWITCHING
- IDEAL FOR OFF-LINE POWER SUPPLIES, ADAPTORS AND PFC
- LIGHTING

INTERNAL SCHEMATIC DIAGRAM



ORDERING INFORMATION

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP5NK50Z	P5NK50Z	TO-220	TUBE
STP5NK50ZFP	P5NK50ZFP	TO-220FP	TUBE
STD5NK50ZT4	D5NK50Z	DPAK	TAPE & REEL
STD5NK50Z-1	D5NK50Z	IPAK	TUBE
STB5NK50Z-1	B5NK50Z	I ² PAK	TUBE

STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value			Unit
		STP5NK50Z STB5NK50Z-1	STP5NK50ZFP	STD5NK50Z STD5NK50Z-1	
V_{DS}	Drain-source Voltage ($V_{GS} = 0$)	500			V
V_{DGR}	Drain-gate Voltage ($R_{GS} = 20\text{ k}\Omega$)	500			V
V_{GS}	Gate- source Voltage	± 30			V
I_D	Drain Current (continuous) at $T_C = 25^\circ\text{C}$	4.4	4.4 (*)	4.4	A
I_D	Drain Current (continuous) at $T_C = 100^\circ\text{C}$	2.7	2.7 (*)	2.7	A
$I_{DM}(\bullet)$	Drain Current (pulsed)	17.6	17.6 (*)	17.6	A
P_{TOT}	Total Dissipation at $T_C = 25^\circ\text{C}$	70	25	70	W
	Derating Factor	0.56	0.2	0.56	W/ $^\circ\text{C}$
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5K Ω)	3000			V
$dv/dt(1)$	Peak Diode Recovery voltage slope	4.5			V/ns
V_{ISO}	Insulation Withstand Voltage (DC)	-	2500	-	V
T_j T_{stg}	Operating Junction Temperature Storage Temperature	-55 to 150 -55 to 150			$^\circ\text{C}$ $^\circ\text{C}$

(●) Pulse width limited by safe operating area

(1) $I_{SD} \leq 4.4\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_j \leq T_{JMAX}$.

(*) Limited only by maximum temperature allowed

THERMAL DATA

		TO-220 I ² PAK	TO-220FP	PAK	
Rthj-case	Thermal Resistance Junction-case Max	1.78	5	1.78	$^\circ\text{C}/\text{W}$
Rthj-amb	Thermal Resistance Junction-ambient Max	62.5			$^\circ\text{C}/\text{W}$
T_I	Maximum Lead Temperature For Soldering Purpose	300			$^\circ\text{C}$

AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I_{AR}	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T_j max)	4.4	A
E_{AS}	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	130	mJ

GATE-SOURCE ZENER DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
BV_{GSO}	Gate-Source Breakdown Voltage	$I_{GS} = \pm 1\text{mA}$ (Open Drain)	30			V

PROTECTION FEATURES OF GATE-TO-SOURCE ZENER DIODES

The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

ELECTRICAL CHARACTERISTICS (TCASE =25°C UNLESS OTHERWISE SPECIFIED) ON/OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1 \text{ mA}$, $V_{GS} = 0$	500			V
I_{DSS}	Zero Gate Voltage Drain Current ($V_{GS} = 0$)	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}$, $T_C = 125^\circ\text{C}$			1 50	μA μA
I_{GSS}	Gate-body Leakage Current ($V_{DS} = 0$)	$V_{GS} = \pm 20\text{V}$			± 10	μA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 50\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 2.2 \text{ A}$		1.22	1.5	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (1)$	Forward Transconductance	$V_{DS} = 15 \text{ V}$, $I_D = 2.2 \text{ A}$		3.1		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25\text{V}$, $f = 1 \text{ MHz}$, $V_{GS} = 0$		535 75 17		pF pF pF
$C_{oss \text{ eq.}} (3)$	Equivalent Output Capacitance	$V_{GS} = 0\text{V}$, $V_{DS} = 0\text{V to } 400\text{V}$		45		pF

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 250 \text{ V}$, $I_D = 2.2 \text{ A}$ $R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		15 10		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 400\text{V}$, $I_D = 4.4 \text{ A}$, $V_{GS} = 10\text{V}$		20 4 10	28	nC nC nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 250 \text{ V}$, $I_D = 2.2\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10 \text{ V}$ (Resistive Load see, Figure 3)		32 15		ns ns
$t_r(V_{off})$ t_f t_c	Off-voltage Rise Time Fall Time Cross-over Time	$V_{DD} = 400\text{V}$, $I_D = 4.4\text{A}$, $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$ (Inductive Load see, Figure 5)		12 12 20		ns ns ns

SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} $I_{SDM} (2)$	Source-drain Current Source-drain Current (pulsed)				4.4 17.6	A A
$V_{SD} (1)$	Forward On Voltage	$I_{SD} = 4.4 \text{ A}$, $V_{GS} = 0$			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 4.4 \text{ A}$, $di/dt = 100\text{A}/\mu\text{s}$ $V_{DD} = 30\text{V}$, $T_J = 150^\circ\text{C}$ (see test circuit, Figure 5)		310 1425 9.2		ns nC A

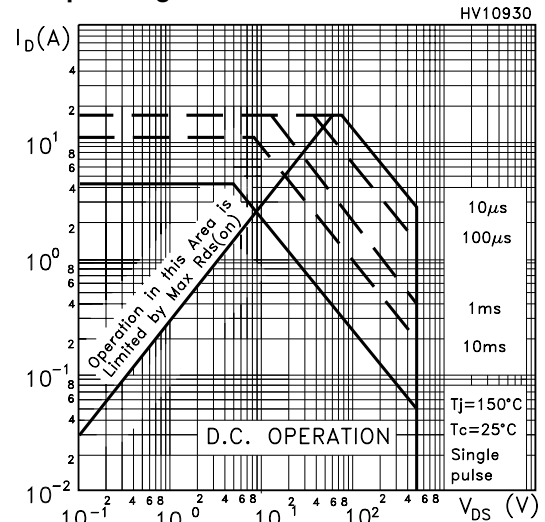
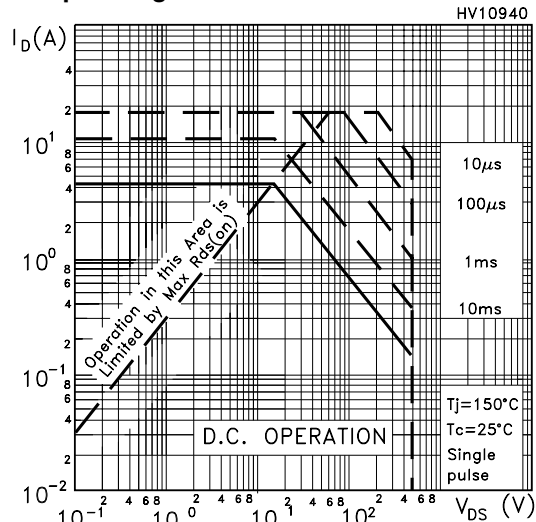
Note: 1. Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.

2. Pulse width limited by safe operating area.

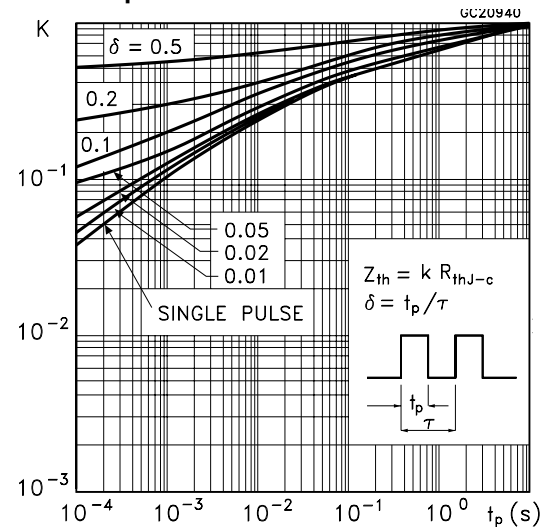
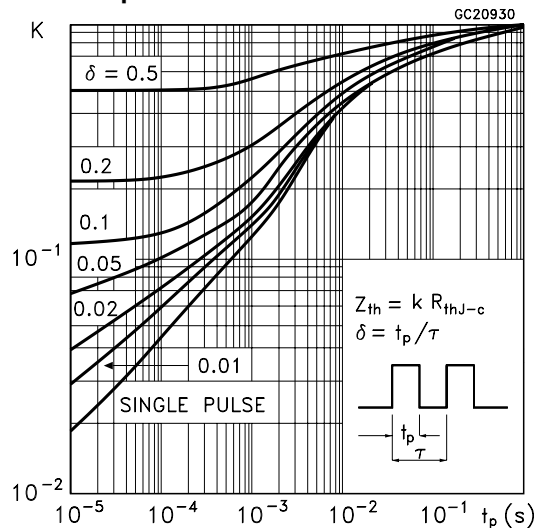
3. $C_{oss \text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

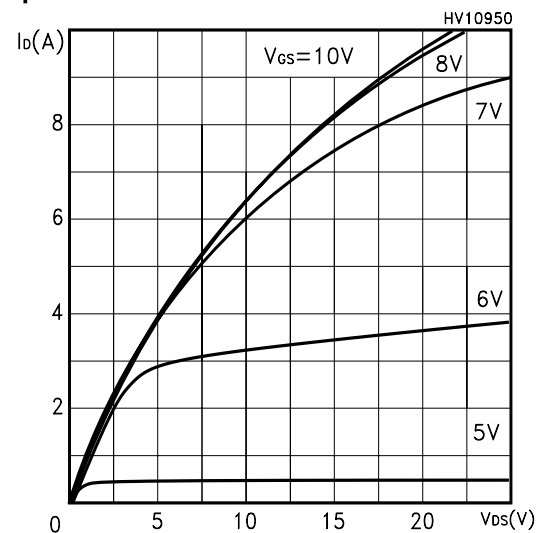
Safe Operating Area For TO-220/DPAK/IPAK/I2PAK Safe Operating Area For TO-220FP



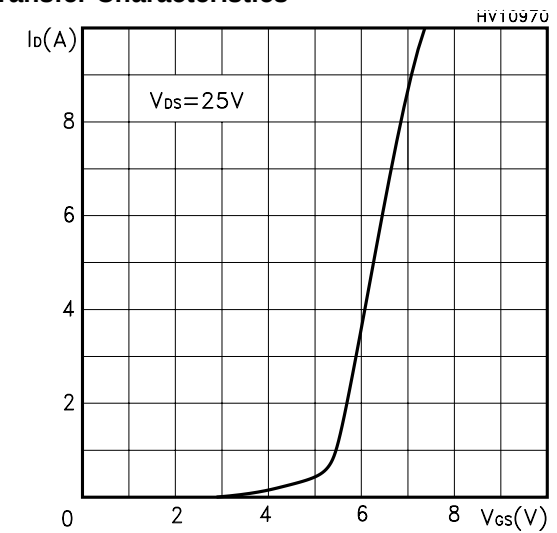
Thermal Impedance For TO-220/DPAK/IPAK/I2PAK Thermal Impedance For TO-220FP



Output Characteristics

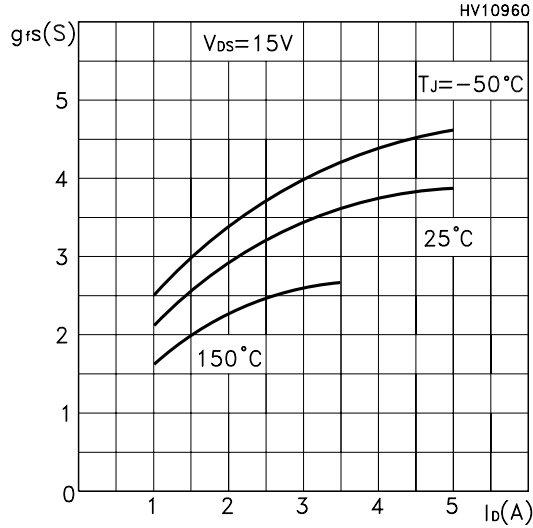


Transfer Characteristics

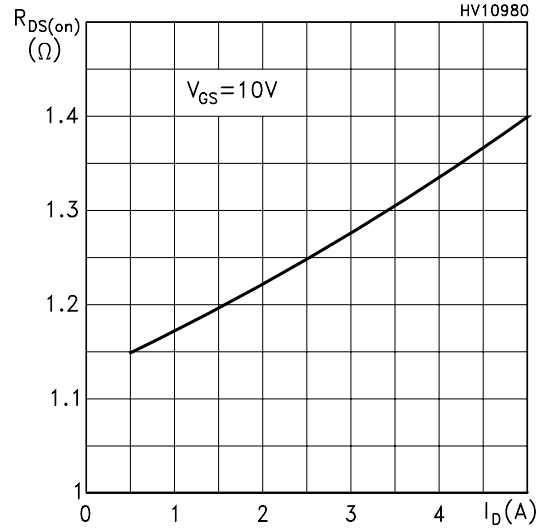


STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

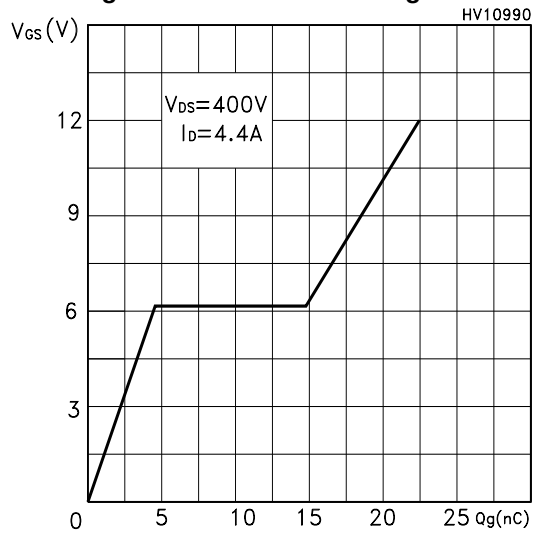
Transconductance



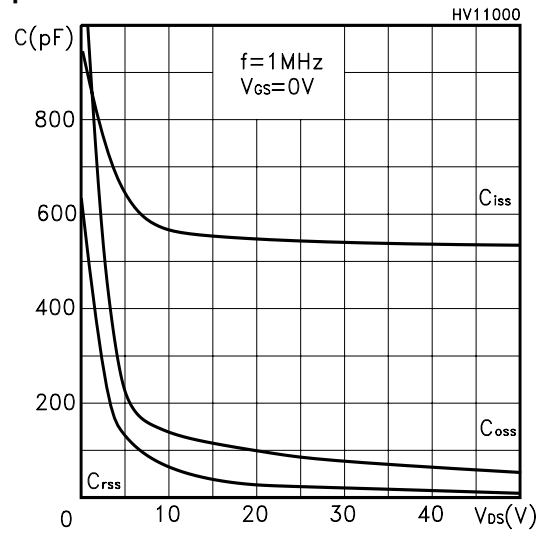
Static Drain-source On Resistance



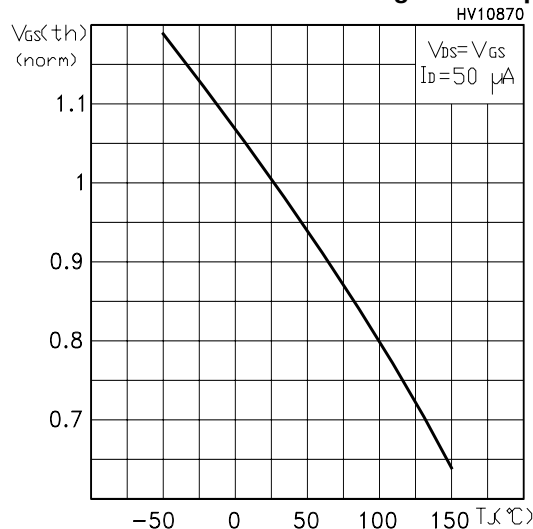
Gate Charge vs Gate-source Voltage



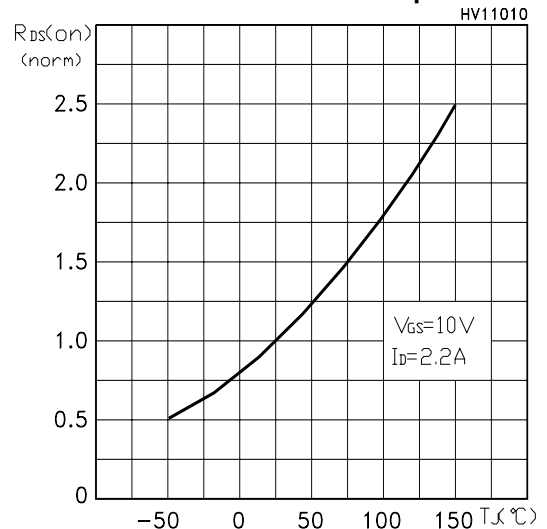
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.

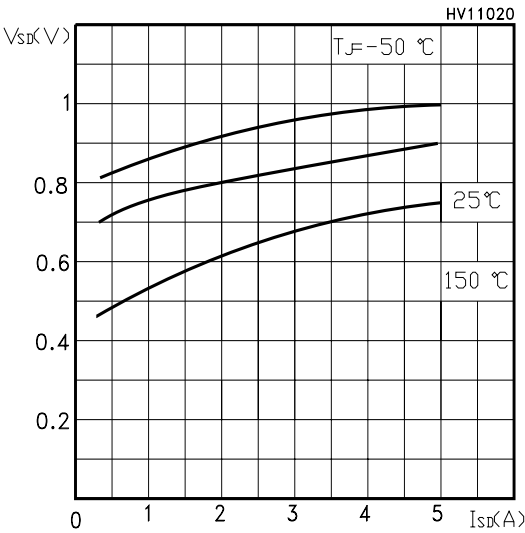


Normalized On Resistance vs Temperature

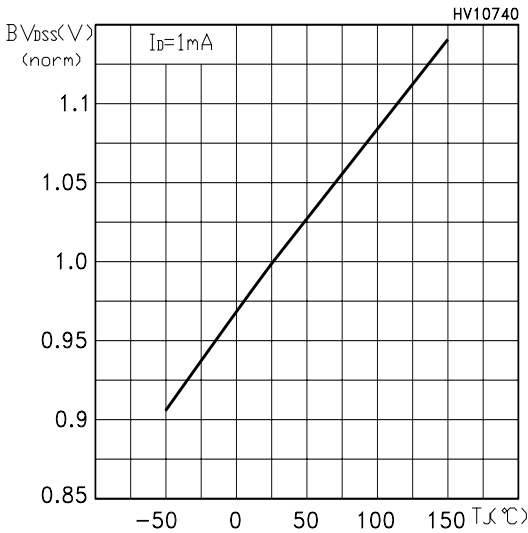


STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

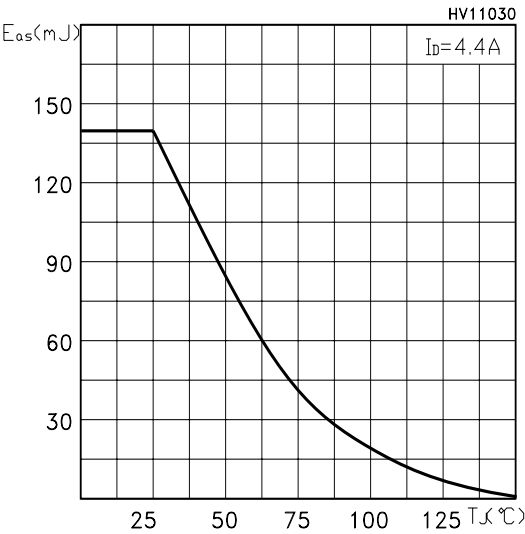
Source-drain Diode Forward Characteristics



Normalized BVDSS vs Temperature



Maximum Avalanche Energy vs Temperature



STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

Fig. 1: Unclamped Inductive Load Test Circuit

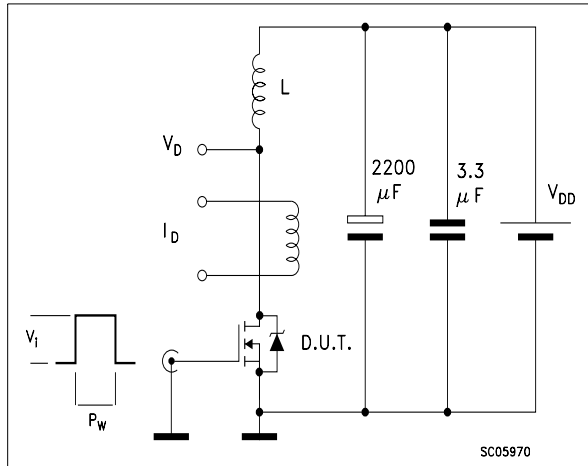


Fig. 2: Unclamped Inductive Waveform

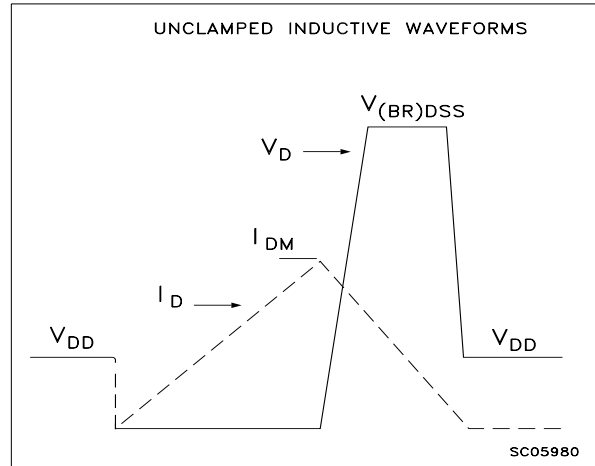


Fig. 3: Switching Times Test Circuit For Resistive Load

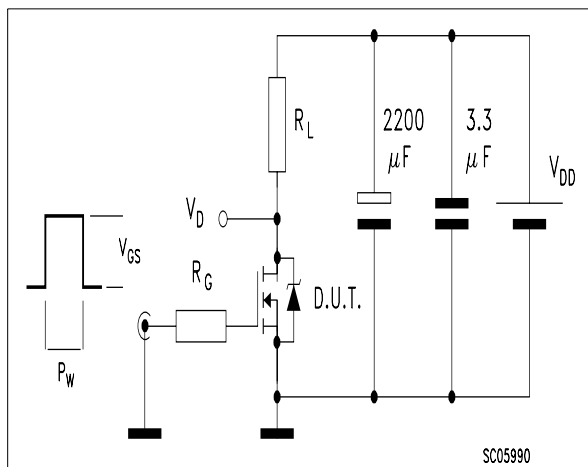


Fig. 4: Gate Charge test Circuit

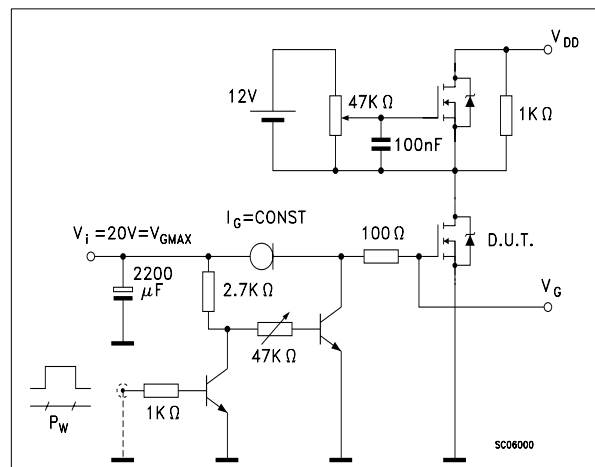
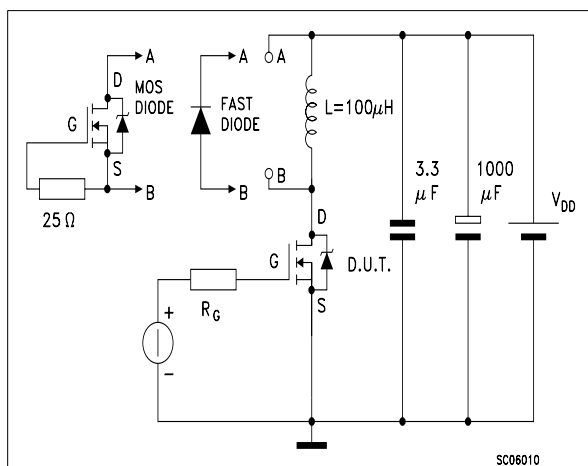


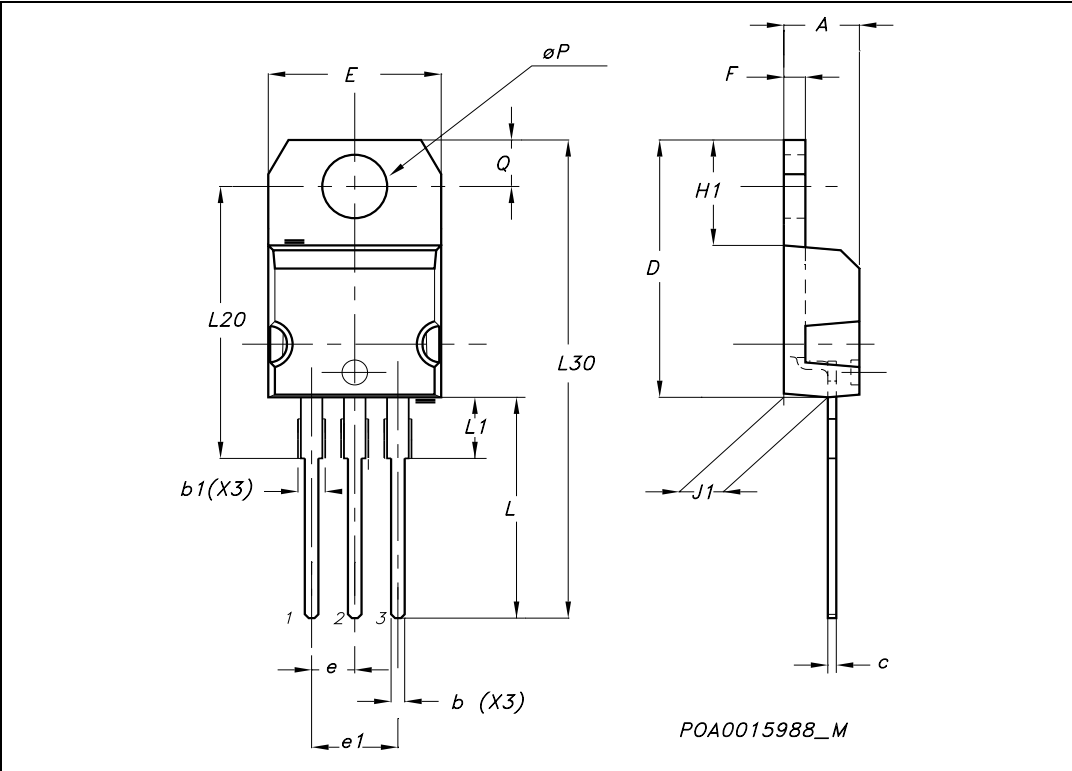
Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

TO-220 MECHANICAL DATA

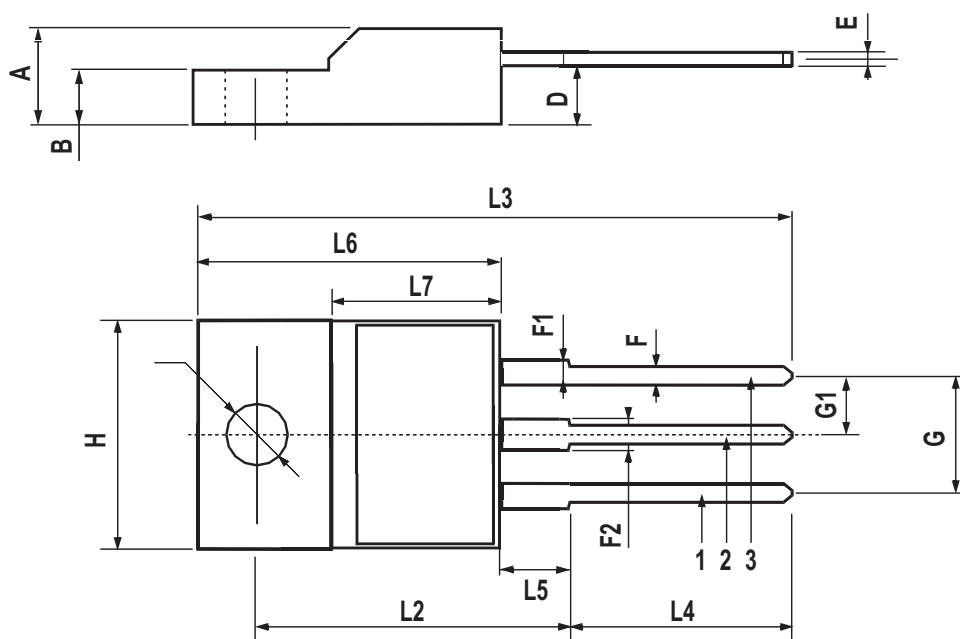
DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

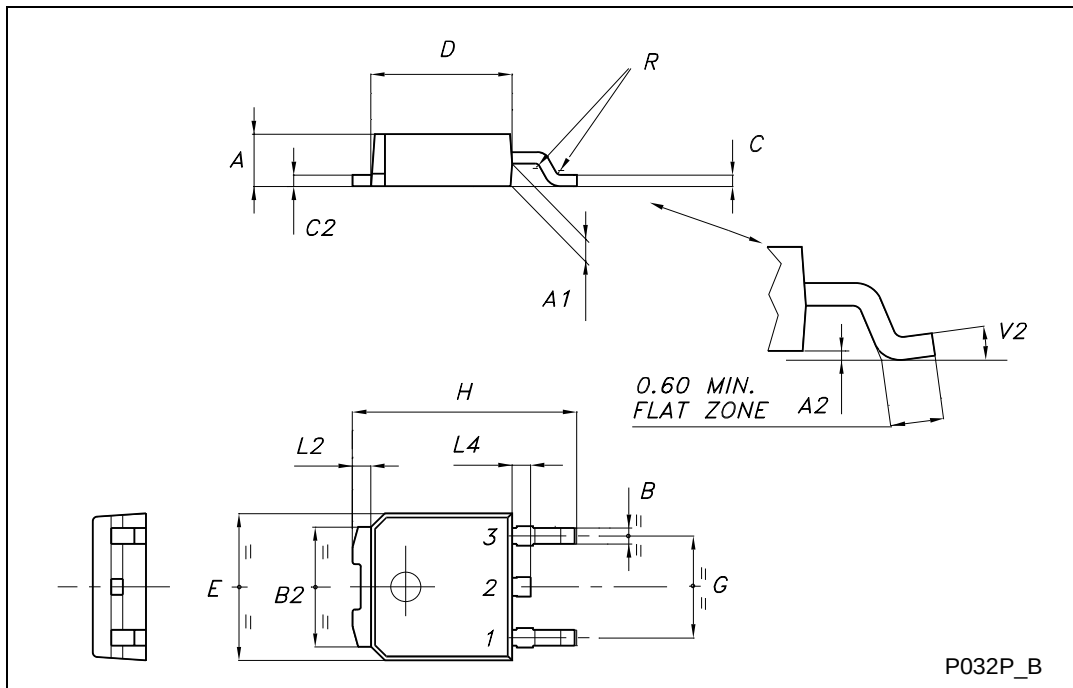
TO-220FP MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.5	0.045		0.067
F2	1.15		1.5	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	.0385		0.417
L5	2.9		3.6	0.114		0.141
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
Ø	3		3.2	0.118		0.126



TO-252 (DPAK) MECHANICAL DATA

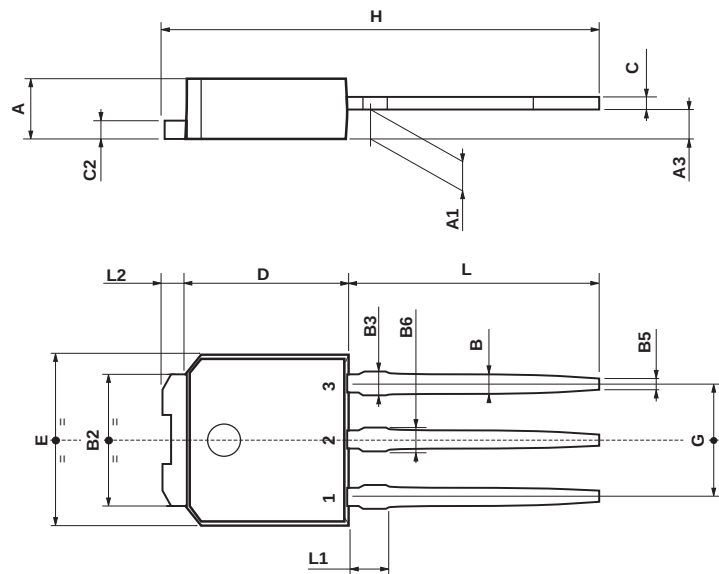
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



STP5NK50Z - STP5NK50ZFP - STD5NK50Z - STD5NK50Z-1 - STB5NK50Z-1

TO-251 (IPAK) MECHANICAL DATA

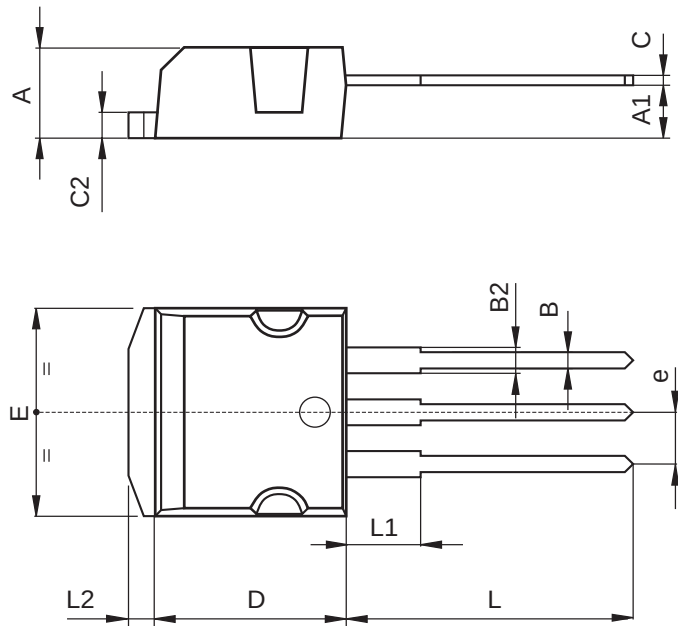
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



0068771-E

TO-262 (I²PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
e	2.4		2.7	0.094		0.106
E	10		10.4	0.393		0.409
L	13.1		13.6	0.515		0.531
L1	3.48		3.78	0.137		0.149
L2	1.27		1.4	0.050		0.055



P011P5/E

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