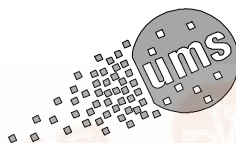


**united
monolithic
semiconductors**



CHA3694-QDG
RoHS COMPLIANT

31-40GHz Variable Gain Amplifier *Preliminary*

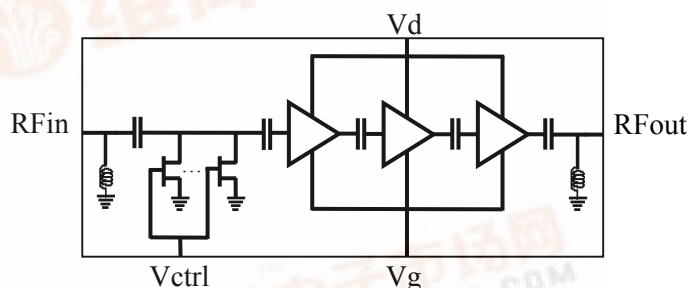
GaAs Monolithic Microwave IC in SMD package

Description

The CHA3694-QDG is a variable gain broadband three-stage monolithic amplifier.

It is designed for a wide range of applications, typically commercial communication systems.

The circuit is manufactured with a Power pHEMT process, 0.15 μ m gate length, via holes through the substrate and air bridges.

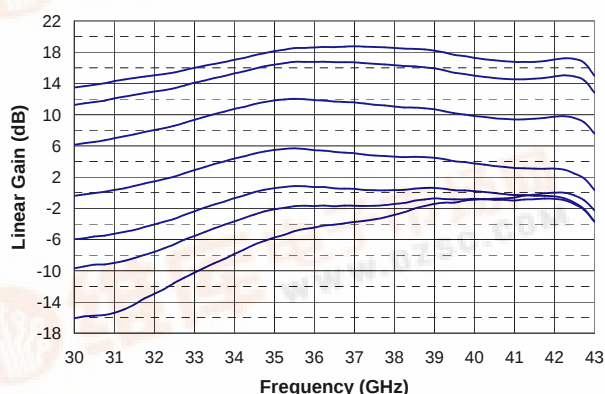


It is available in lead-free SMD package.

Main Features

- Broadband performance 31-40GHz
- 18dB gain
- 25dBm output IP3
- 19dB gain control range
- 24LQFN4x4
- ESD protected (see page 9)

On board measurements



Main Characteristics

Tamb. = +25°C, Vd = +3.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	31		40	GHz
G	Small signal gain		18		dB
Gc	Gain control range		19		dB
OIP3	3 rd order output intercept point @ max. gain		25		dBm

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

Electrical Characteristics

Tamb. = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	31		40	GHz
G	Nominal gain @ max. gain (Vctrl=-1.5V) (31-34GHz)		15		dB
	Nominal gain @ max. gain (Vctrl=-1.5V) (34-40GHz)		18		dB
NF	Noise figure @ nominal gain (31-34GHz)		10		dB
	Noise figure @ nominal gain (37-40GHz)		8		dB
RLin	Input Return loss (any attenuation) (31-34GHz)		-4		dB
	Input Return loss (any attenuation) (37-40GHz)		-7		dB
RLout	Output Return loss (any attenuation) (31-34GHz)		-7		dB
	Output Return loss (any attenuation) (37-40GHz)		-5		dB
OIP3	3 rd order output intercept point @ nominal gain		25		dBm
P1dB	Output power at 1dB gain compression @ nominal gain		17		dBm
Gc	Gain control range (31-34GHz)		25		dB
	Gain control range (37-40GHz)		19		dB
Vd	Drain bias voltage		3.5		V
Id	Drain bias current (*)		160		mA
Id P1dB	Drain current at 1dB gain compression		180		mA
Vg	Gate bias voltage		-1		V
Vctrl	Variable gain control voltage	-1.5		+0.6	V

(*) Id not affected by Vctrl.

These values are representative of on board measurements as defined on the drawing 96270 (see page 10).

Absolute Maximum Ratings (1)

Tamb. = +25°C

Symbol	Parameter	Values	Unit
Vd	Maximum drain bias voltage	4	V
Id	Maximum quiescent bias current	200	mA
Vg	Gate bias voltage	-2.0 to +0.4	V
Vctrl	Variable gain control voltage	-2.0 to +1.0	V
Pin	Maximum RF input power overdrive @ 3.5V	5	dBm
Tch	Maximum channel temperature (2)	175	°C
Ta	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Thermal Resistance channel to ground paddle =156.6°C/W for Tamb. = +85°C, Vd= +3.5V & Id= 160mA.

Typical Package Sij parameters for Vctrl= -1.5V

Preliminary

Tamb. = +25°C, Vd = +3.5V, Id = 160mA

Freq (GHz)	dB(S11)	Ph(S11) (°)	dB(S12)	Ph(S12) (°)	dB(S21)	Ph(S21) (°)	dB(S22)	Ph(S22) (°)
2,0	-0,4	144	-51,6	-41	-54,8	-83	-4,7	122
3,0	-0,4	127	-49,2	-58	-48,2	-25	-6,5	147
4,0	-0,5	109	-48,4	-104	-45,3	-90	-1,1	119
5,0	-0,6	89	-49,8	-137	-46,0	-147	-1,2	85
6,0	-2,3	67	-52,4	-169	-42,3	103	-2,5	60
7,0	-1,1	64	-53,0	167	-38,2	-52	-3,7	40
8,0	-0,8	42	-52,8	130	-32,5	-99	-4,8	20
9,0	-0,9	22	-53,7	93	-24,8	-146	-6,5	3
10,0	-1,0	2	-55,0	54	-17,7	152	-8,2	-5
11,0	-1,1	-19	-57,2	27	-12,7	85	-7,6	-11
12,0	-1,3	-41	-59,1	-28	-9,4	20	-6,3	-27
13,0	-1,7	-64	-62,0	-55	-6,9	-43	-5,3	-48
14,0	-2,2	-88	-65,5	-168	-5,0	-102	-4,4	-69
15,0	-3,2	-115	-56,7	-168	-3,5	-159	-3,7	-91
16,0	-5,5	-144	-52,8	121	-2,1	147	-3,2	-112
17,0	-11,0	-172	-52,0	77	-1,0	93	-2,9	-133
18,0	-21,5	-112	-50,2	71	-0,2	42	-2,9	-153
19,0	-10,8	-93	-50,3	62	0,7	-5	-3,1	-174
20,0	-7,1	-115	-47,9	41	2,1	-49	-3,6	164
21,0	-5,6	-137	-48,8	14	4,1	-96	-4,5	138
22,0	-4,9	-157	-52,7	2	6,4	-146	-6,1	109
23,0	-4,8	-174	-54,3	21	8,5	159	-8,3	71
24,0	-5,0	170	-48,9	20	10,0	101	-10,9	24
25,0	-5,2	157	-47,1	32	10,8	43	-12,4	-32
26,0	-5,3	146	-46,0	2	11,3	-13	-11,5	-82
27,0	-5,2	135	-43,5	-6	11,6	-65	-10,4	-122
28,0	-5,3	123	-43,8	-19	12,1	-117	-9,2	-155
29,0	-5,4	112	-42,6	-34	12,7	-169	-8,0	175
30,0	-5,7	103	-41,4	-59	13,5	137	-7,0	145
31,0	-5,3	95	-41,0	-86	14,3	84	-6,9	114
31,5	-4,7	89	-45,1	-127	14,7	56	-6,9	101
32,0	-4,3	82	-53,4	-150	15,0	28	-7,4	85
32,5	-4,3	75	-57,5	49	15,4	1	-8,4	74
33,0	-4,1	70	-45,2	-30	16,0	-27	-9,2	65
33,5	-3,8	61	-43,5	-20	16,5	-56	-10,8	56
34,0	-3,5	53	-42,4	-52	17,0	-86	-12,7	50
34,5	-3,5	42	-42,6	-54	17,6	-116	-16,0	60
35,0	-3,5	31	-41,2	-60	18,1	-148	-17,0	94
35,5	-3,8	20	-39,5	-61	18,5	179	-13,2	106
36,0	-4,5	7	-37,5	-76	18,6	145	-10,5	100
36,5	-5,4	-5	-37,4	-82	18,7	112	-8,7	95
37,0	-6,7	-15	-38,5	-88	18,8	78	-7,2	89
37,5	-8,3	-27	-39,1	-104	18,7	44	-6,3	81
38,0	-10,4	-39	-39,0	-95	18,5	9	-6,0	70
38,5	-13,5	-45	-40,1	-100	18,4	-26	-5,7	63
39,0	-15,6	-47	-40,9	-106	18,2	-63	-5,4	56
39,5	-17,3	-41	-41,0	-111	17,7	-100	-5,5	45
40,0	-17,8	-34	-38,5	-94	17,3	-137	-5,4	34
41,0	-17,6	-81	-34,4	-109	16,8	147	-7,5	1
42,0	-18,1	-110	-30,5	-133	17,1	56	-10,9	-67
43,0	-7,3	-167	-29,1	173	15,0	-82	-11,9	161
44,0	-4,8	139	-35,2	121	-0,4	146	-7,9	170
45,0	-3,0	102	-43,2	73	-18,9	80	-3,2	134
46,0	-2,8	78	-46,5	160	-39,6	36	-2,4	110
47,0	-2,8	54	-38,7	-131	-36,8	-111	-1,8	95
48,0	-3,5	32	-34,0	-174	-30,0	-174	-1,7	81
49,0	-5,1	11	-30,6	140	-27,4	140	-1,5	62
50,0	-11,5	5	-28,5	83	-27,5	84	-2,4	38

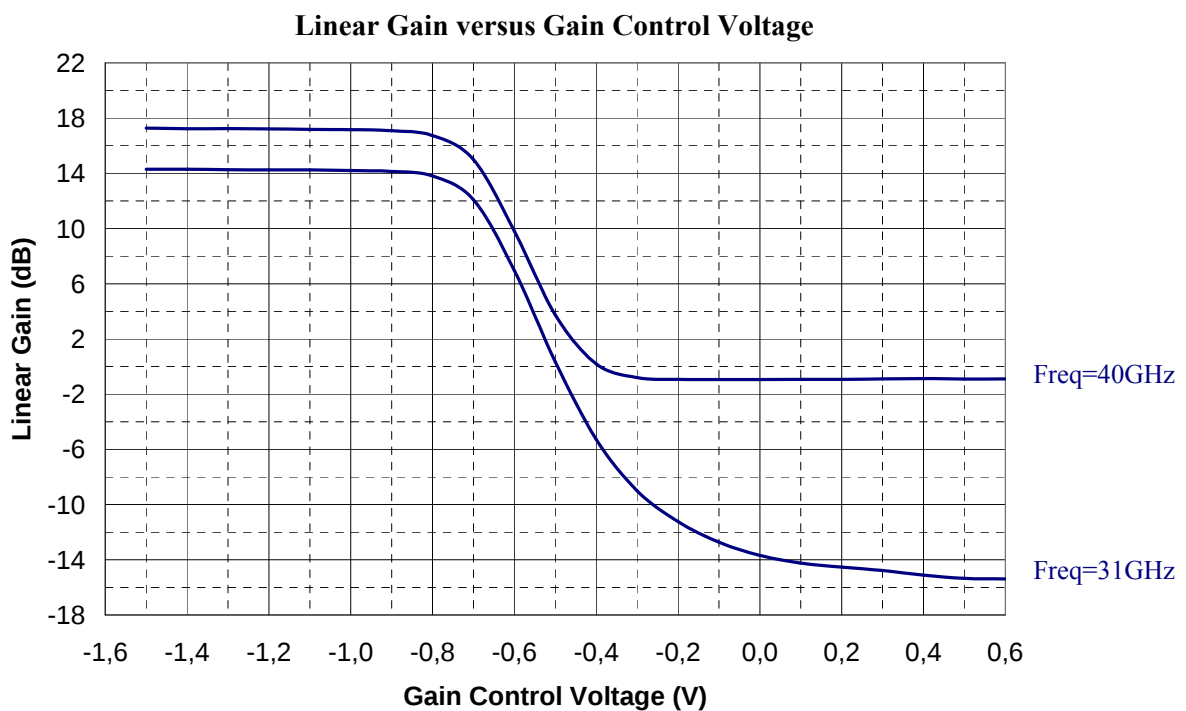
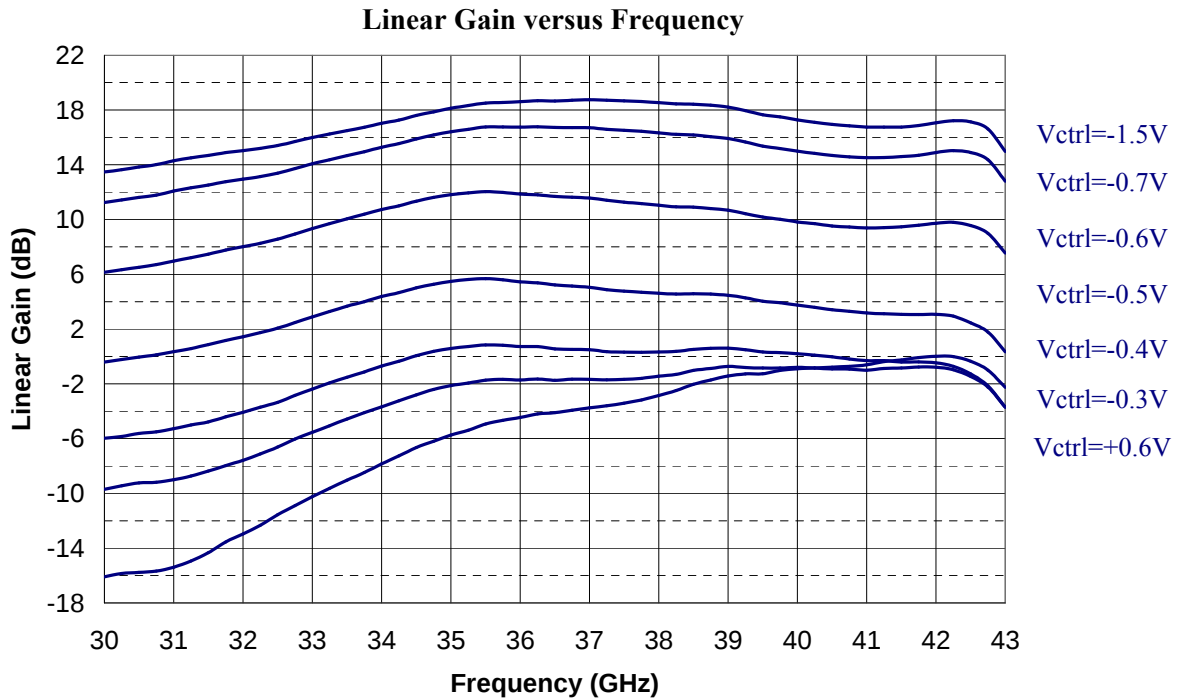
Refer to the "definition of the Sij reference planes" section below.

Typical Measured Performance

Preliminary

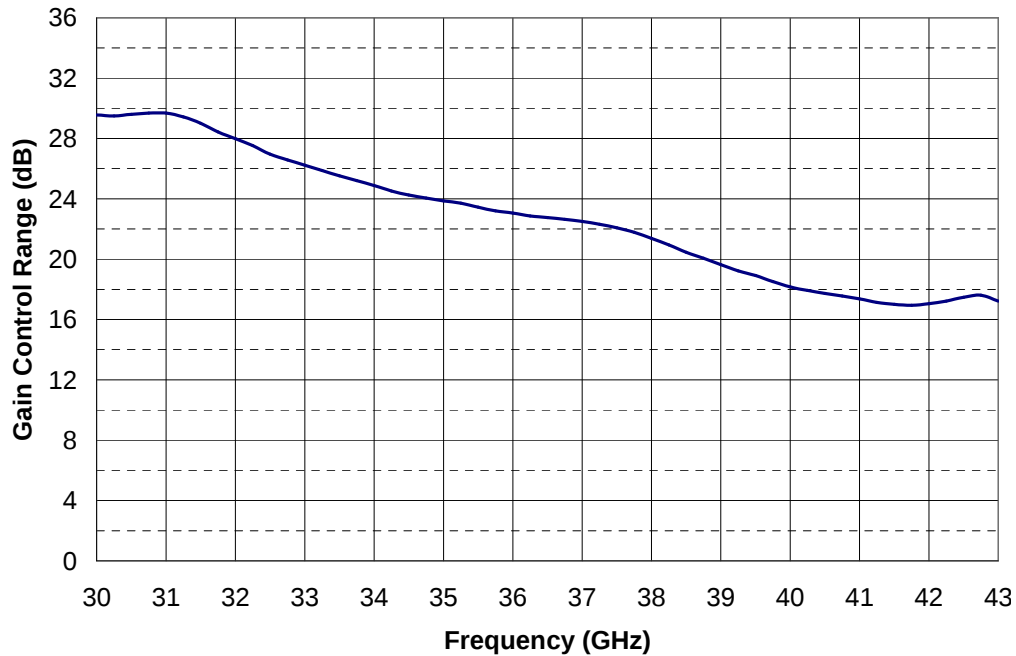
Tamb. = +25°C, Vd = +3.5V, Vg tuned for Id = 160mA

Measurements in the package access planes, using the proposed land pattern & board 96270, as defined page 10.

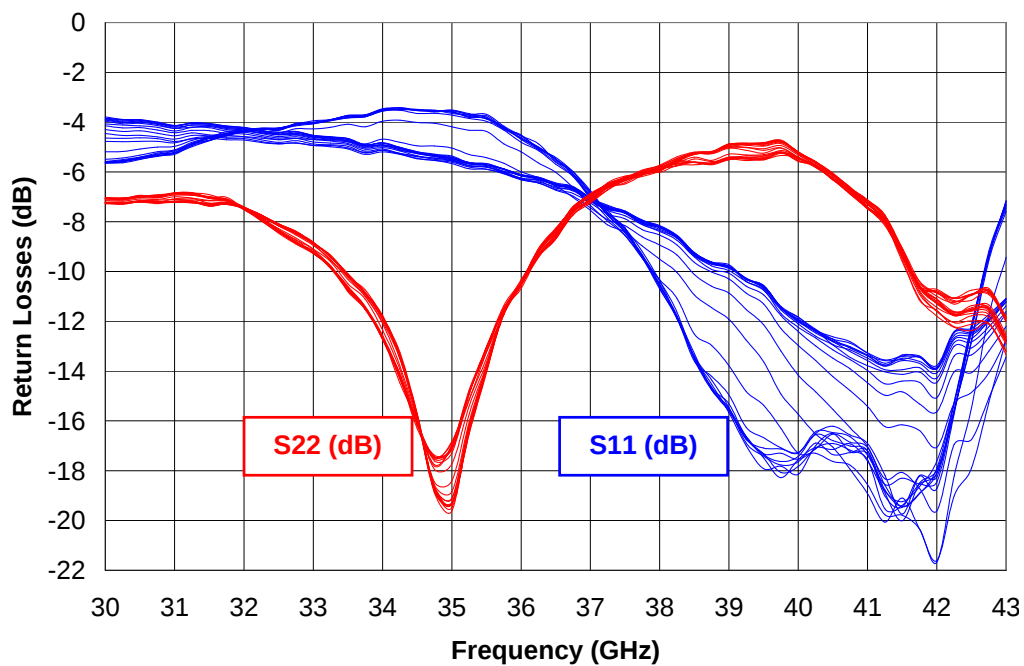


Preliminary

Gain Control Range versus Frequency

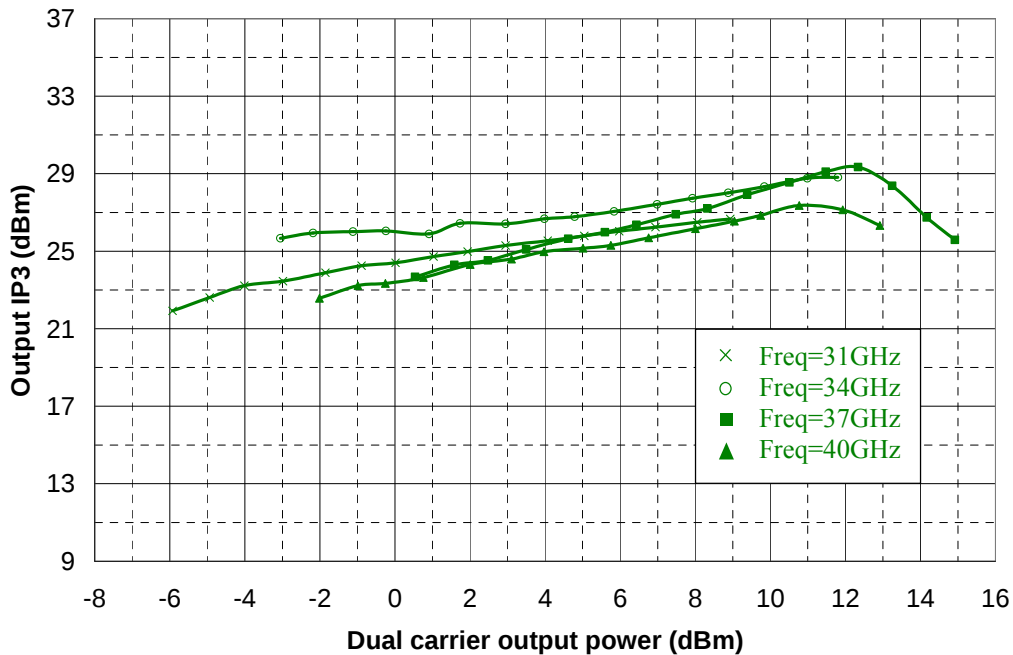


Return Losses versus Frequency and Gain Control Voltage

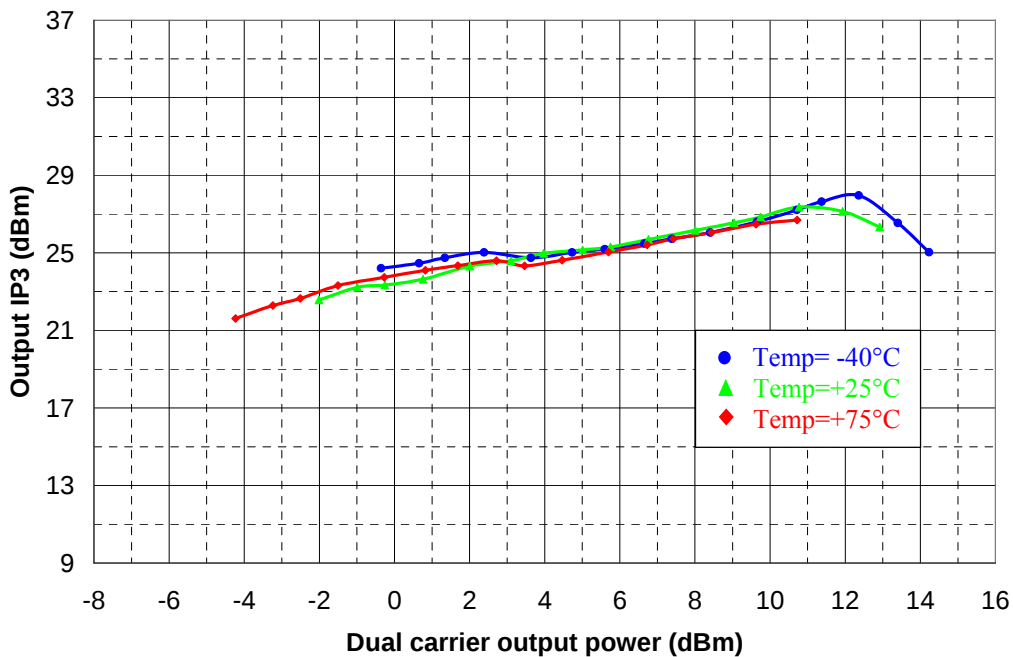


Measurements in the connector access planes (losses not deembedded), using the proposed land pattern & board 96270, as defined page 10.

Output IP3 versus Dual Carrier Output Power for Nominal Gain @ 25°C



Output IP3 versus Dual Carrier Output Power for Nominal Gain @ 40GHz



31-40GHz Variable Gain Amplifier

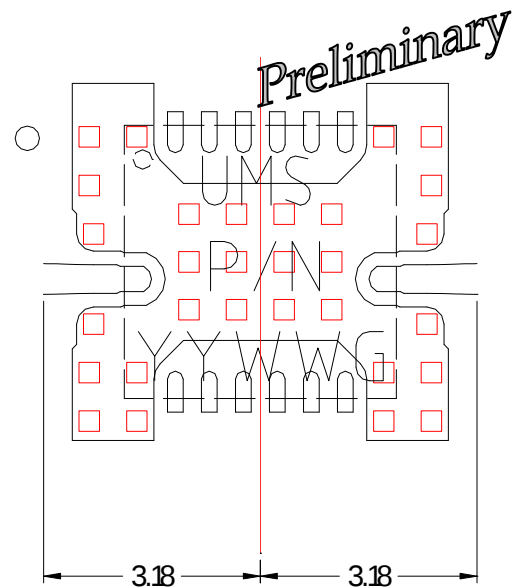
Preliminary



1- Nc	9- Nc	17- Gnd	25- GND Exposed Pad
2- Gnd	10- Vctrl	18- Nc	
3- Gnd	11- VG	19- Nc	
4- RF IN	12- Nc	20- Nc	
5- Gnd	13- Gnd	21- VD	
6- Gnd	14- Gnd	22- Nc	
7- Nc	15- RF OUT	23- Nc	
8- Nc	16- Gnd	24- Nc	

Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board 96270 shown beside. The reference is the symmetrical axis of the package. The input and output reference planes are located at 3.18mm offset (input wise and output wise respectively) from this axis. Then, the given Sij incorporates this land pattern.



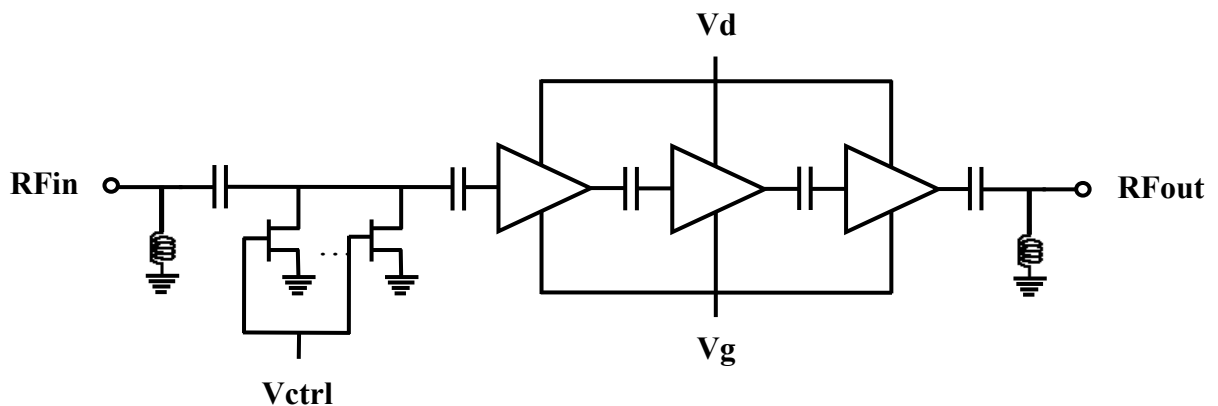
SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Note

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.

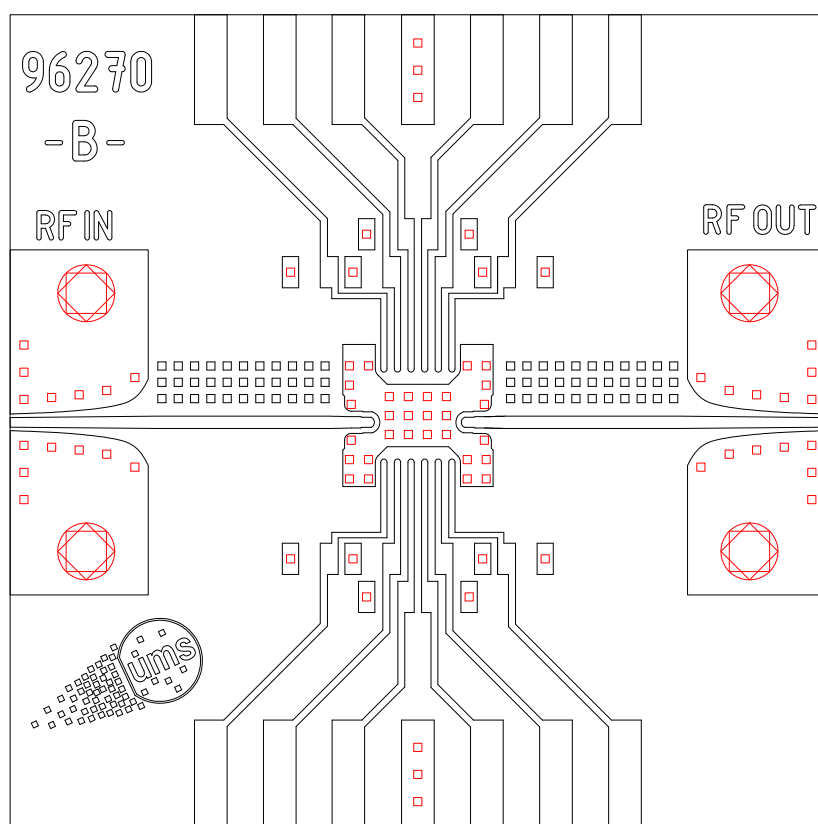


ESD protections are also implemented on gate and control accesses.

The DC connections do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling (10nF) on the PC board, as close as possible to the package.

Proposed Assembly board "96270" for the 24L-QFN4x4 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Ordering Information

QFN 4x4 RoHS compliant package: CHA3694-QDG/XY
Stick: XY = 20 Tape & reel: XY = 21

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