

7-16GHz Medium Power Amplifier

preliminary

GaAs Monolithic Microwave IC in SMD package

Description

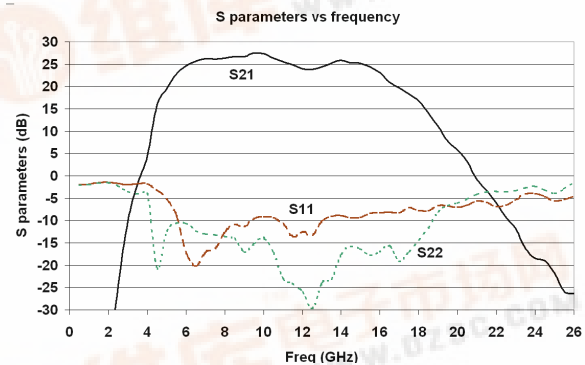
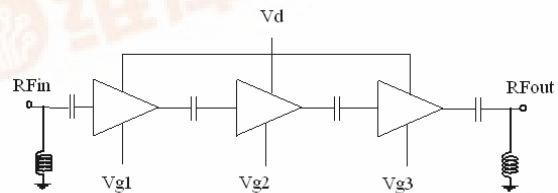
The CHA5051-QDG is a high gain three-stage monolithic medium power amplifier. It is designed for a wide range of applications, from military to commercial communication systems.

The circuit is manufactured with a pHEMT process, 0.15µm gate length, via holes through the substrate.

It is supplied in lead-free SMD package

Main Features

- Broadband performance 7-16GHz
- 25dB gain & 3.2dB noise figure
- RF ports ESD protected (see page 8)
- 25dBm output power @ 1dB compression
- DC power consumption, 310mA @ 4.5V
- 24LQFN4x4



Typical on board measurements

Main Characteristics

Tamb. = 25°C, Vd = 4.5V

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		16	GHz
G	Small signal gain		25		dB
NF	Noise figure		3.2		dB
P1dB	Output power at 1dB gain compression		25		dBm
Id	Bias current		310		mA

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!



Electrical Characteristics

Tamb.=25°C, Vd=4.5V and Id=310mA

These values are representative of on board measurements as defined on the drawing 96270B

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Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	7		16	GHz
G	Small signal gain		25		dB
P1dB	Pulsed output power at 1dB compression		25		dBm
P03	Output power at 3dB gain compression		26		dBm
NF	Noise Figure		3.2		dB
VSWRin	Input VSWR		2.0:1		
VSWRout	Output VSWR		2.0:1		
IP3	Output IP3 from 7 to 12GHz from 13 to 16 GHz		32 29		dBm
Vd	DC voltage		4.5		V
Id	Bias current		310		mA

Absolute Maximum Ratings

Tamb.=25°C (1)

Symbol	Parameter	Values	Unit
Vd	Maximum Drain bias voltage	+5	V
Id	Power supply quiescent current	390	mA
Vg	Gate bias voltage	-2 to +0.4	V
Pin	Maximum input power overdrive(2)	+10	dBm
Tj	Maximum channel temperature (3)	+175	°C
Top	Operating temperature range	-40 to +80	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

(2) Duration < 1s.

(3) Thermal Resistance channel to ground paddle =67.6°C/W for T_{paddle}. =+80°C

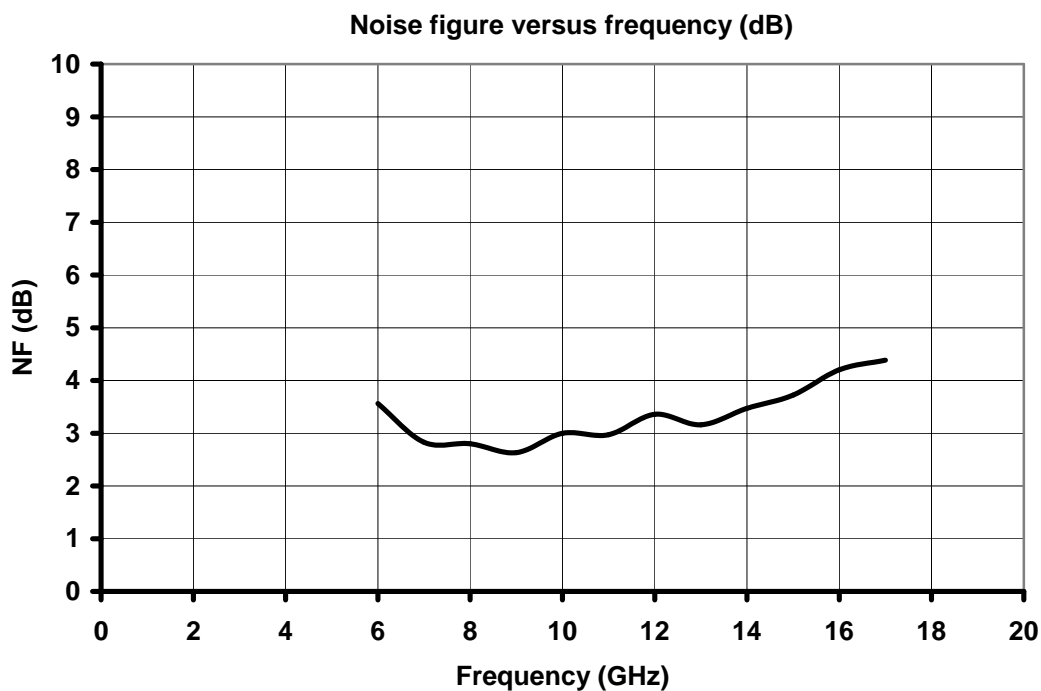
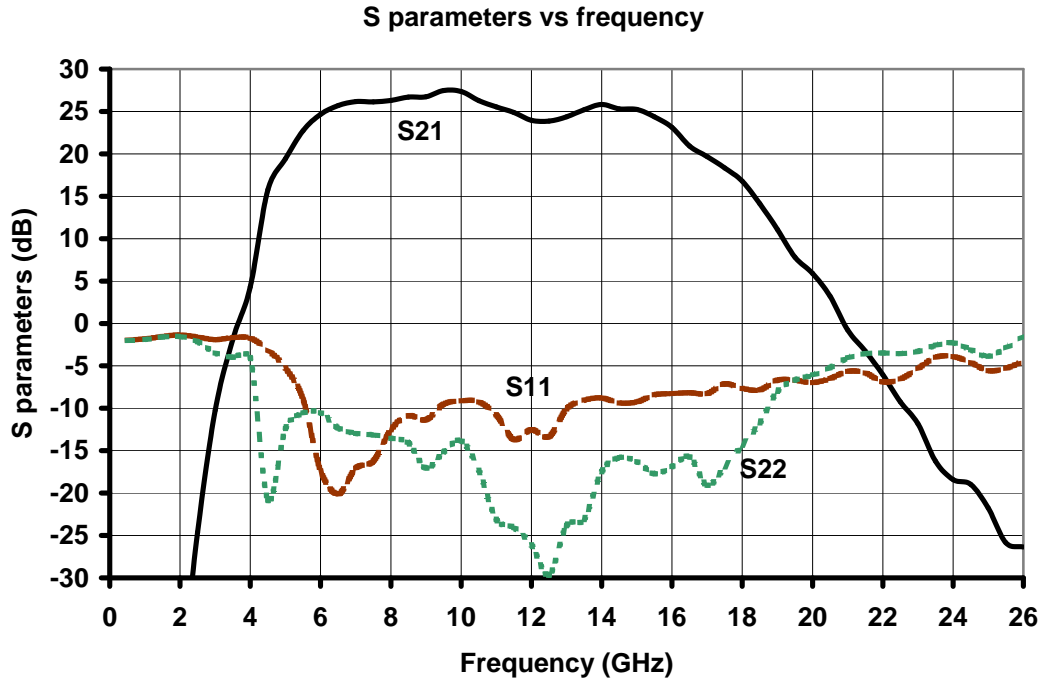
Typical Measured Performance

On board measurement

Tamb.=+25°C, Vd=+4.5V Id=310 mA

Measurement in the connector access planes, using the proposed land pattern & board 96270B

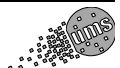
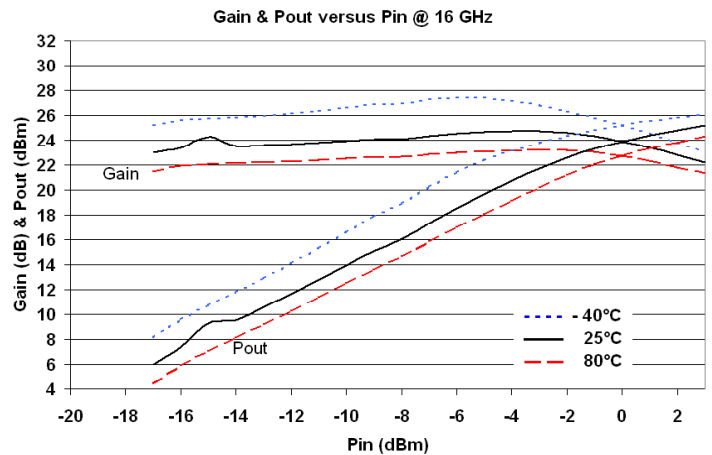
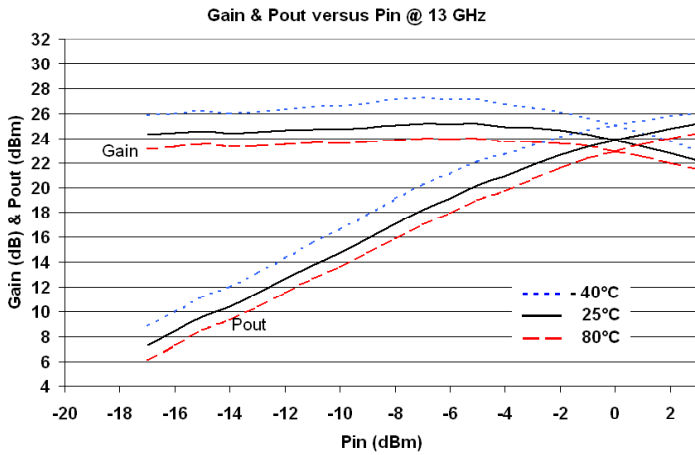
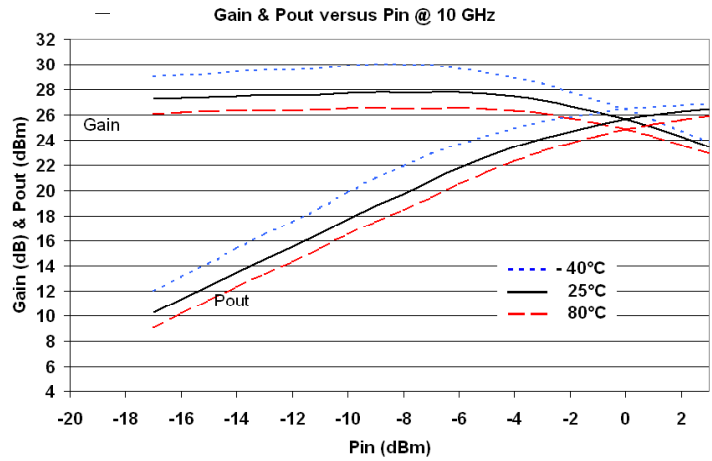
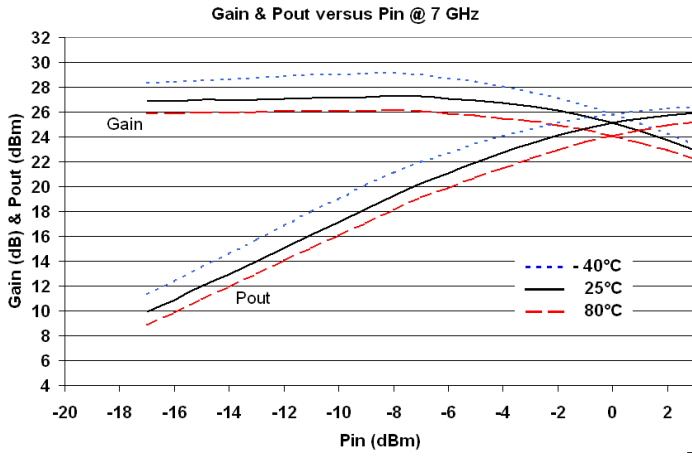
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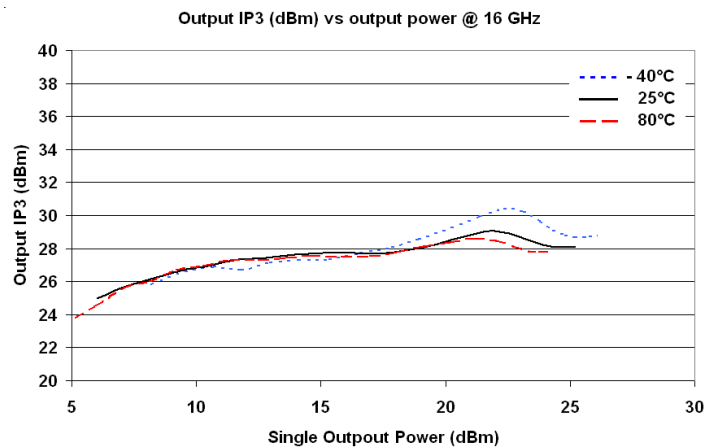
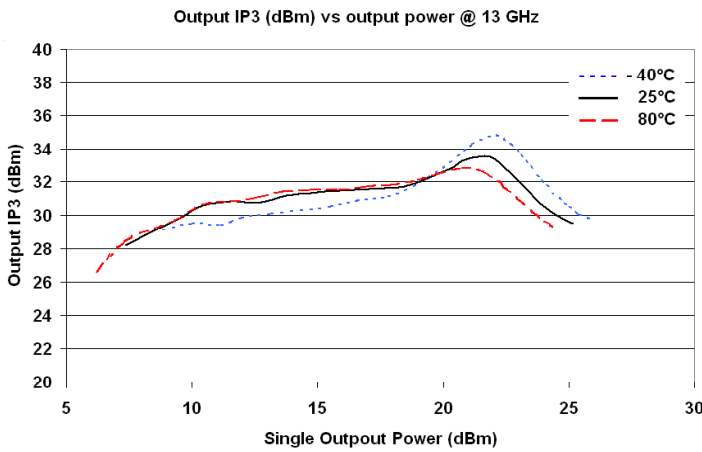
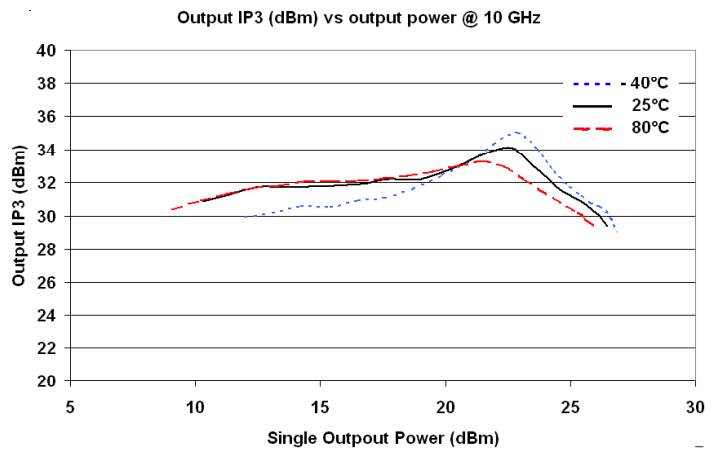
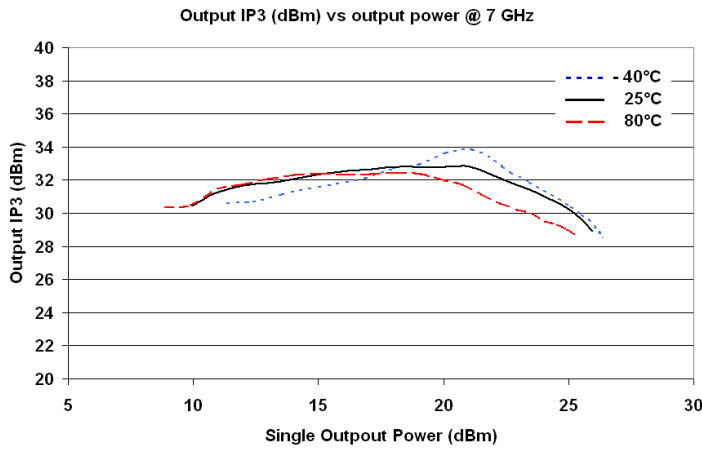
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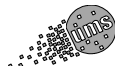
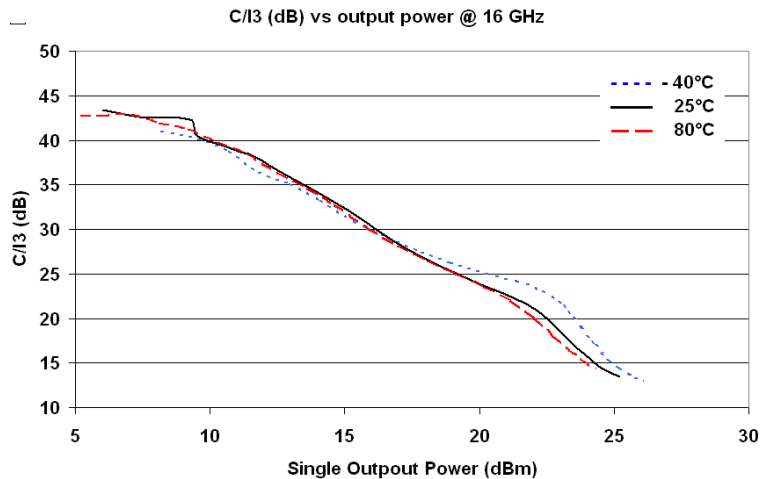
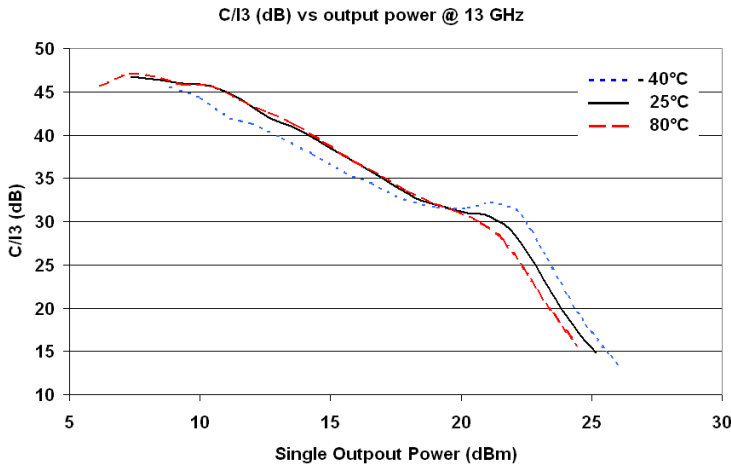
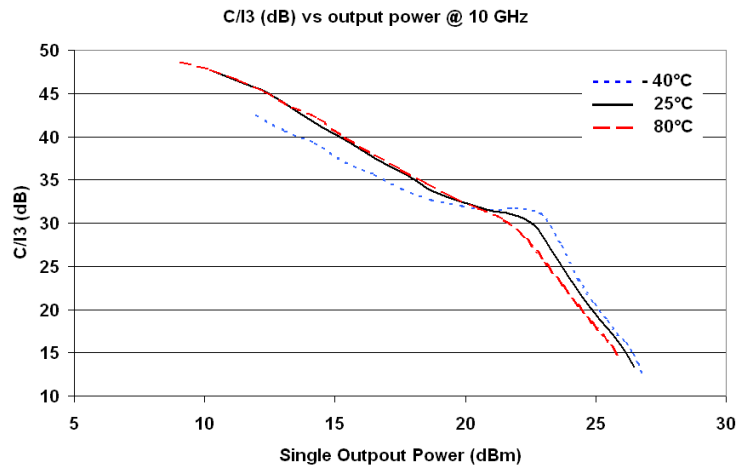
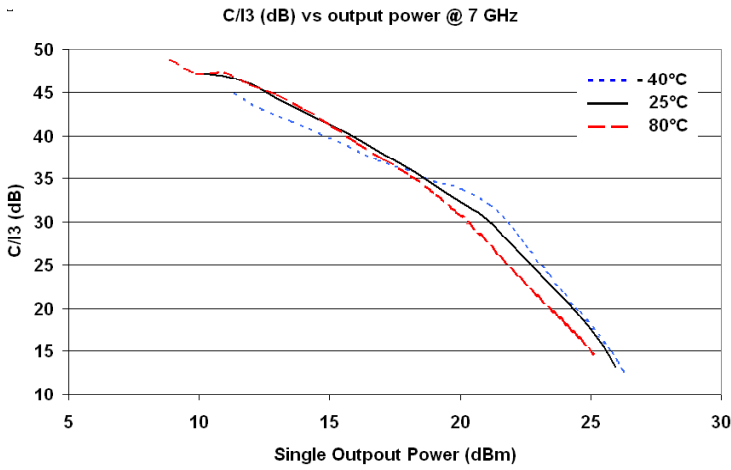
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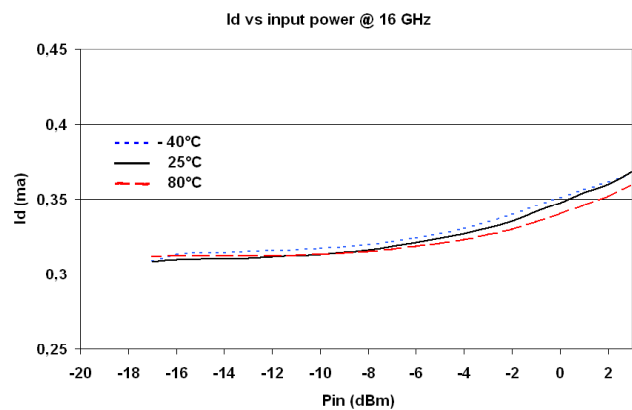
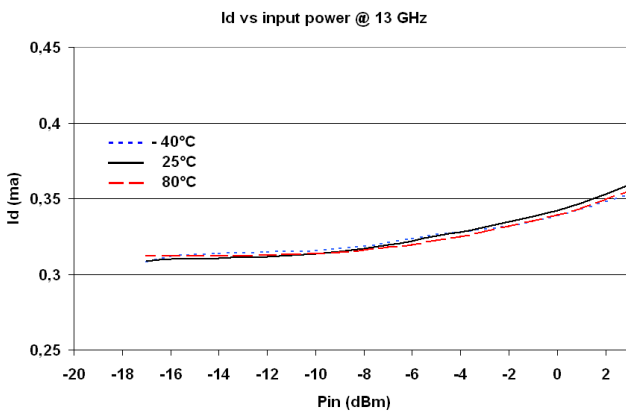
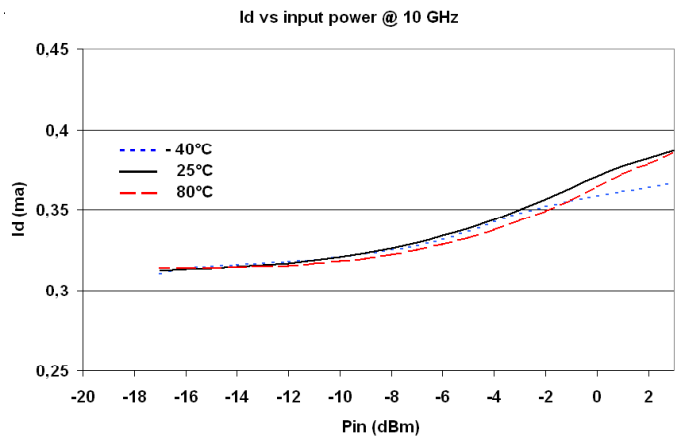
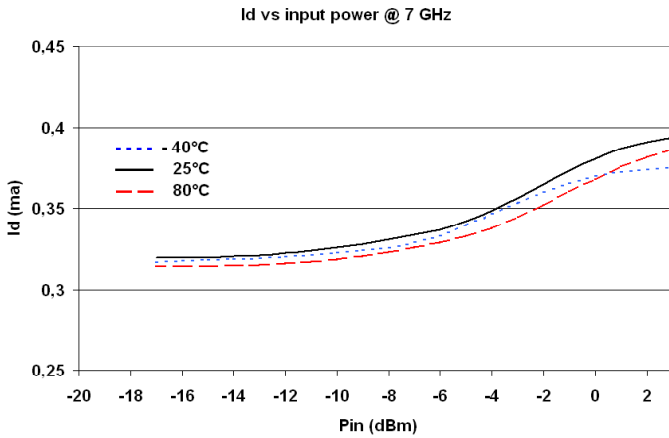
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Typical Package Sij parameters

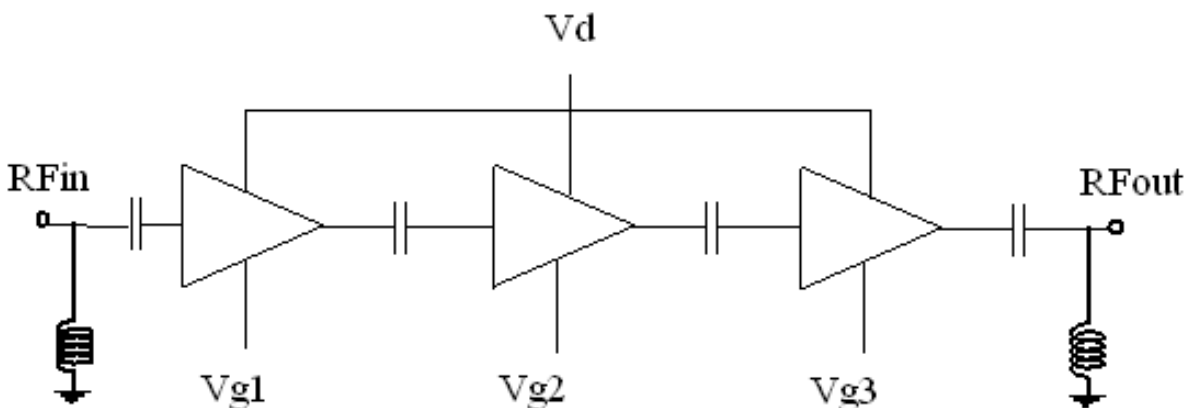
Tamb.=+25°C, Vd1=+4.5V, Id=310mA

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Freq (GHz)	dB(S11)	P(S11) (°)	dB(S21)	P(S21) (°)	dB(S12)	P(S12) (°)	dB(S22)	P(S22) (°)
1	-1,4	107	-62,2	-100	-59,8	-110	-1,4	105
2	-1,1	42	-42,5	-80	-67,8	142	-1,3	35
3	-1	-14	-9,4	-178	-63,5	116	-2,5	-34
4	-1,2	-69,9	4,9	59	-58,5	11	-3,4	-91
5	-3,9	-135	19,9	-64	-65,2	115	-10,1	-98
6	-18,5	-170	25	170	-72,7	75	-9,8	-133
7	-12,9	-112	26,1	65	-70,5	2	-10,5	-160
8	-10,1	-139	26,5	-22	-72,8	38	-11,6	173
9	-8,5	-169	26,5	-100	-65,6	71	-11,8	149
10	-8,4	150	26,5	-179	-62,5	47	-13	110
11	-9,8	110	25,7	108	-60,3	-66	-16,8	68
12	-11,5	69	25,1	42	-66	-145	-21,7	-7
13	-12,8	19	24,9	-22	-62,4	-159	-19,7	-95
14	-12,3	-24	24,8	-88	-54,4	-168	-15,8	-139
15	-8,8	-65	24,9	-162	-53,2	125	-13,6	-168
16	-5,9	-110	23,6	115	-50,7	100	-12,4	169
17	-4,8	-154	20,2	37	-53,1	31	-10,7	153
18	-4,7	170	16	-32	-53,7	73	-8,6	134
19	-4,9	139	11,8	-97	-54	47	-6,3	110
20	-5	109	7,5	-160	-53,4	56	-4,3	82
21	-4,8	78	2,7	137	-53	50	-2,7	52
22	-4,4	46	-2,3	79	-48,8	67	-1,6	23
23	-3,7	14	-7,9	23	-44	52	-0,9	-5
24	-3,2	-17	-13,9	-26	-40,4	3	-0,7	-31
25	-2,7	-46	-20,3	-73	-43,7	-46	-0,8	-54
26	-2,3	-73	-27,3	-112	-52	-7	-0,8	-75

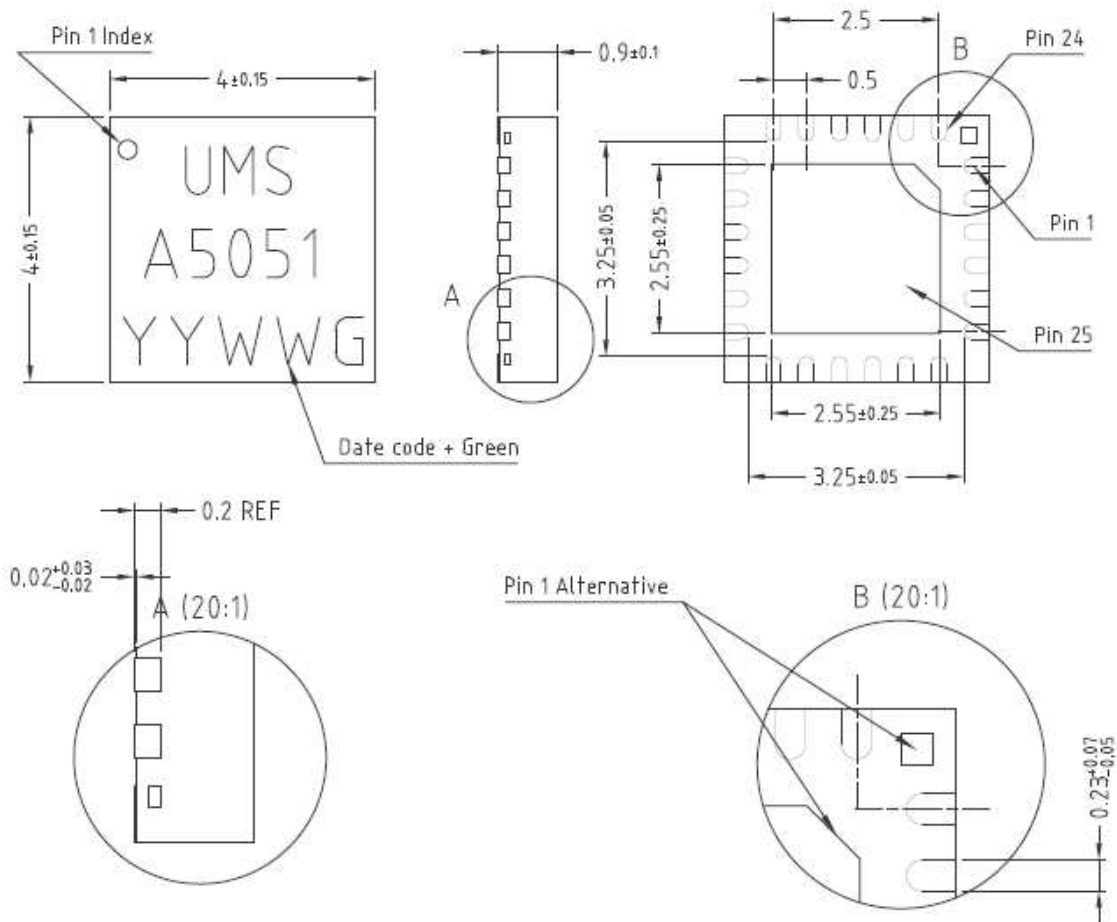
Note

Due to ESD protection circuits on RF input and output, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



Package outline:

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Units : mm

From the standard : JEDEC MO-220 [VGGD-6 / VGGD-8]

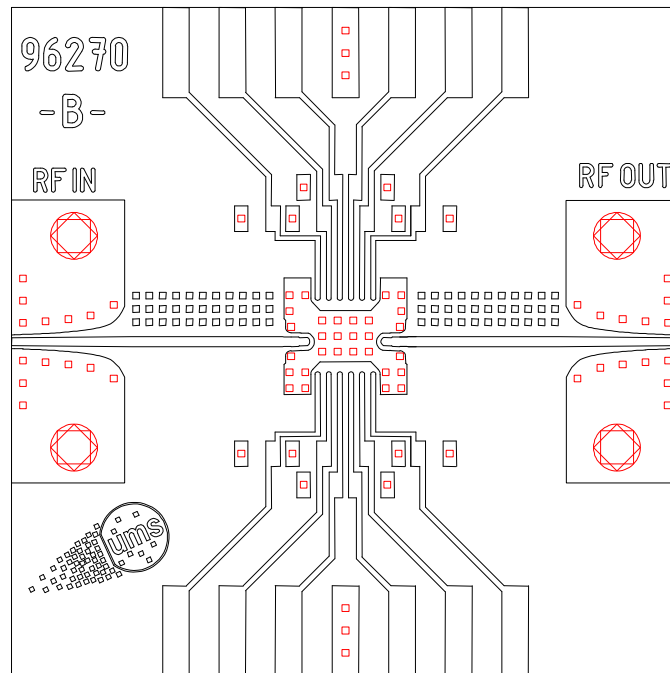
Matt tin, Lead free (Green)

1- NC	9- Vg2	17- GND	25- GND Exposed Pad
2- GND	10- Vg3	18- NC	
3- GND	11- NC	19- NC	
4- RF IN	12- NC	20- Vd	
5- GND	13- GND	21- NC	
6- GND	14- GND	22- NC	
7- NC	15- RF OUT	23- NC	
8- Vg1	16- GND	24- NC	

Proposed assembly board "96270B" for the 24L-QFN4x4 products characterization.

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- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



The SMD leadless package has been designed for high volume surface mount PCB assembly process. A typical footprint is proposed for the PCB (motherboard) in the previous drawing. For the mounting process standard techniques involving solder paste and a suitable reflow process can be used.

Assembly process

Please refer to application note AN0017

Ordering Information

QFN 4x4 RoHS compliant package: CHA5051-QDG/XY
Stick: XY=20 Tape & reel: XY=21

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