

17-27GHz High Power Amplifier

Preliminary

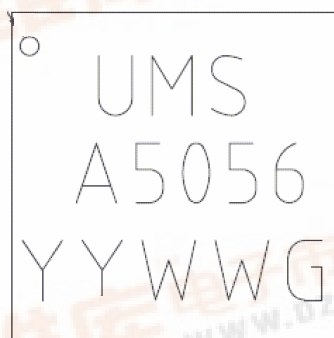
GaAs Monolithic Microwave IC in SMD leadless package

Description

The CHA5056-QGG is a three-stage monolithic high power amplifier.

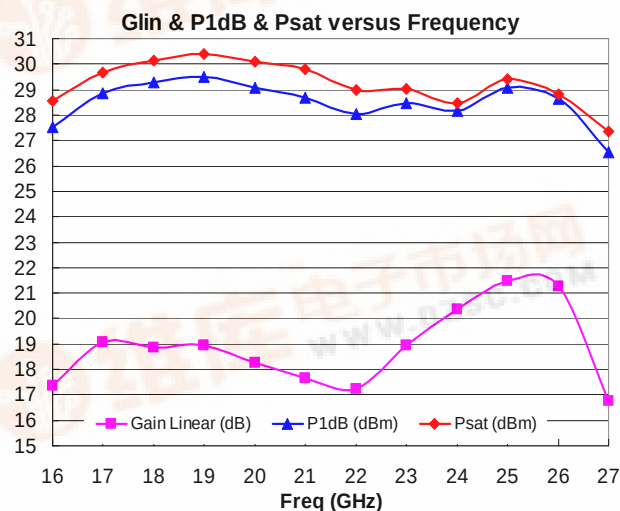
The circuit is manufactured with a power P-HEMT process, 0.15μm gate length, via holes through the substrate.

It is supplied in RoHS compliant SMD package



Main Features

- Broadband performance 17-27GHz
- 28.5dBm Output Power @1dB compression
- 38dBm 3rd order intercept point
- High gain: 19dB
- ESD protected (see page 6)
- DC power consumption, 890mA @ 4.5V
- 28LQFN5x5



Typical on board measurements

Main Characteristics

Tamb = +25°C, Vd1=Vd2=Vd3= +4.5V, Id (Quiescent)=890mA

Symbol	Parameter	Min	Typ	Max	Unit
F_op	Operating Frequency Range	17		27	GHz
P_1dB	Output power at 1dB compression		28.5		dBm
G_lin	Linear Gain		19		dB

ESD Protections: Electrostatic discharge sensitive device observe handling precautions !



Electrical Characteristics

Tamb = +25°C, CW biasing mode

These values are representative of onboard measurements as defined on the drawing 96402.

Preliminary

Symbol	Parameter	Min	Typ	Max	Unit
Fop	Operating frequency range	17		27	GHz
G_lin	Linear Gain from 17 to 24GHz		18		dB
	from 24.5 to 26.5GHz		20		dB
P1dB	Output power at 1dB gain compression		28.5		dBm
Psat	Saturated Output power		29.5		dBm
OIP3	Output 3 rd Order Intercept Point @ Id=890mA		37		dBm
	Output 3 rd Order Intercept Point @ Id=700mA		38		dBm
IS11I	Input return loss		2.0:1		dB
IS22I	Output return loss		2.2:1		dB
Id	Quiescent Drain current (1)		890		mA
Id_1dBc	Drain current @1dB gain compression		1		A
Vd 1,2,3	Positive drain bias voltage		4.5		V
Vg	Negative gate bias voltage		-2.2		V

(1) This parameter is fixed by gate voltage Vg

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	5	V
Id	Drain bias current with Vd=4.5V Small Signal	1100	mA
Vg	Gate bias voltage	-4 to +0.8	V
Pin	RF input power	15	dBm
Tj	Junction temperature (2)	175	°C
Top	Operating temperature range	-40 to +80	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Thermal Resistance channel to ground paddle =20.5°C/W for Tground paddle. = +80°C with 4.5V, 890mA

Typical Package Sij parameters

Preliminary

Tamb = +25°C, Vd1=Vd2=Vd3= +4.5V, Id = 890mA

Freq (GHz)	dB (S11)	P (S11) (°)	dB (S21)	P (S21) (°)	dB (S12)	P (S12) (°)	dB (S22)	P (S22) (°)
1,0	-0,6	155	-46,8	-20	-90,8	66	-0,4	154
2,0	-0,5	130	-51,8	-85	-70,3	-66	-0,6	129
3,0	-0,6	106	-55,9	-136	-67,7	-35	-0,7	102
4,0	-0,7	81	-52,6	71	-67,4	-6	-0,7	74
5,0	-0,8	55	-51,5	9	-79,3	-9	-0,9	45
6,0	-1,0	30	-49,3	-81	-71,3	-166	-1,0	14
7,0	-1,2	3	-50,5	52	-70,7	-148	-1,1	-21
8,0	-1,4	-24	-29,8	-33	-61,6	32	-1,3	-62
9,0	-1,7	-50	-18,3	-131	-61,3	-60	-1,8	-112
10,0	-1,8	-77	-11,5	134	-55,1	-158	-3,0	-175
11,0	-2,0	-107	-6,3	46	-57,0	158	-5,4	111
12,0	-2,2	-136	-1,9	-36	-60,8	124	-8,9	31
13,0	-2,6	-166	2,3	-113	-56,3	129	-11,9	-43
14,0	-3,5	162	7,2	172	-48,8	86	-13,6	-96
15,0	-5,4	128	12,7	86	-49,0	31	-17,3	-118
16,0	-9,1	92	16,9	-12	-50,5	0	-14,3	-108
17,0	-14,5	50	18,6	-114	-51,8	-37	-11,0	-140
18,0	-19,7	-41	18,5	150	-61,6	45	-10,2	-167
19,0	-15,2	-114	17,9	62	-54,6	7	-10,2	165
20,0	-11,8	-147	17,3	-20	-53,3	-24	-11,5	141
21,0	-9,4	180	17,0	-100	-59,8	-51	-13,7	114
22,0	-9,1	149	17,4	180	-56,6	-1	-18,6	83
23,0	-9,7	111	18,3	95	-62,3	112	-29,9	14
24,0	-12,1	62	19,6	0	-51,6	31	-24,4	-131
25,0	-19,3	-15	20,9	-110	-46,2	9	-17,4	-154
26,0	-20,4	178	19,5	121	-46,9	-7	-14,4	179
27,0	-13,6	77	15,1	-13	-42,3	-18	-13,1	130
28,0	-8,3	0	5,6	-168	-40,8	-38	-11,9	14
29,0	-5,9	-55	-11,8	70	-38,1	-47	-8,4	-79
30,0	-4,1	-97	-27,1	-46	-33,5	-74	-5,7	-127
31,0	-3,1	-132	-29,8	-123	-31,4	-122	-4,1	-162
32,0	-2,3	-160	-31,5	-171	-33,1	-171	-3,5	173
33,0	-1,9	175	-36,1	148	-37,5	162	-3,1	148
34,0	-1,6	152	-42,3	143	-40,3	153	-3,4	126
35,0	-1,4	134	-49,3	165	-41,2	153	-6,2	96
36,0	-1,2	118	-44,1	151	-40,5	136	-9,1	159
37,0	-1,1	103	-43,8	129	-44,1	85	-2,4	134
38,0	-1,0	90	-43,7	102	-48,9	87	-0,8	112
39,0	-1,0	75	-43,9	24	-53,0	114	-0,6	96
40,0	-1,5	60	-46,6	-161	-50,1	112	-0,1	82

Refer to the “definition of the Sij reference planes” section below

Preliminary

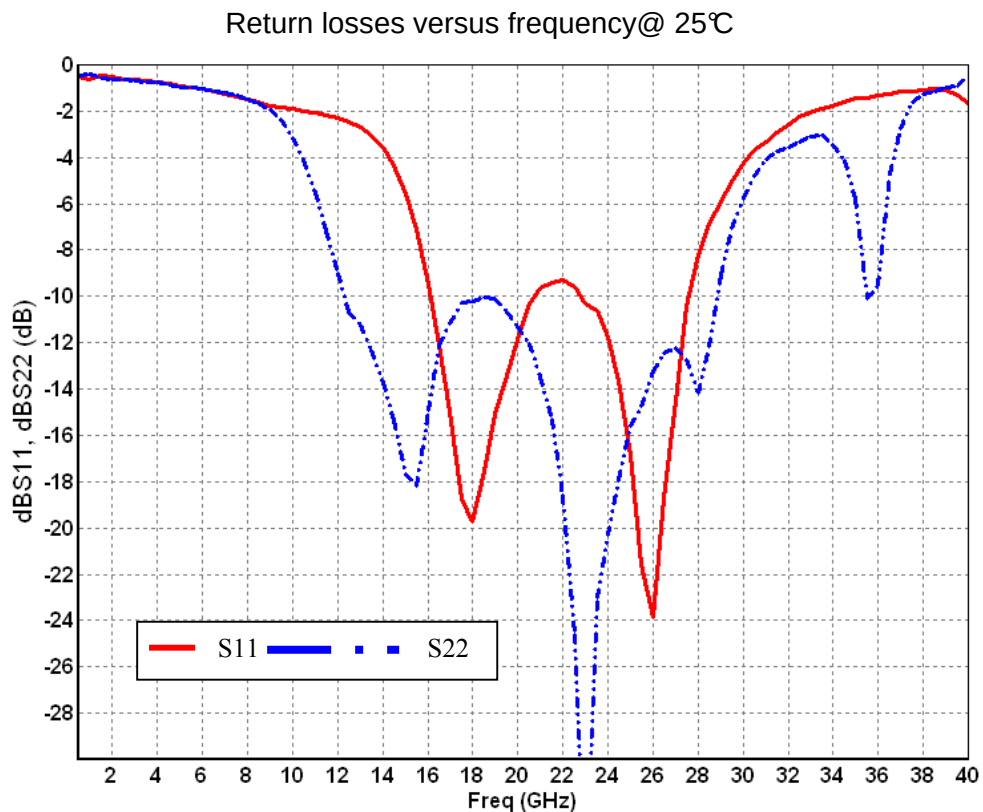
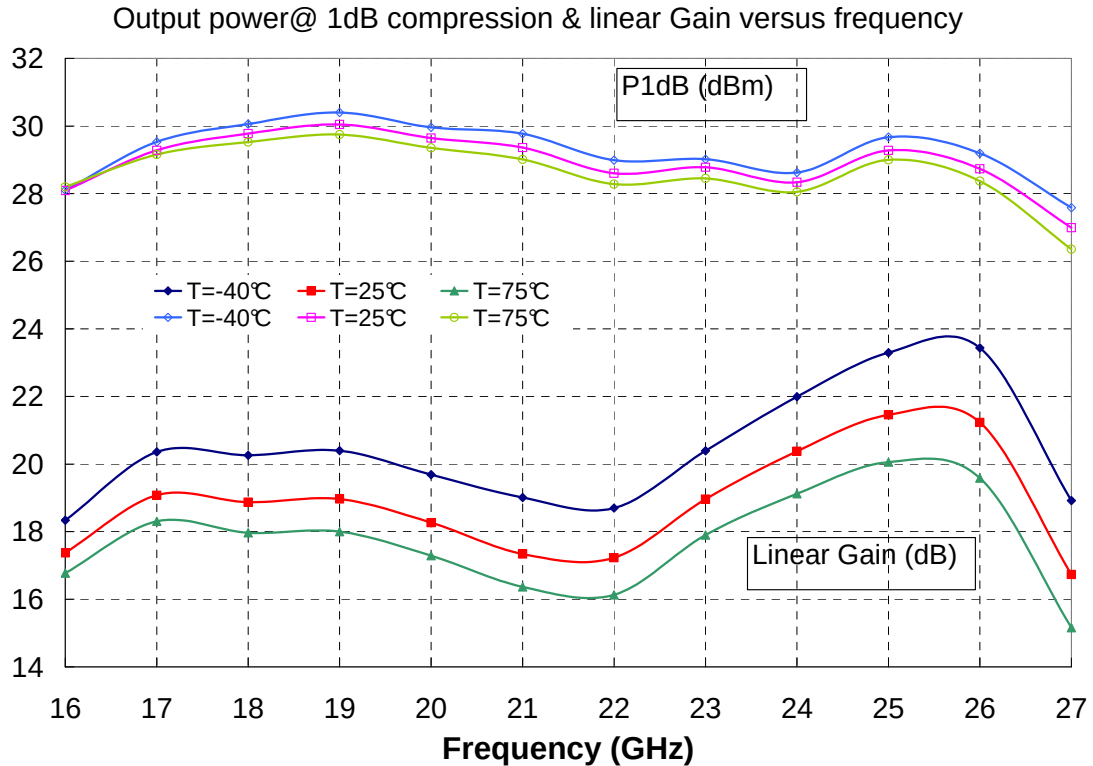
Tamb = +25°C, Vd1=Vd2=Vd3= +4.5V, Id = 700mA

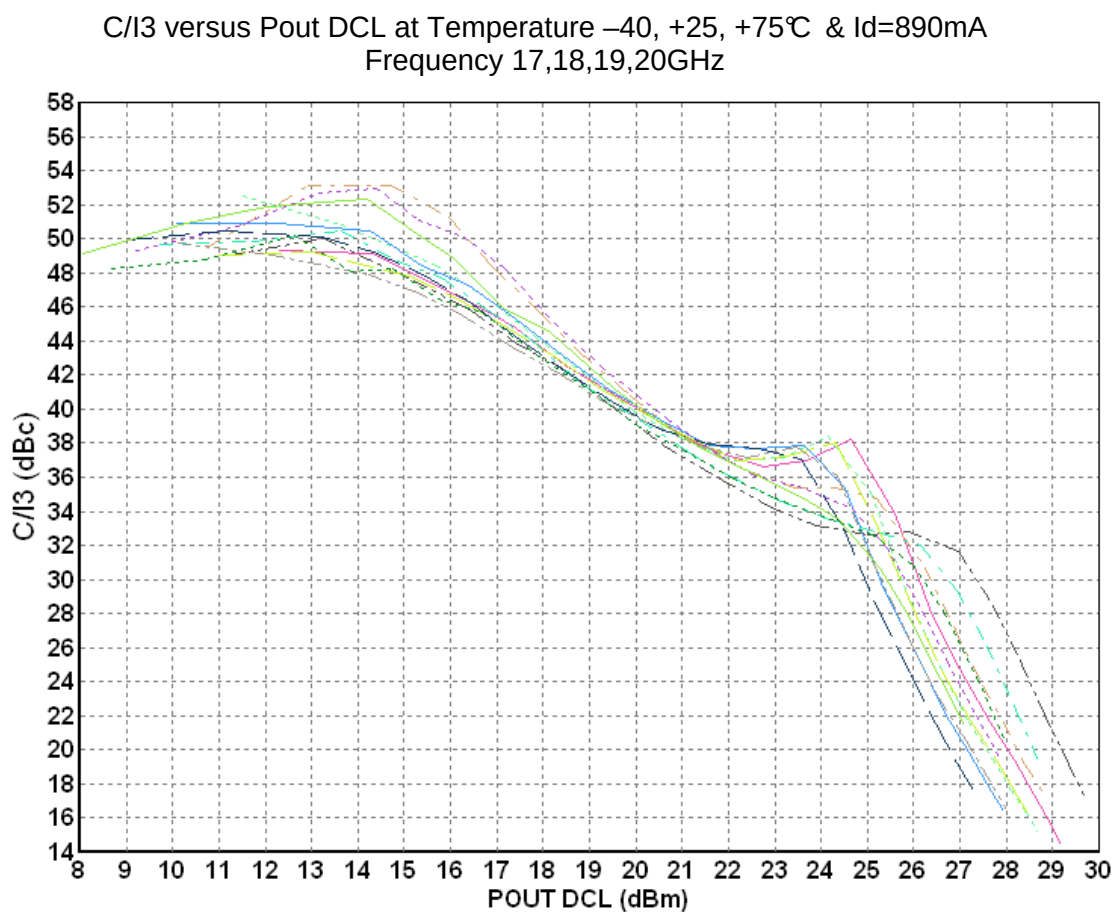
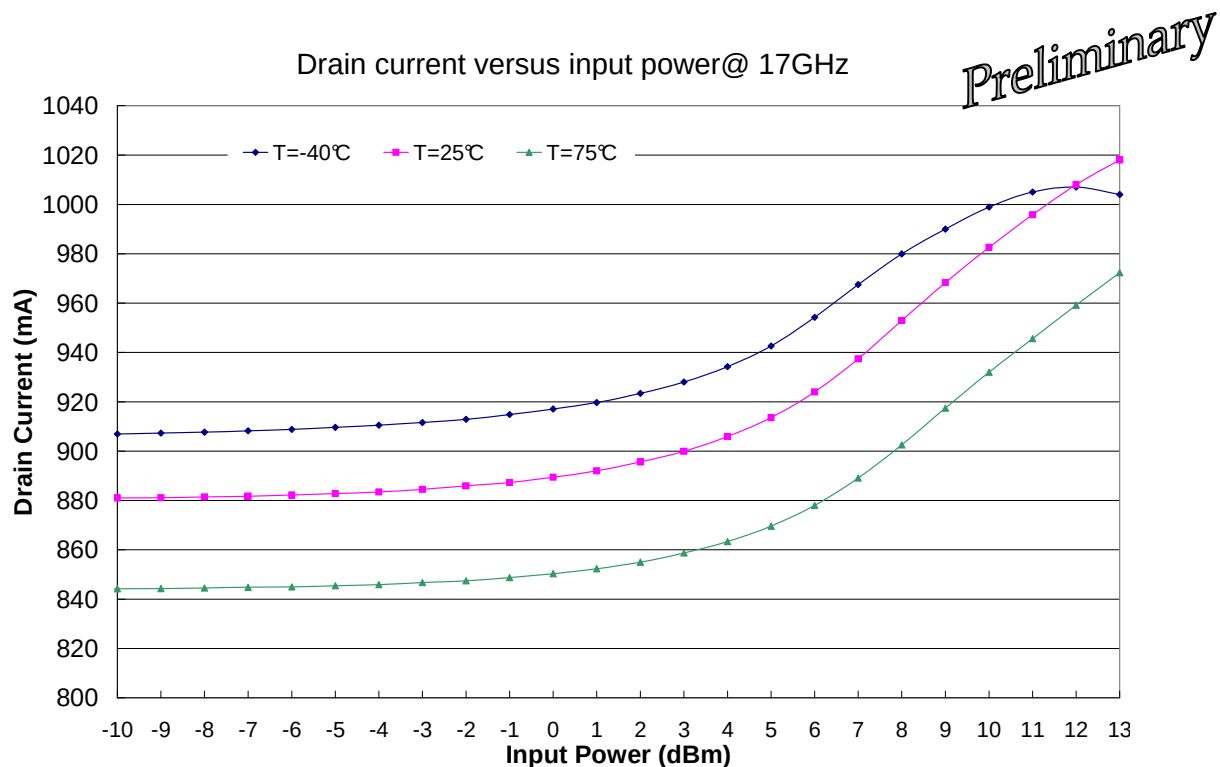
Freq (GHz)	dB (S11)	P (S11) (°)	dB (S21)	P (S21) (°)	dB (S12)	P (S12) (°)	dB (S22)	P (S22) (°)
1	-0,6	155	-48,5	-19	-83,8	-103	-0,4	154
2	-0,5	130	-50,6	-85	-69,9	-77	-0,6	129
3	-0,6	106	-59,4	-155	-66,8	-28	-0,7	102
4	-0,7	81	-54,7	106	-66,3	4	-0,7	75
5	-0,8	55	-51,0	4	-75,4	-2	-0,9	45
6	-1,0	30	-50,9	-87	-71,1	-176	-1,0	14
7	-1,1	4	-53,6	26	-69,8	-144	-1,1	-21
8	-1,4	-23	-30,2	-34	-61,0	36	-1,3	-62
9	-1,6	-50	-18,8	-132	-60,1	-66	-1,8	-111
10	-1,8	-77	-11,9	132	-55,3	-156	-3,0	-174
11	-2,0	-107	-6,8	45	-56,7	162	-5,3	113
12	-2,2	-136	-2,4	-37	-61,9	123	-8,7	34
13	-2,5	-166	1,7	-115	-57,4	133	-11,8	-38
14	-3,4	162	6,4	170	-49,0	84	-13,3	-90
15	-5,3	128	11,7	85	-49,5	35	-16,0	-114
16	-8,9	92	15,9	-12	-50,3	2	-13,5	-110
17	-14,3	48	17,7	-114	-51,7	-36	-10,4	-141
18	-19,4	-41	17,6	151	-63,7	37	-9,7	-171
19	-15,1	-114	17,0	63	-55,0	6	-10,1	161
20	-11,8	-147	16,4	-19	-53,1	-22	-11,8	136
21	-9,5	-179	16,1	-99	-59,2	-55	-14,5	108
22	-9,0	151	16,4	-179	-56,7	-7	-20,8	76
23	-9,5	113	17,3	97	-62,7	102	-34,0	-44
24	-11,8	65	18,6	3	-52,0	31	-22,0	-143
25	-18,3	-10	20,0	-107	-45,7	7	-16,9	-160
26	-20,9	-178	18,6	123	-46,5	-8	-13,9	173
27	-13,9	78	14,1	-10	-42,4	-17	-12,6	123
28	-8,4	2	4,5	-162	-40,9	-37	-11,0	12
29	-5,9	-54	-12,8	77	-38,1	-47	-7,9	-78
30	-4,1	-96	-28,0	-43	-33,5	-75	-5,4	-127
31	-3,1	-131	-30,5	-122	-31,5	-123	-3,9	-162
32	-2,3	-160	-32,1	-171	-33,2	-172	-3,4	172
33	-1,8	175	-35,3	145	-37,5	162	-3,0	148
34	-1,6	153	-39,2	130	-40,2	155	-3,3	125
35	-1,4	134	-44,2	172	-41,1	153	-6,2	95
36	-1,2	118	-43,7	150	-40,8	138	-9,3	161
37	-1,0	103	-47,4	160	-43,5	90	-2,4	134
38	-1,0	90	-40,6	83	-49,6	84	-0,8	112
39	-1,0	75	-52,6	28	-51,7	97	-0,6	97
40	-1,5	60	-43,9	-133	-51,7	115	-0,1	82

Refer to the “definition of the Sij reference planes” section below

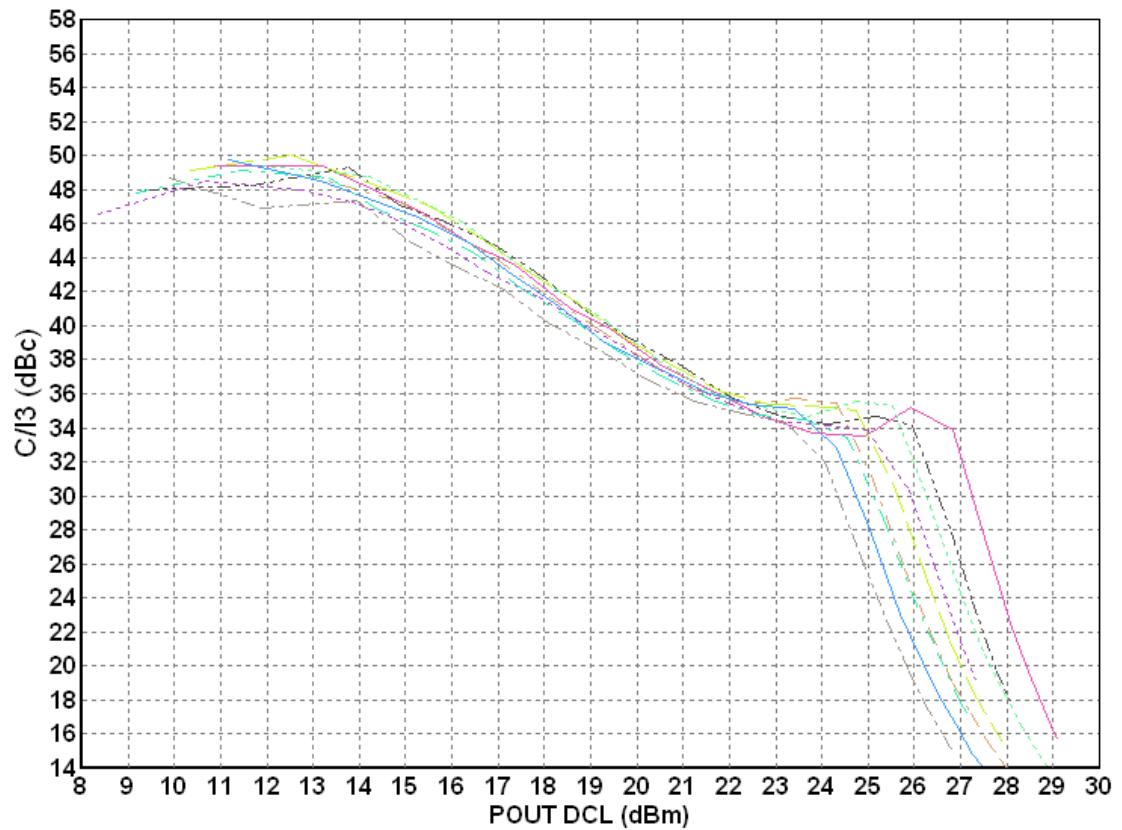
*Preliminary***Typical Measured Performance**T_{amb} = +25°C, V_{d1}=V_{d2}=V_{d3} = +4.5V, I_d =890mA, CW bias sing mode

Measurements in the package access planes, using the proposed land pattern & board 96402

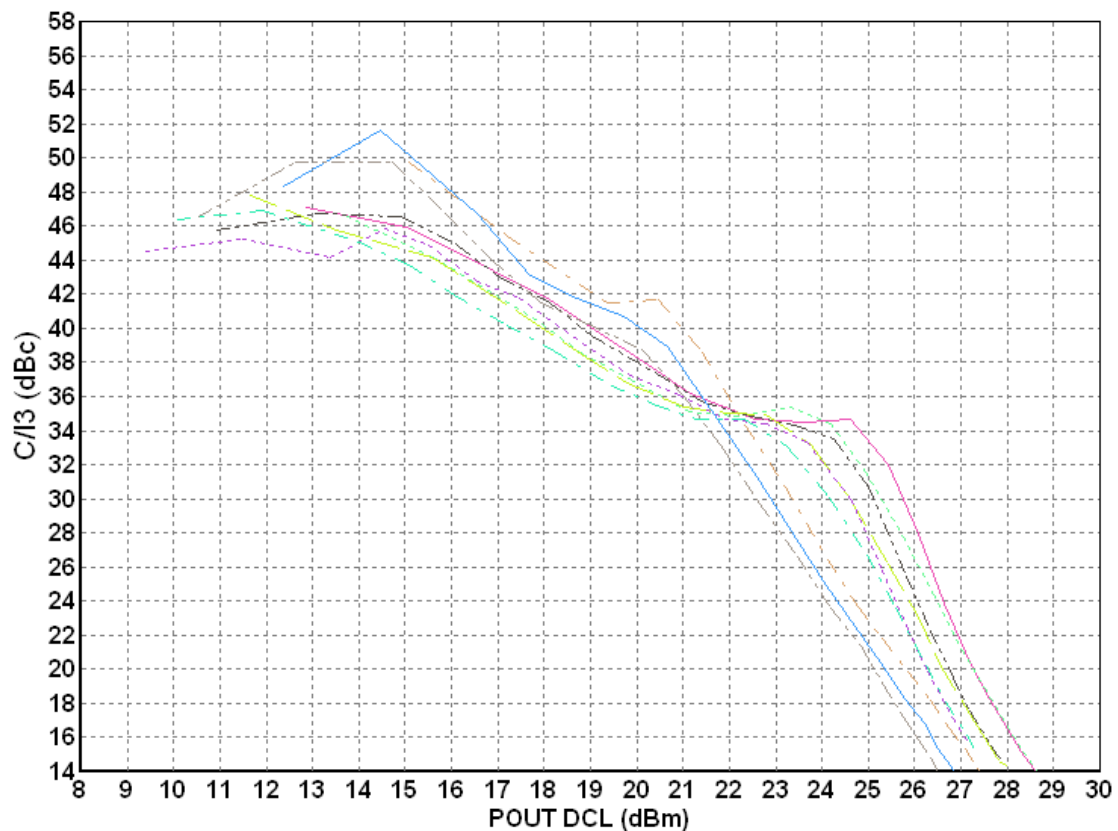




Frequency 21,22,23 GHz



Frequency 24, 25, 26 GHz

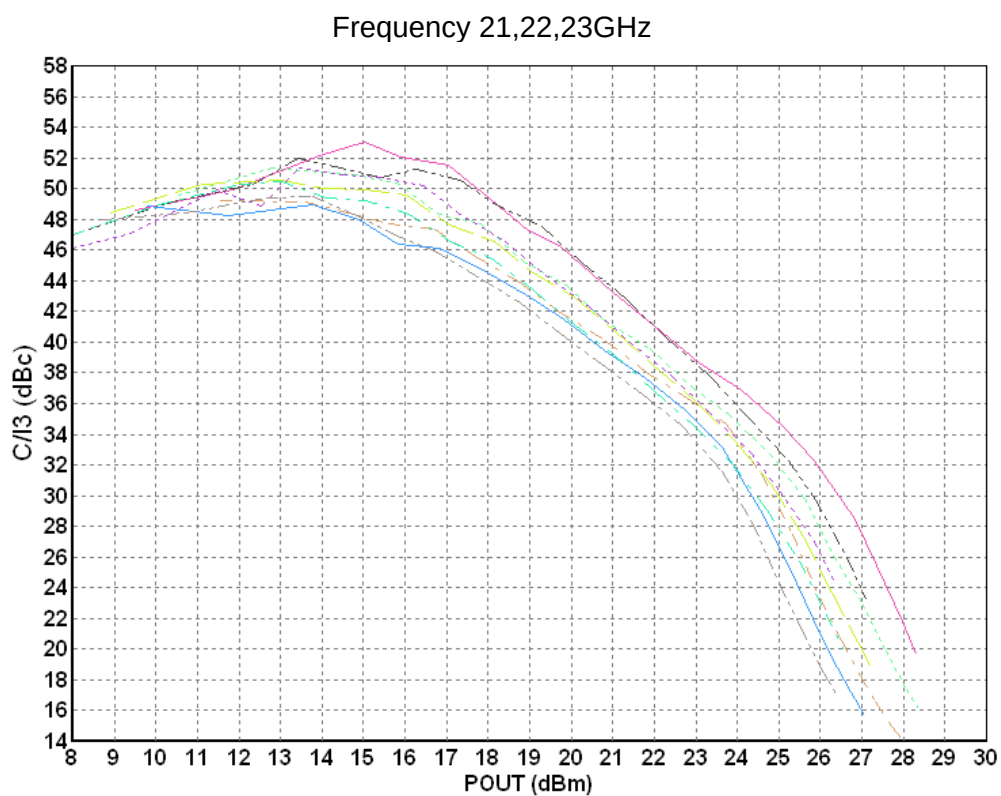
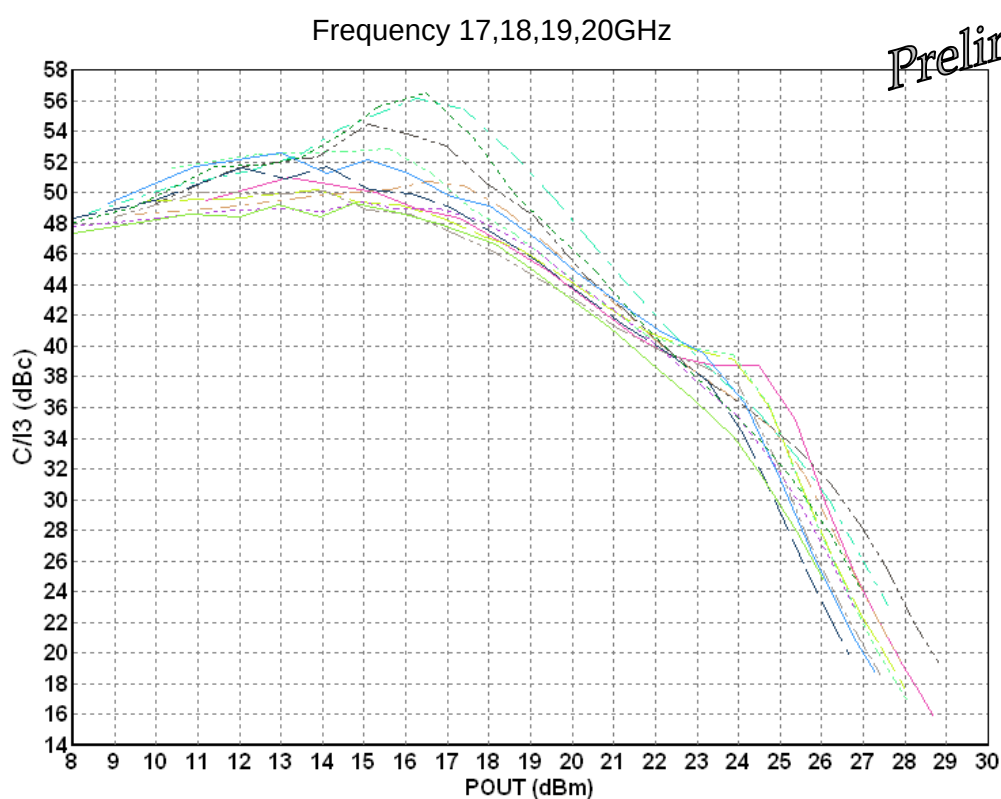


C/I3 versus Pout DCL at Temperature -40, +25, +75°C & Id=700mA

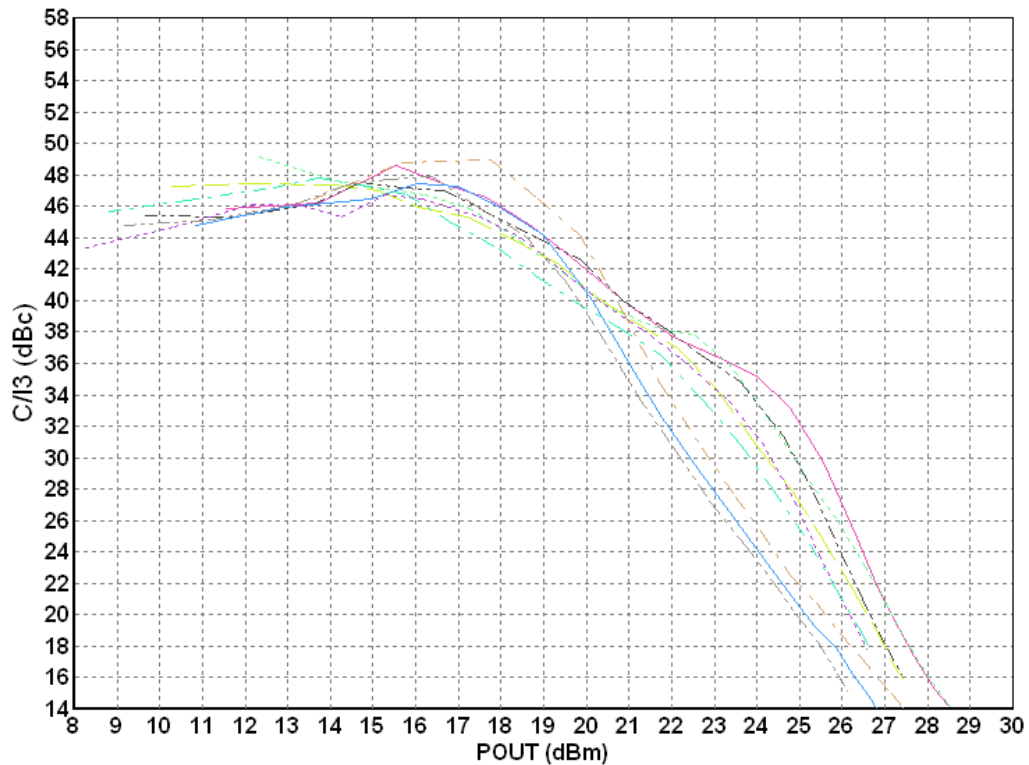
Ref.: DSCHA5056QGG7033 - 02 Feb 07

7/12

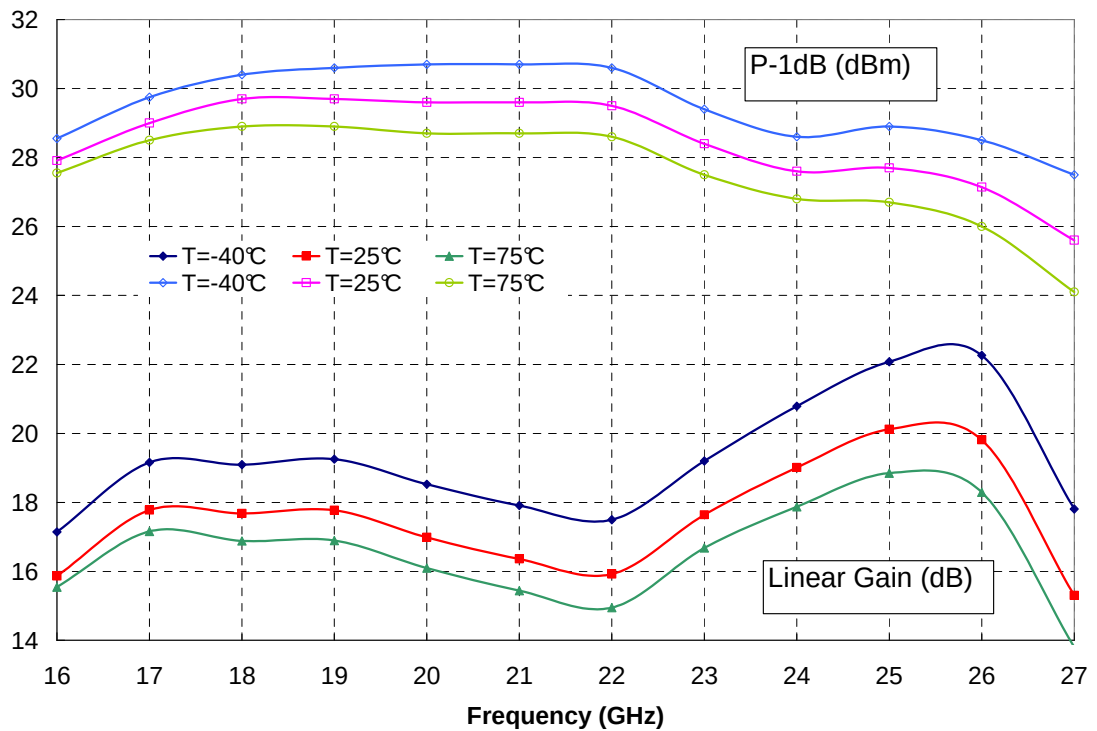
Specifications subject to change without notice



Frequency 24, 25, 26GHz



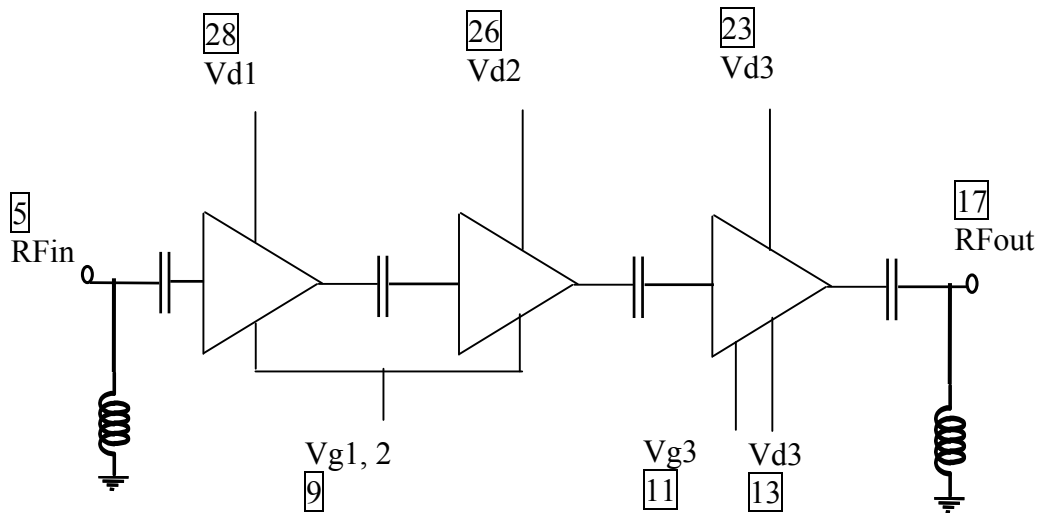
Output power@ 1dB compression & linear Gain versus frequency at 700mA



Note

Preliminary

Due to ESD protection, RFin and RFout are DC grounded, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF accesses.



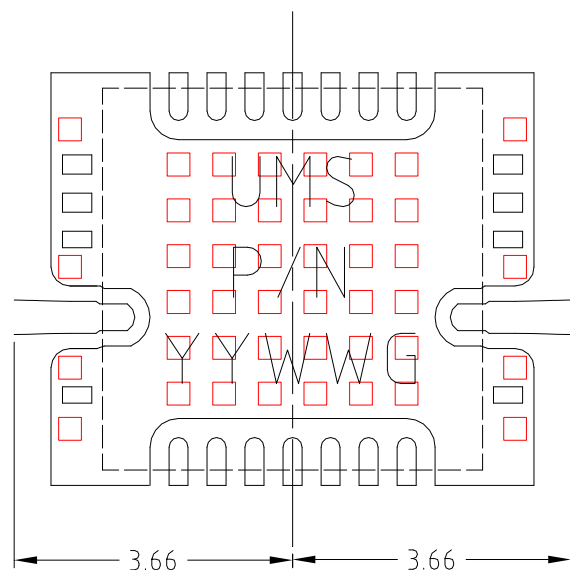
ESD protections are also implemented on gate accesses.

The DC connections does not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

Definition of the Sij reference planes

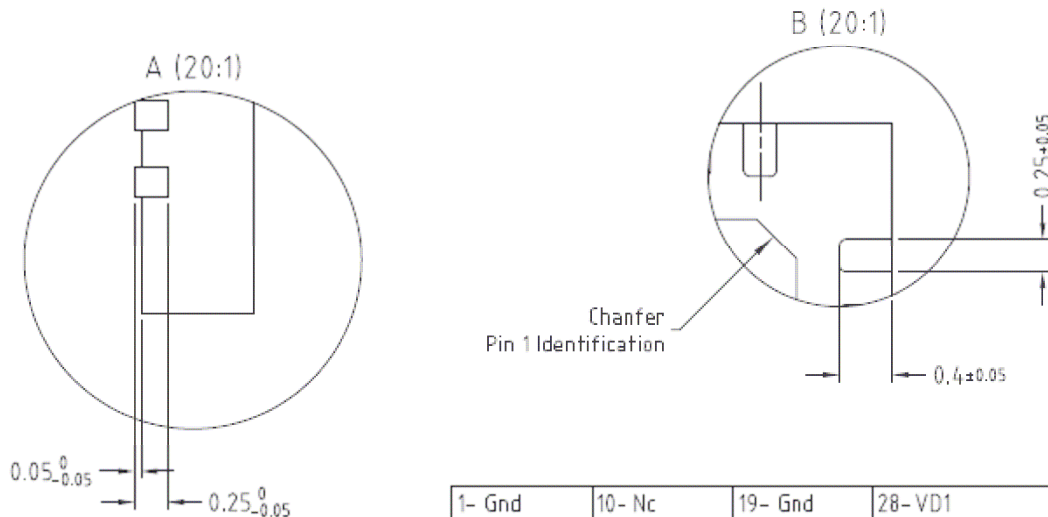
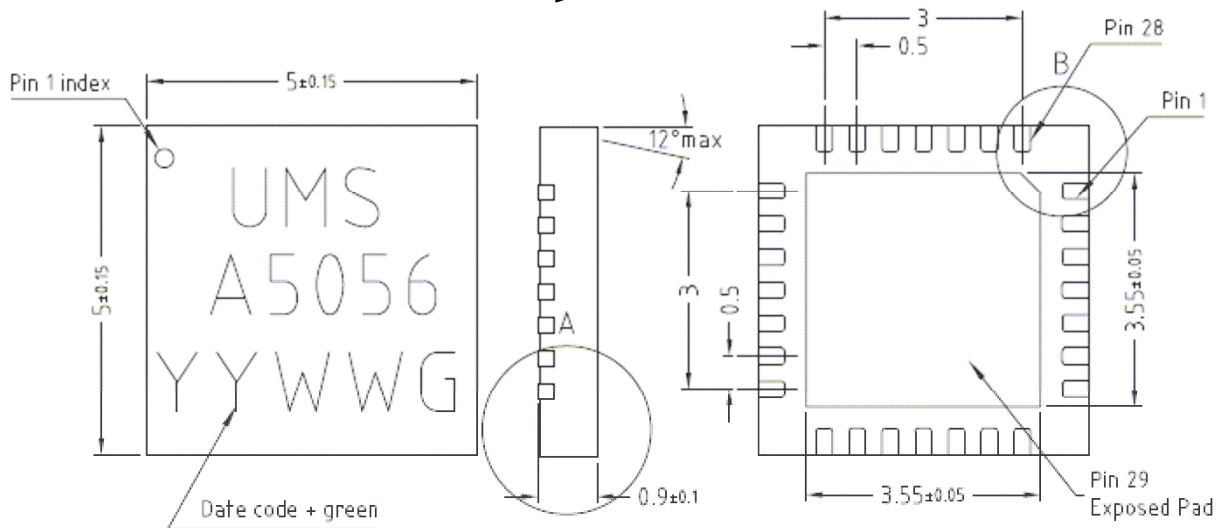
The reference planes are defined from the footprint of the recommended characterization board shown below under the number 96402.

The reference is the symmetrical axis of the package. The input and output reference planes are located at 3.66mm offset (input wise and output wise respec.) from this axis. Then, the given Sij incorporates this land pattern.



Package outline

Preliminary



Matt tin, Lead free (Green)

Units : mm

From the standard : JEDEC MO-220 [VEED-6]

1- Gnd	10- Nc	19- Gnd	28- VD1
2- Nc	11- VG3	20- Nc	29- GND Exposed Pad
3- Gnd	12- Nc	21- Gnd	
4- Gnd	13- VD3	22- Nc	
5- RF IN	14- Nc	23- VD3	
6- Gnd	15- Gnd	24- Nc	
7- Gnd	16- Gnd	25- Nc	
8- Nc	17- RF OUT	26- VD2	
9- VG1-VG2	18- Gnd	27- Nc	

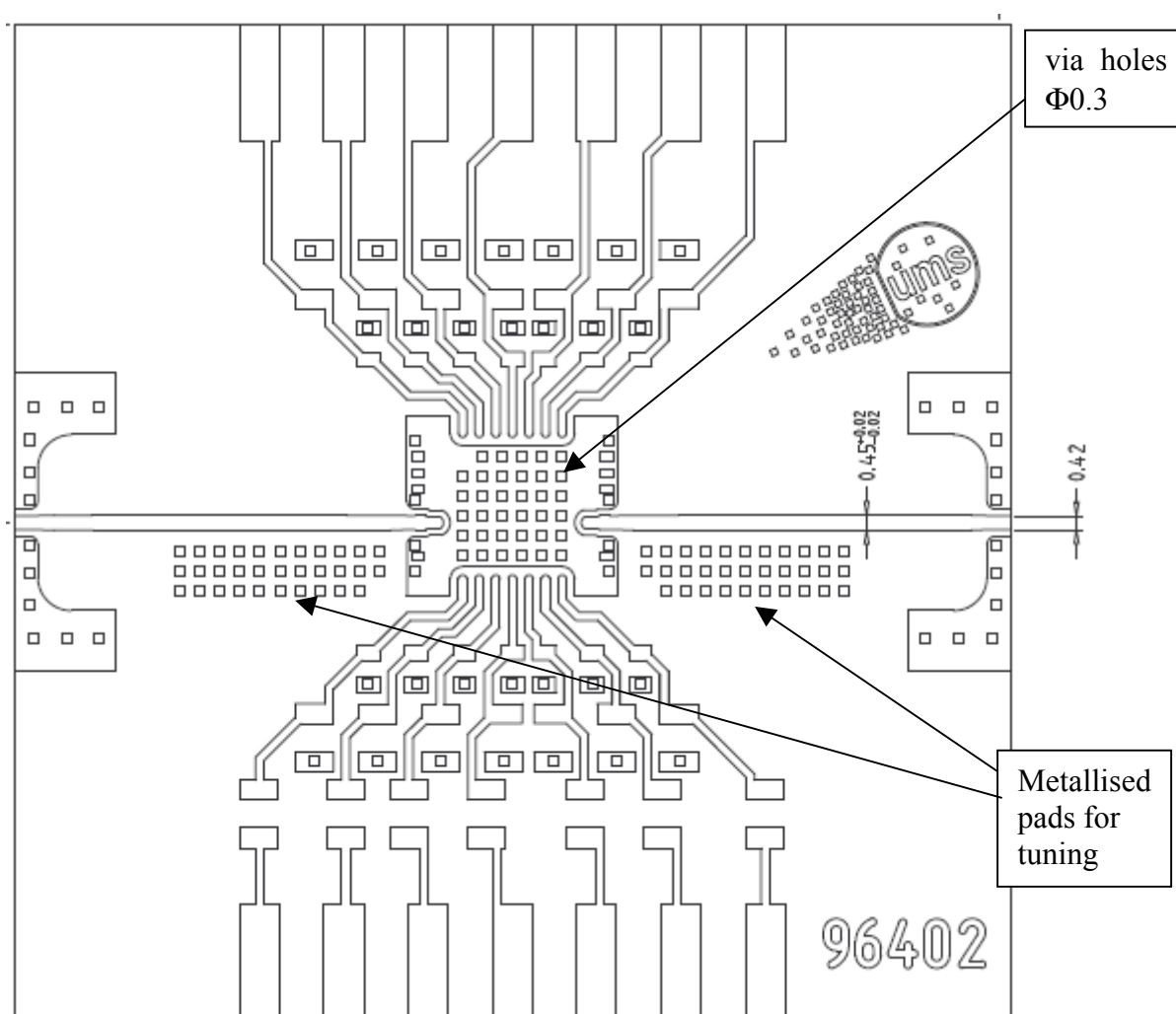
SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

Proposed Assembly board "96402" for the 28L-QFN5x5 products characterization.

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



Ordering Information

QFN 5x5 RoHS compliant package: CHA5056-QGG/XY
Stick: XY = 20 Tape & reel: XY = 21

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