

## 12-27GHz Bidirectionnal Detector

*Preliminary*

### GaAs Monolithic Microwave IC in SMD leadless package

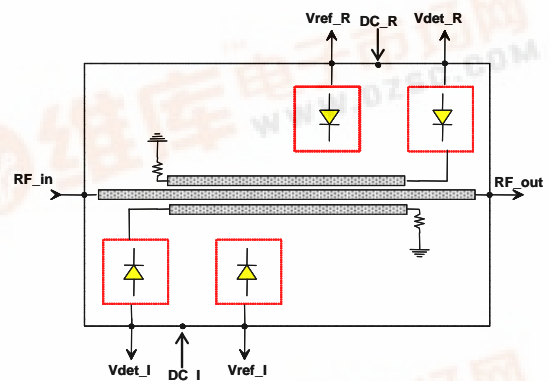
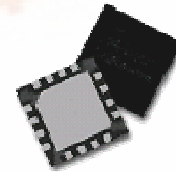
#### Description

The CHE1260-QAG is a bidirectionnal detector that integrates a passive bidirectionnal coupler, two matched detector diodes and two reference diodes.

It allows the measurement of transmitted and reflected power. It is designed for a wide range of applications where an accurate transmitted power control is required, typically commercial communication systems.

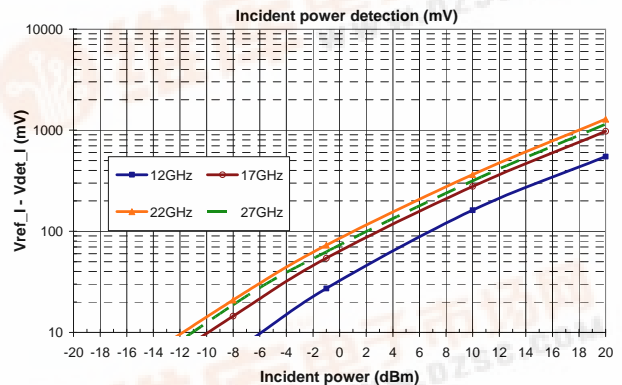
The circuit is manufactured with a Schottky diode MMIC process, 1 $\mu$ m gate length, via holes through the substrate and air bridges.

It is supplied in leadless SMD package.



#### Main Features

- Wide frequency range 12-27GHz
- Bidirectionnal detection
- 30dB dynamic range
- ESD protected
- 16L-QFN3x3 SMD package



#### Main Characteristics

Tamb = +25°C, VDC = +4.5V (on DC\_I and DC\_R)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	12		27	GHz
IL	Insertion Loss		1		dB
Dr	Dynamic Range		30		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!



**Electrical Characteristics**

*Preliminary*

Tamb = +25°C, VDC = +4.5V (on DC\_I and DC\_R)

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	12		27	GHz
IL	Insertion Loss		1		dB
Cd	Coupler Directivity		15		dB
Dr	Dynamic Range		30		dB
Pr	Power Range: 12 - 17GHz 17 - 21GHz 21 - 24GHz 24 - 27GHz  (for transmitted and/or reflected power)	-1 -3 -6 -8			dBm
Vdetect_I	Voltage detection from transmitted power Vref_I – Vdet_I From Pr_min to Pr_max		20 to 2200		mV
Vdetect_R	Voltage detection from reflected power Vref_R – Vdet_R From Pr_min to Pr_max		20 to 2200		mV
RLin	Input return loss		-12		dB
RLout	Output return loss		-12		dB
VDC	Bias Voltage		4.5		V
IDC	Bias Current (on ports DC_I or DC_R)		33		µA

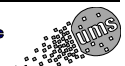
These values are representative of on board measurements as defined page 8, with 100kΩ resistor in parallel on pads Vdet\_I, Vref\_I, Vdet\_R and Vref\_R (see notes, page 9).

**Absolute Maximum Ratings (1)**

Tamb = +25°C

Symbol	Parameter	Values	Unit
VDC	Bias voltage (on ports DC_I and DC_R)	6	V
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C
P_max	Maximum power (for transmitted and/or reflected power)	30	dBm

(1) Operation of this device above anyone of these paramaters may cause permanent damage.



# 12-27GHz Detector

# CHE1260-QAG

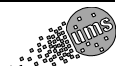
## Typical Package Sij parameters

*Preliminary*

Tamb = +25°C, Vdc = +4.5V (on DC\_I and DC\_R), 100k Ω resistor in parallel on pads Vdet\_I, Vref\_I, Vdet\_R and Vref\_R (see notes, page 9).

Freq (GHz)	dB(S11)	Ph(S11) (°)	dB(S12)	Ph(S12) (°)	dB(S2 1)	Ph(S21) (°)	dB(S22)	Ph(S22) (°)
2	-27.2	43	-0.2	-35	-0.2	-35	-26.8	34
3	-24.0	33	-0.2	-53	-0.2	-53	-23.8	21
4	-21.7	18	-0.3	-70	-0.3	-70	-21.3	5
5	-19.9	3	-0.3	-87	-0.3	-88	-19.6	-11
6	-18.4	-15	-0.4	-105	-0.4	-105	-18.2	-27
7	-17.3	-33	-0.4	-122	-0.4	-122	-16.9	-43
8	-16.1	-51	-0.5	-140	-0.5	-140	-15.8	-58
9	-15.2	-70	-0.5	-157	-0.5	-157	-14.9	-74
10	-14.5	-88	-0.6	-174	-0.6	-174	-14.1	-90
11	-13.7	-107	-0.7	168	-0.7	168	-13.3	-105
12	<b>-13.0</b>	<b>-124</b>	<b>-0.7</b>	<b>151</b>	<b>-0.7</b>	<b>151</b>	<b>-12.7</b>	<b>-121</b>
13	<b>-12.5</b>	<b>-141</b>	<b>-0.8</b>	<b>134</b>	<b>-0.8</b>	<b>134</b>	<b>-12.3</b>	<b>-138</b>
14	<b>-12.3</b>	<b>-157</b>	<b>-0.8</b>	<b>117</b>	<b>-0.8</b>	<b>117</b>	<b>-12.3</b>	<b>-155</b>
15	<b>-12.6</b>	<b>-172</b>	<b>-0.8</b>	<b>100</b>	<b>-0.8</b>	<b>100</b>	<b>-12.7</b>	<b>-172</b>
16	<b>-13.3</b>	<b>172</b>	<b>-0.8</b>	<b>82</b>	<b>-0.8</b>	<b>82</b>	<b>-13.6</b>	<b>170</b>
17	<b>-14.6</b>	<b>157</b>	<b>-0.7</b>	<b>65</b>	<b>-0.7</b>	<b>65</b>	<b>-15.2</b>	<b>150</b>
18	<b>-17.5</b>	<b>142</b>	<b>-0.7</b>	<b>47</b>	<b>-0.7</b>	<b>47</b>	<b>-18.2</b>	<b>127</b>
19	<b>-22.5</b>	<b>131</b>	<b>-0.7</b>	<b>29</b>	<b>-0.7</b>	<b>29</b>	<b>-23.6</b>	<b>100</b>
20	<b>-34.9</b>	<b>161</b>	<b>-0.7</b>	<b>11</b>	<b>-0.7</b>	<b>11</b>	<b>-31.9</b>	<b>23</b>
21	<b>-24.9</b>	<b>-105</b>	<b>-0.7</b>	<b>-8</b>	<b>-0.7</b>	<b>-8</b>	<b>-25.1</b>	<b>-73</b>
22	<b>-18.8</b>	<b>-116</b>	<b>-0.8</b>	<b>-26</b>	<b>-0.8</b>	<b>-26</b>	<b>-19.6</b>	<b>-105</b>
23	<b>-15.9</b>	<b>-132</b>	<b>-0.9</b>	<b>-45</b>	<b>-0.9</b>	<b>-45</b>	<b>-17.3</b>	<b>-131</b>
24	<b>-15.1</b>	<b>-149</b>	<b>-1.0</b>	<b>-63</b>	<b>-1.0</b>	<b>-63</b>	<b>-16.2</b>	<b>-154</b>
25	<b>-14.6</b>	<b>-163</b>	<b>-1.1</b>	<b>-81</b>	<b>-1.1</b>	<b>-81</b>	<b>-15.9</b>	<b>-176</b>
26	<b>-15.3</b>	<b>-178</b>	<b>-1.2</b>	<b>-99</b>	<b>-1.2</b>	<b>-99</b>	<b>-15.9</b>	<b>160</b>
27	<b>-16.3</b>	<b>165</b>	<b>-1.2</b>	<b>-118</b>	<b>-1.2</b>	<b>-118</b>	<b>-16.2</b>	<b>136</b>
28	-17.6	153	-1.3	-137	-1.3	-137	-17.0	110
29	-18.9	138	-1.4	-156	-1.4	-156	-17.1	83
30	-21.0	125	-1.5	-175	-1.4	-175	-17.9	53
31	-24.9	121	-1.5	165	-1.6	165	-18.7	15
32	-30.0	140	-1.6	145	-1.6	145	-19.7	-32
33	-23.0	-169	-1.7	125	-1.7	124	-18.1	-91
34	-16.4	-179	-1.9	103	-1.9	103	-14.4	-139
35	-12.2	163	-2.3	82	-2.3	82	-11.1	-174
36	-9.4	147	-2.8	61	-2.8	61	-8.1	159
37	-7.3	129	-3.4	41	-3.4	41	-6.5	135
38	-5.8	114	-3.9	23	-3.9	23	-5.5	117
39	-5.4	101	-4.2	7	-4.2	7	-5.3	102
40	-5.3	91	-4.0	-11	-4.0	-11	-5.5	91
41	-7.4	73	-4.5	-34	-4.4	-34	-7.2	71
42	-9.2	68	-4.3	-58	-4.4	-58	-9.8	69
43	-10.3	84	-4.7	-85	-4.7	-85	-11.6	93
44	-7.6	96	-5.7	-112	-5.7	-112	-7.3	105
45	-4.9	90	-7.1	-136	-7.0	-136	-4.4	97
46	-2.9	79	-8.8	-161	-8.7	-160	-2.6	84
47	-2.1	68	-11.0	179	-10.8	178	-1.5	71
48	-1.9	56	-12.7	163	-12.7	162	-0.9	56
49	-1.8	48	-14.4	142	-14.3	141	-0.9	41
50	-2.0	40	-16.8	123	-16.8	123	-1.5	28

Refer to the "definition of the Sij reference planes" section below.

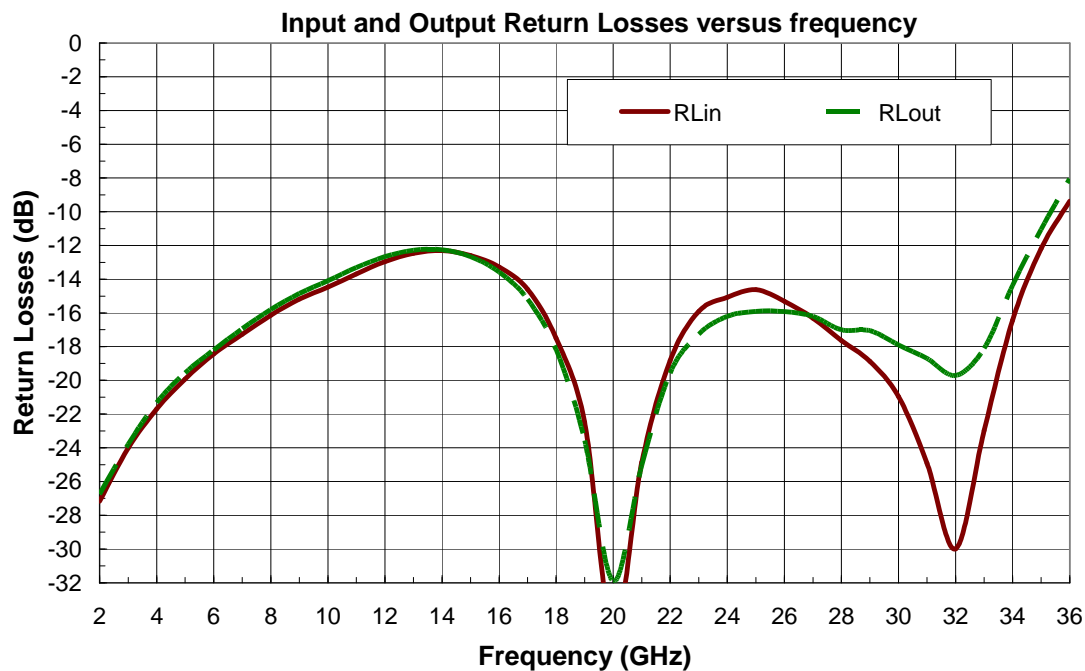
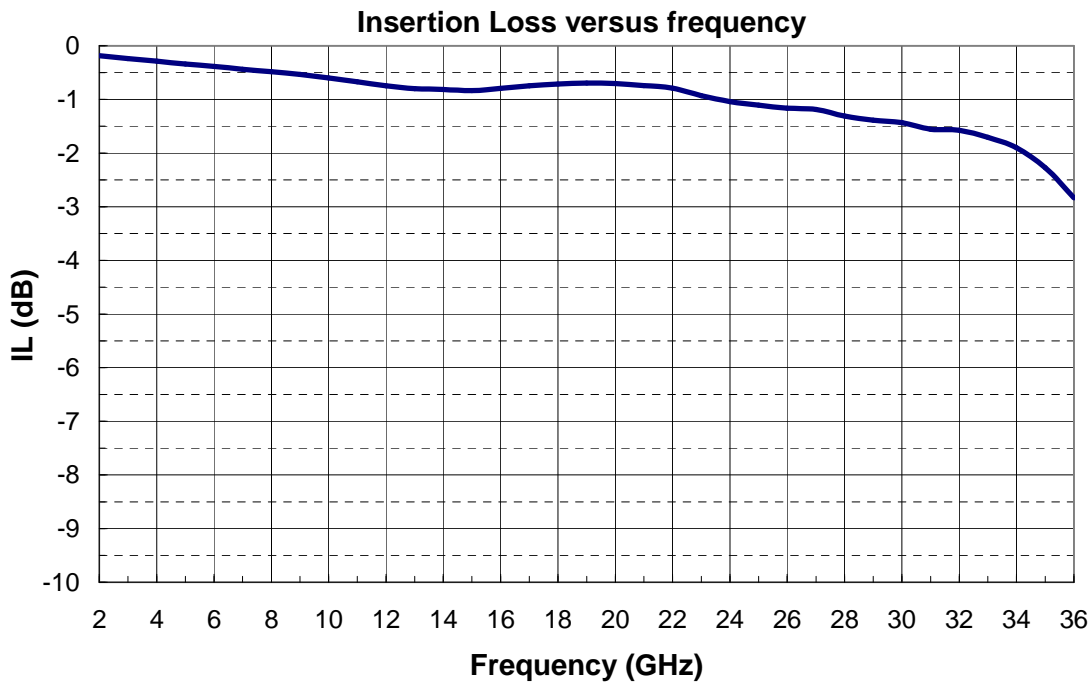


## Typical Measured Performance

*Preliminary*

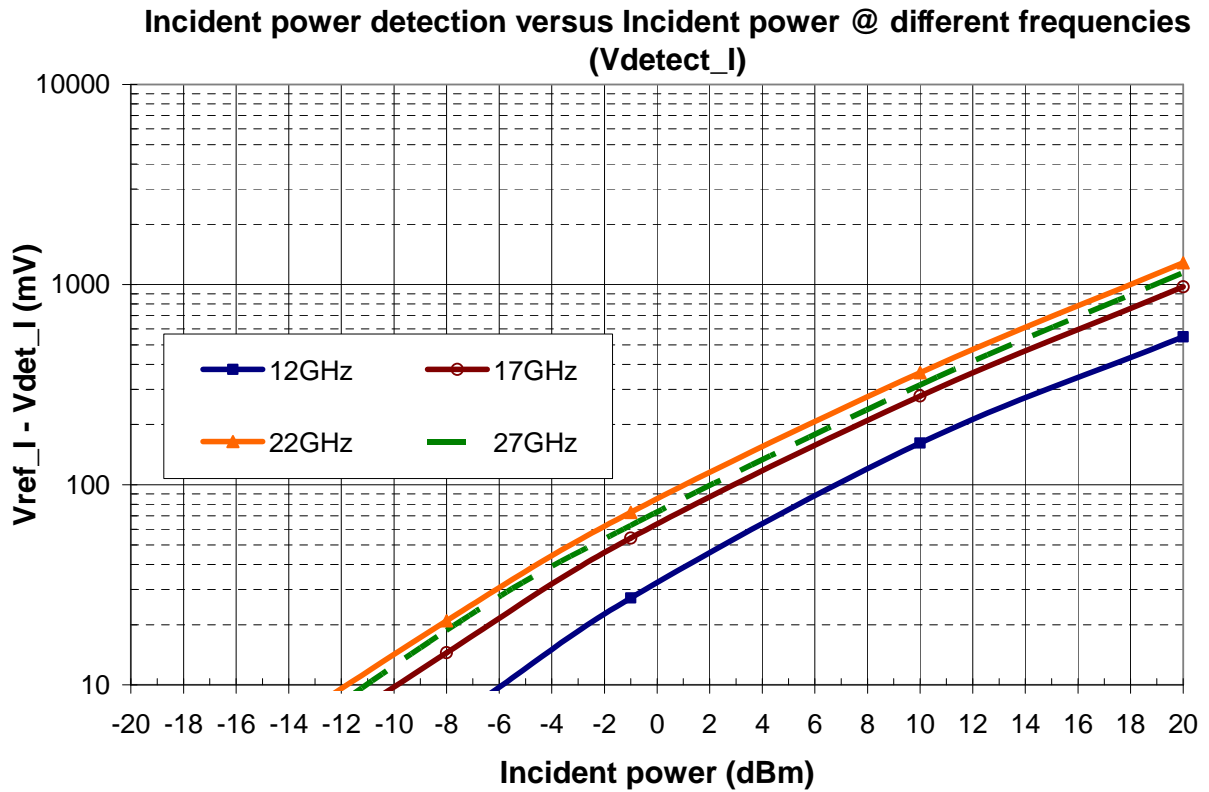
Tamb = +25°C, Vdc = +4.5V (on DC\_I and DC\_R), 100k Ω resistor in parallel on pads Vdet\_I, Vref\_I, Vdet\_R and Vref\_R (see notes, page 9).

- Losses measurements in the package access plans (refer to the “definition of the Sij reference planes” section below).



- Power measurements in the plan of the connectors, using the proposed land pattern & board 96272-B (see page 10).

*Preliminary*



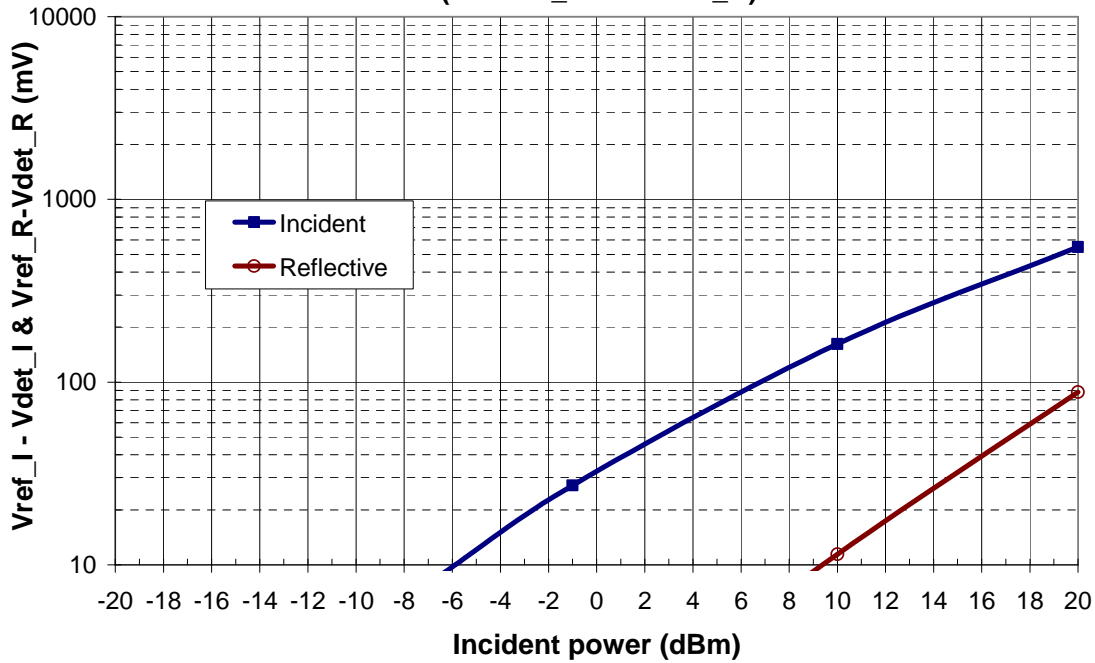
The CHE1260-QAG is a bidirectionnal detector using a symmetrical bidirectionnal coupler. Therefore the incident power detection versus incident power is identical to the reflective power detection versus reflected power.

The reflective power detection versus incident power depends on both the coupler directivity and the reflective environment of the package.

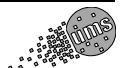
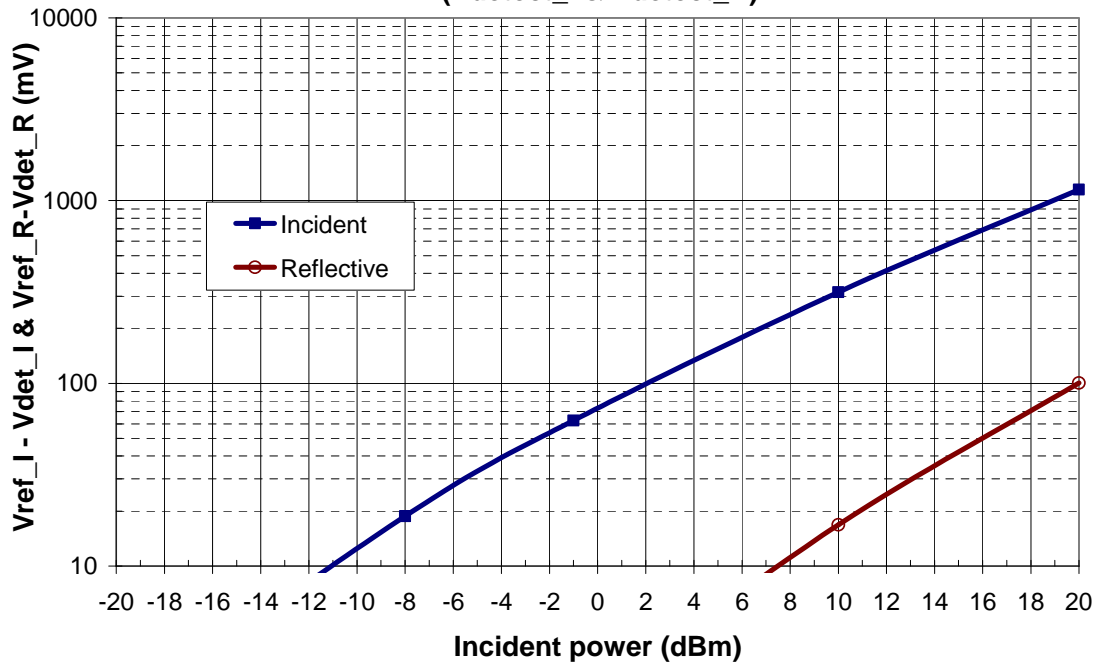
The following typical measured performance are obtained for a packaged detector, assembled on a connectorized board.

*Preliminary*

Incident and reflective power detection versus Incident power @ 12GHz  
(Vdetect\_I & Vdetect\_R)



Incident and reflective power detection versus Incident power @ 27GHz  
(Vdetect\_I & Vdetect\_R)

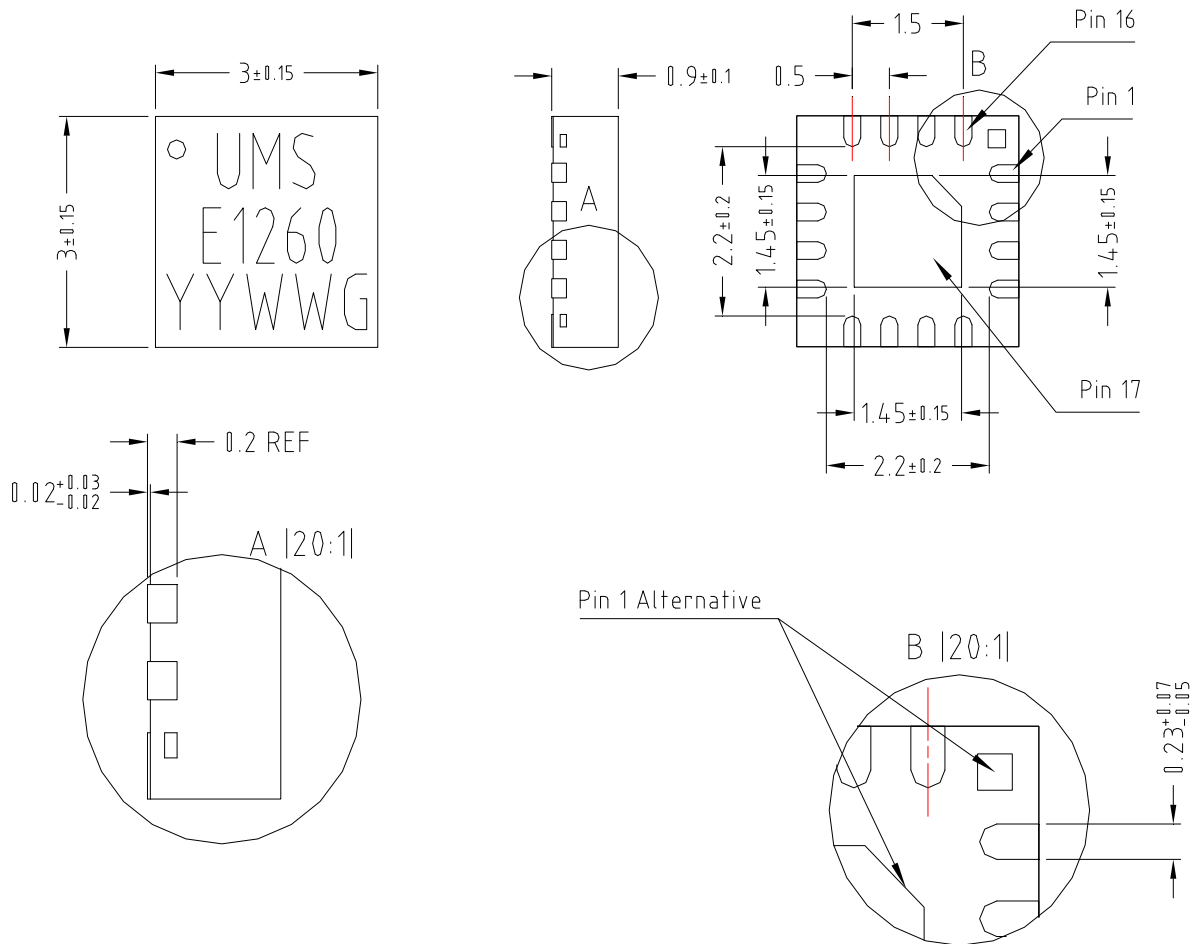


# 12-27GHz Detector

# CHE1260-QAG

Package outline:

*Preliminary*



Matt tin, Lead free (Green)

Units : mm

From the standard : JEDEC M0-220 [VEED-6]

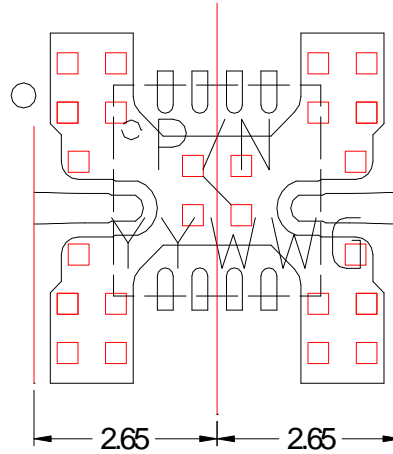
1-Nc	9-Gnd	17-( Exposed Pad ) GND
2-Gnd	10-RF OUT	
3-RF IN	11-Gnd	
4-Gnd	12-Nc	
5-DET I	13-Nc	
6-DC I	14-DET R	
7-REF I	15-DC R	
8-Nc	16-REF R	

*Preliminary*

## Definition of the Sij reference planes

The reference planes are defined from the footprint of the recommended characterization board shown here

The reference is the symmetrical axis of the package. The input and output reference planes are located at 2.65mm offset (input wise and output wise respectively) from this axis. Then, the given Sij incorporates this land pattern.



## SMD mounting procedure

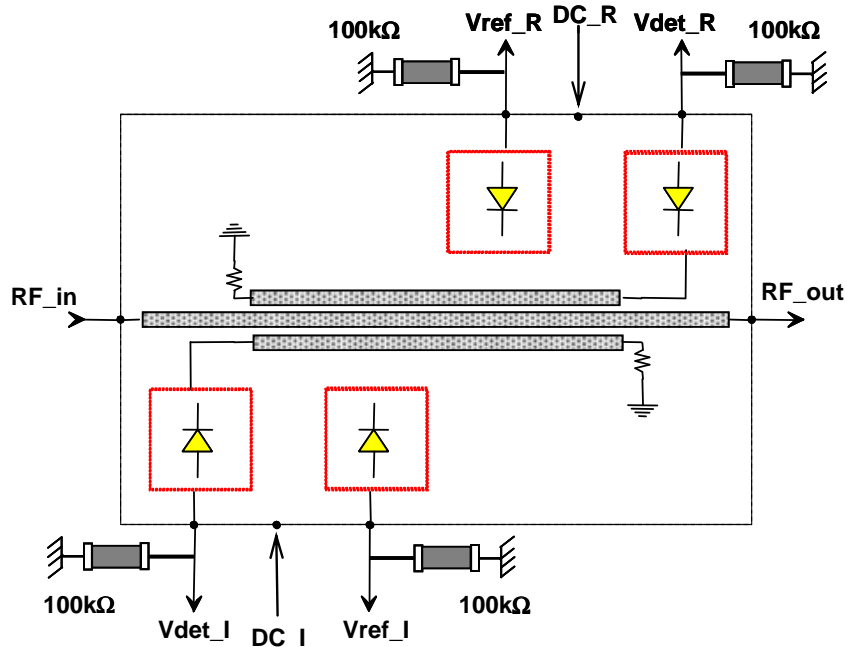
The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.



## Notes

*Preliminary*



Recommended external resistors assembly

100kΩ resistors in parallel with Vdet\_I, Vref\_I, Vdet\_R and Vref\_R pads are recommended to provide the best behaviour in the whole operating temperature range.

As the voltage detection is the difference between Vref\_X and Vdet\_X (X= I or R), the external resistor value should be identical on these ports. For information, a variation of 2% leads around 1mV variation of detected voltage.

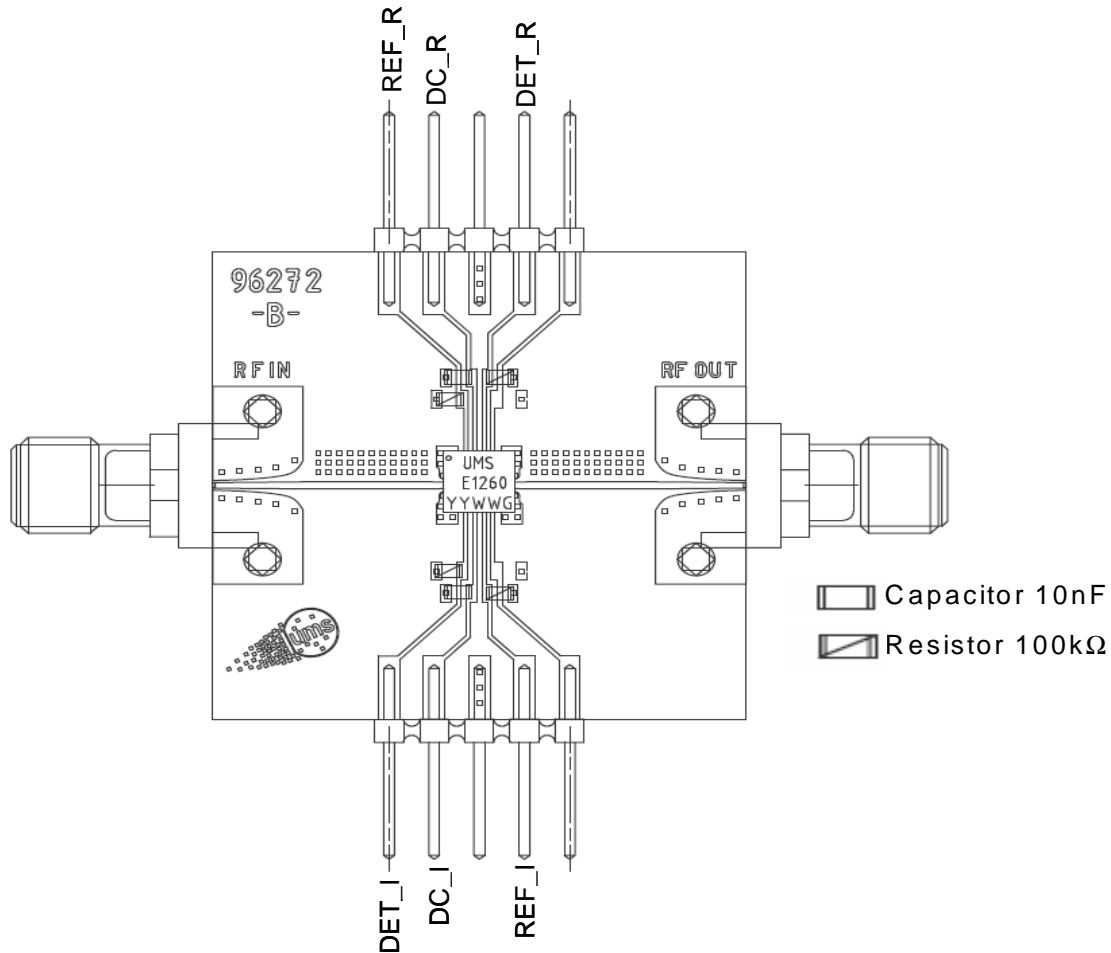
ESD protections are implemented on Vdet\_I, Vref\_I, Vdet\_R and Vref\_R accesses.

The DC connections (DC\_R & DC\_I) do not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

## Proposed Assembly board "96272-B" for the 16L-QFN3x3 products characterization

*Preliminary*

- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.



## Ordering Information

QFN 3x3 RoHS compliant package: CHE1260-QAG/XY  
 Stick: XY = 20      Tape & reel: XY = 21

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