12-40GHz Wide Band Detector

Preliminary

GaAs Monolithic Microwave IC in SMD leadless package

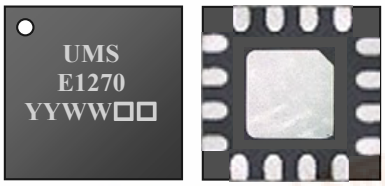
Description

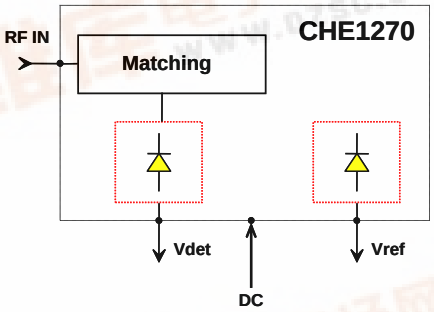
The CHE1270-QAG is a detector that integrates a matched detector diode (Vdet) and a reference diode (Vref).

It is designed for a wide range of applications where an accurate transmitted power control is required, typically commercial communication systems.

The circuit is manufactured with a Schottky diode MMIC process, 1µm gate length, via holes through the substrate and air bridges.

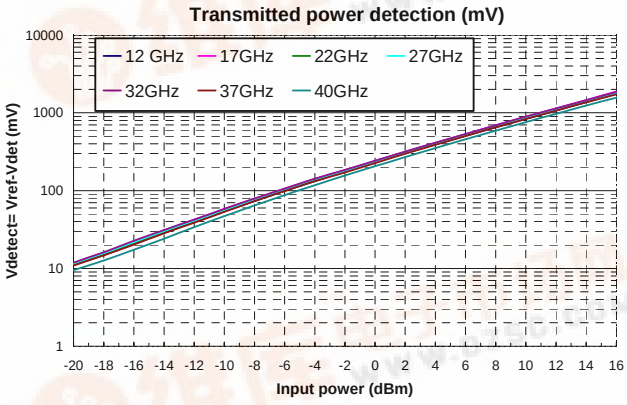
It is available in leadless SMD package.





Main Features

- Wide frequency range: 12-40GHz
- 30dB dynamic range
- ESD protected
- 16L-QFN3x3 SMD package



Main Characteristics

Tamb = +25℃, VDC = +4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	12		40	GHz
Dr	Dynamic range		30		dB
RL	Return Loss		-10		dB

ESD Protection: Electrostatic discharge sensitive device. Observe handling precautions!

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Electrical Characteristics (1)

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Tamb = +25°C, VDC = +4.5V

Symbol	Parameter	Min	Typ	Max	Unit
F	Frequency range	12		40	GHz
Dr	Dynamic range (for Input Power detection)		30		dB
IPd	Input Power detection	-15		15	dBm
Vdetect	Voltage detection Vref – Vdet from IPd_min to IPd_max		10 to 2000		mV
RL	Return Loss (12 – 36GHz) Return Loss (36 – 40GHz)		-10 -8		dB dB
VDC	Bias Voltage		4.5		V
IDC	Bias Current		70		µA

(1) These values are representative of onboard measurements as defined on the drawing 96272-B (page 8) with 27kΩ resistor in parallel on Vdet and Vref pads.

Absolute Maximum Ratings (1)

Tamb = +25°C

Symbol	Parameter	Values	Unit
VDC	Bias voltage	6	V
P_max	Maximum Power	18	dBm
Top	Operating temperature range	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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Typical Measured Performance

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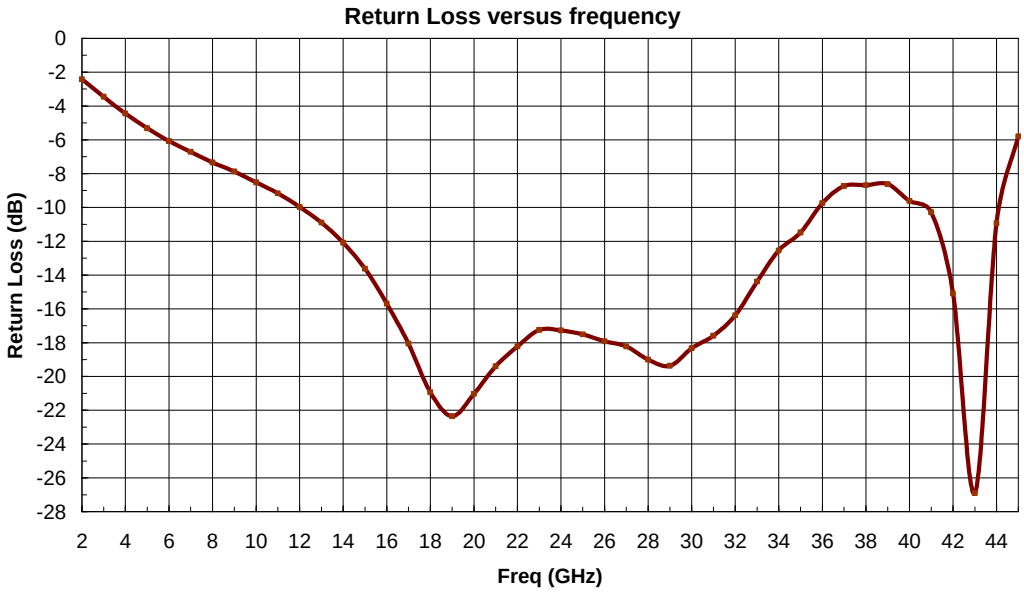
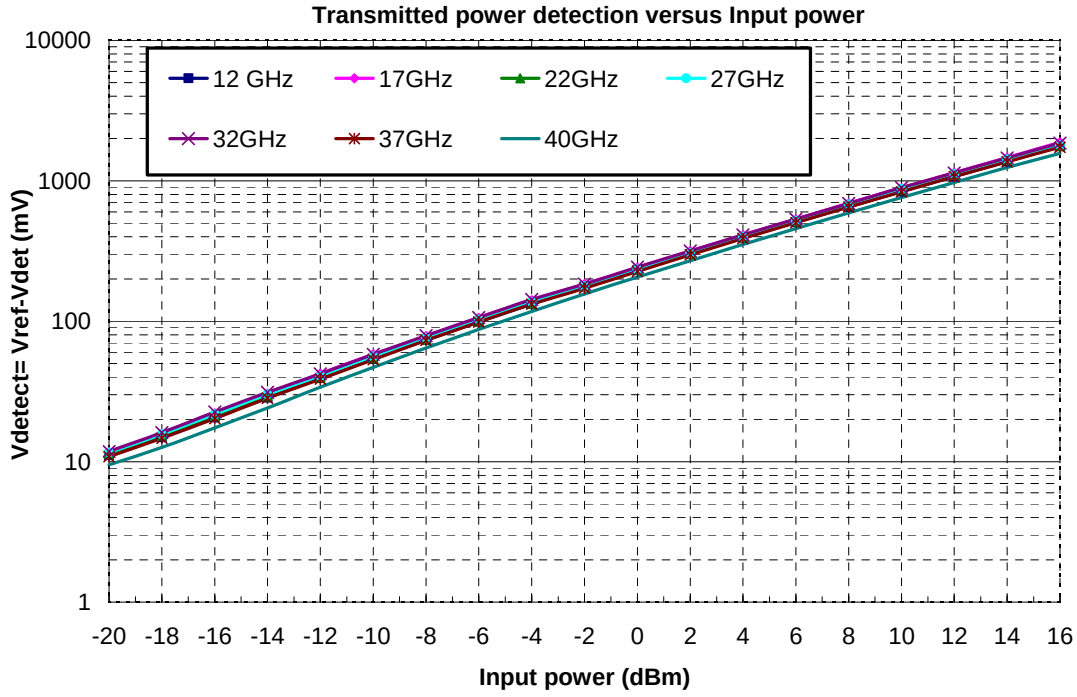
Tamb = +25°C, Vdc = +4.5V, 27kΩ resistor in parallel on Vdet and Vref pads (see notes, page 7).

- Return Loss measurement in the package access plans (refer to the "definition of the Sij reference planes" section below).



- Power measurements in the plan of the connectors, using the proposed land pattern & board 96272-B (see page 8).



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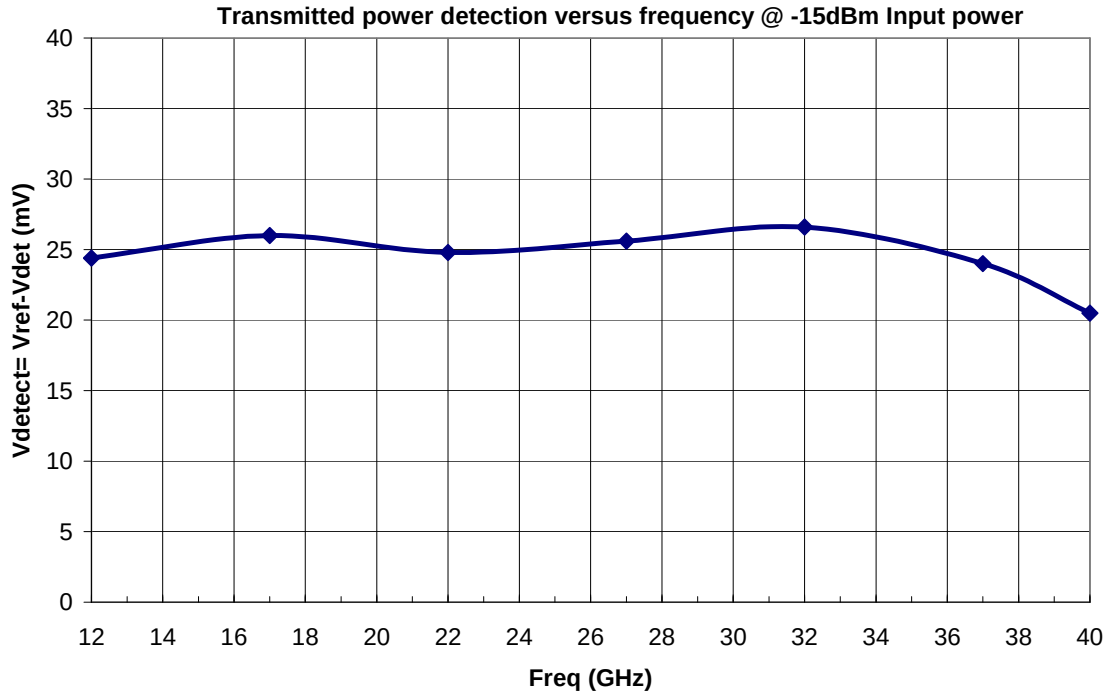

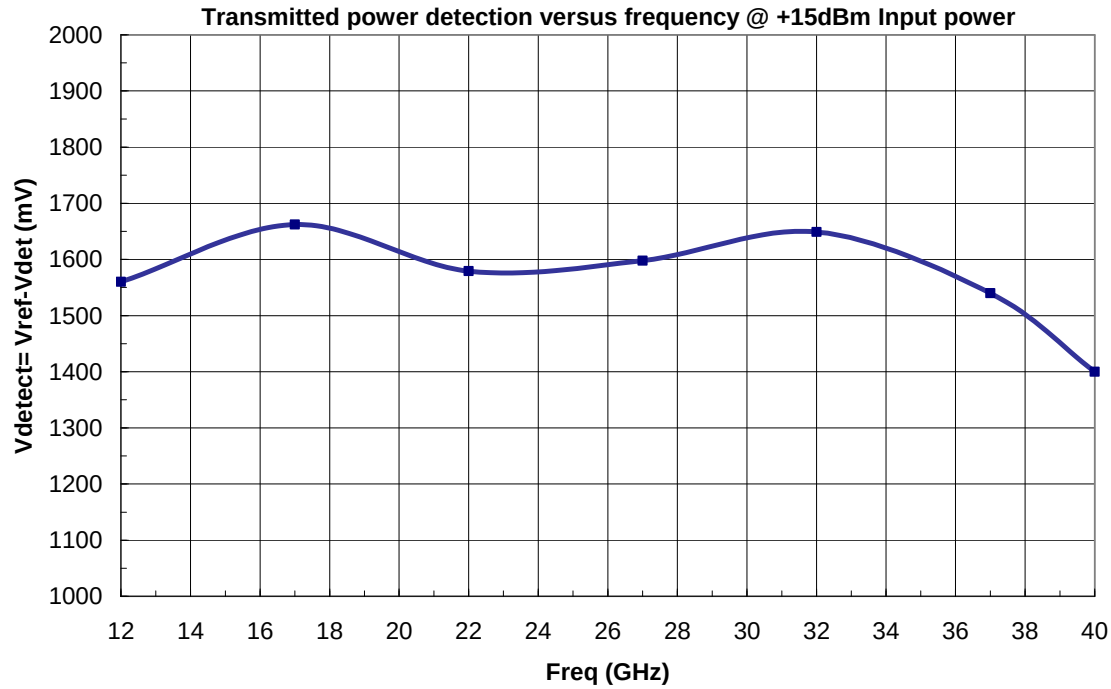

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Package outline [(1)]:

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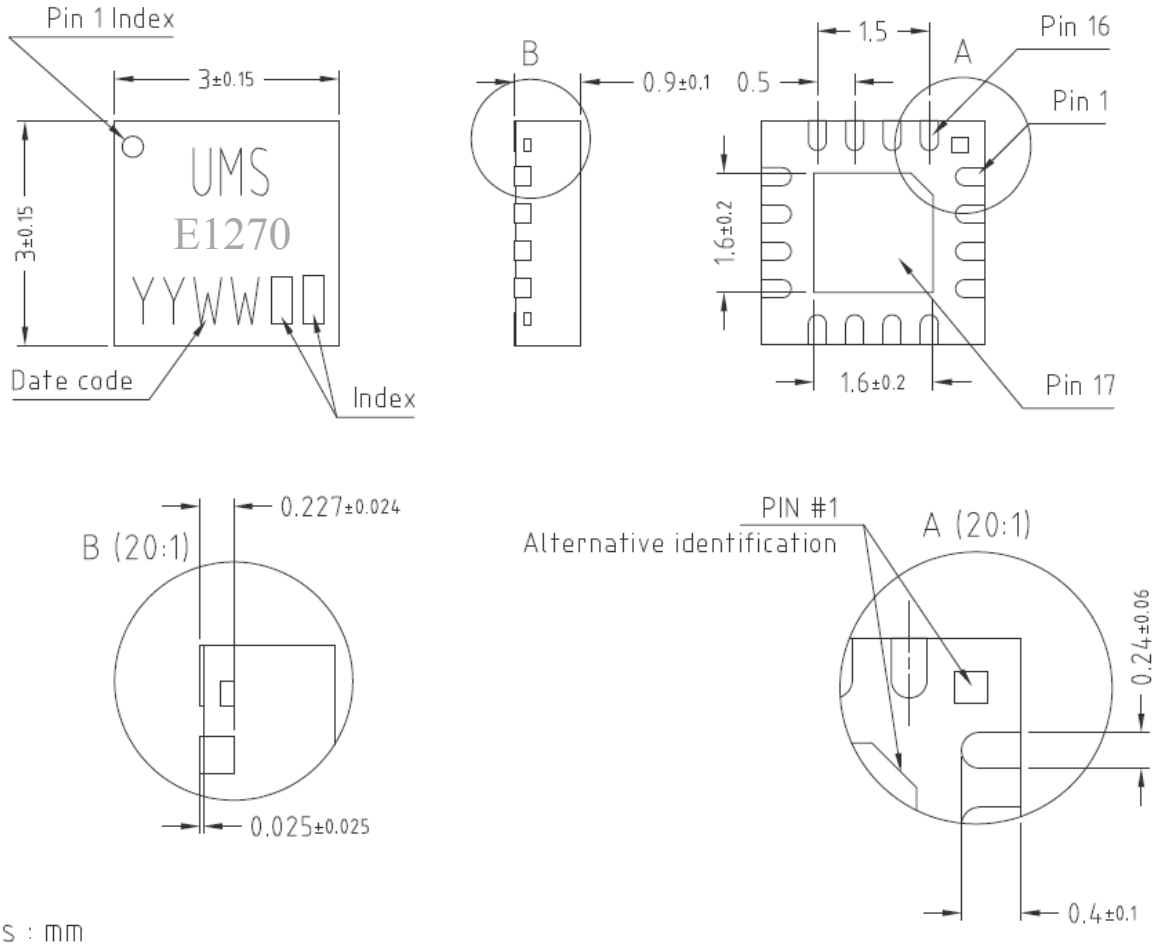

Units : mm
From the standard : JEDEC MO-220 [VEED]
Matt tin, Lead free (Green)

Matt tin, Lead Free	(Green)	1-	Nc	9-	Gnd
Units	mm	2-	Gnd	10-	Nc
From the standard	JEDEC MO-220	3-	RF IN	11-	Gnd
	(VEED)	4-	Gnd	12-	Nc
17- GND		5-	VDET	13-	Nc
		6-	DC	14-	Nc
		7-	VREF	15-	Nc
		8-	Nc	16-	Nc

[(1)]The package outline drawing included to this data-sheet is given for indication. Refere to the application note AN0017 available at http://www.ums-gaas.com for exact package dimensions.

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Definition of the Sij reference planes

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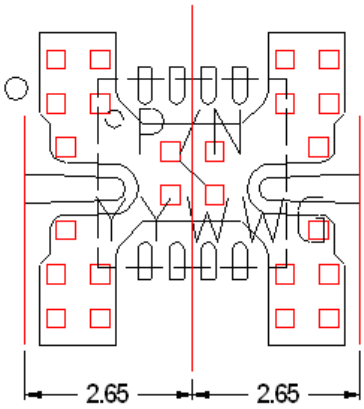
The reference planes used for Sij measurements given above are symmetrical from the symmetrical axis of the package (see drawing beside). The input and output reference planes are located at 2.65mm offset (input wise and output wise respectively) from this axis. Then, the given Sij parameters incorporate the land pattern of the evaluation motherboard recommended at the page 8.



Recommanded package footprint

Refere to the application note AN0017 available at http://www.ums-gaas.com for package foot print recommandations.

SMD mounting procedure

The SMD leadless package has been designed for high volume surface mount PCB assembly process. The dimensions and footprint required for the PCB (motherboard) are given in the drawings above.

For the mounting process standard techniques involving solder paste and a suitable reflow process can be used. For further details, see application note AN0017.

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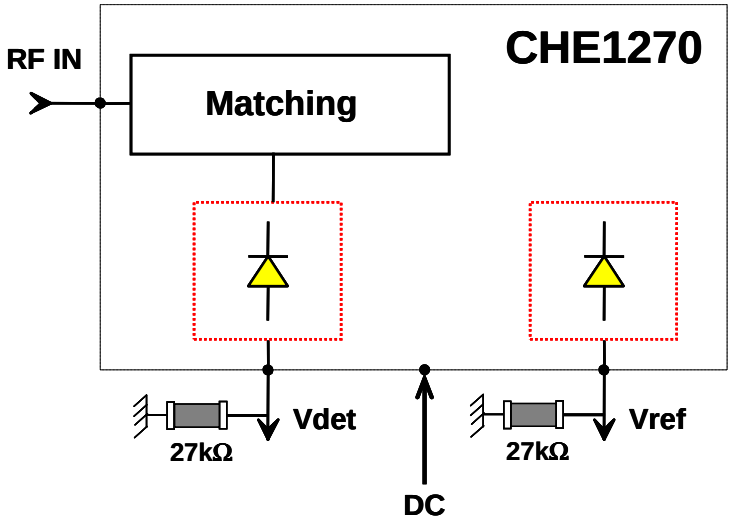
Notes

Preliminary



Recommended external resistors assembly

27kΩ resistors in parallel with Vdet and Vref pads are recommended to provide the best behaviour in the whole operating temperature range.

As the voltage detection is the difference between Vref and Vdet, the external resistor value should be identical on these two ports.
For information, a variation of 3% leads around 1mV variation of detected voltage.

Due to ESD protection circuits on RF input, an external capacitance might be requested to isolate the product from external voltage that could be present on the RF access.
ESD protections are also implemented on Vdet and Vref accesses.

The DC connection (on DC pad) does not include any decoupling capacitor in package, therefore it is mandatory to provide a good external DC decoupling on the PC board, as close as possible to the package.

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Evaluation mother board:

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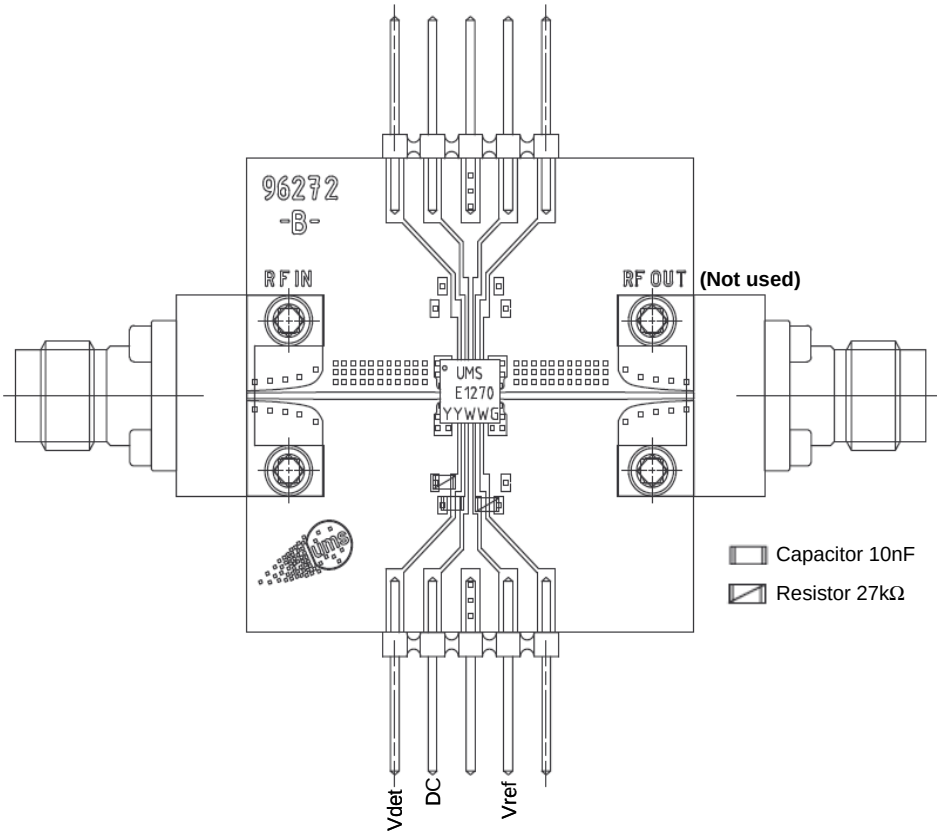
- Compatible with the proposed footprint.
- Based on typically Ro4003 / 8mils or equivalent.
- Using a microstrip to coplanar transition to access the package.
- Recommended for the implementation of this product on a module board.
- Decoupling capacitors of 10nF ±10% are recommended for all DC accesses.
- (See application note AN0017 for details).



Ordering Information

QFN 3x3 RoHS compliant package: CHE1270-QAG/XY
Stick: XY = 20 Tape & reel: XY = 21

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