

## Fully Integrated HBT K-band VCO

### GaAs Monolithic Microwave IC In QFN package

#### Description

The CHV2411a-QDG is a monolithic multifunction for frequency generation. It integrates a X-band "push-push" oscillator with frequency control (VCO) thanks to base-collector diodes, used as varactors, a K-band buffer amplifiers and a divider by 8. The VCO is fully integrated on HBT process. All the active devices are internally self biased.

The circuit is fully integrated on InGaP HBT process: 2µm emitter length, via holes through the substrate and high Q passive elements.

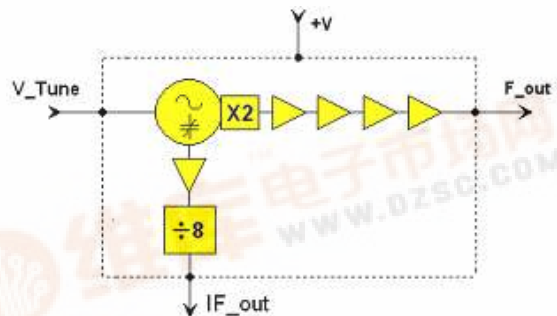
The chip is delivered in a 24 Leads RoHS compliant QFN4x4 package.

#### Main Features

- K-band VCO+K-band buffers+Prescalar/8
- Fully integrated VCO (no need for external Resonator)
- Low phase noise
- High temperature range
- High frequency stability
- On chip self biased devices
- Standard SMD package : 24L-QFN4x4

#### Main Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
F_out	Specified output frequency range	24	24.125	24.25	GHz
F_vco	Oscillator frequency		F_out/2		GHz
IF_out	Output Intermediate frequency		F_out/16		GHz
Pout	Output power at F_out	13	16		dBm
PFI	Output power at Intermediate frequency (IF)	-3	0		dBm
PN	SSB Phase Noise @ F_out @ 100 kHz		-90	-80	dBc/Hz



Multifunction block diagram



Plastic package

**ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !**



## Electrical Characteristics

### Full temperature range

#### VCO & buffer Part

Symbol	Parameters	Min	Typ	Max	Unit
F_out	Output Frequency range (Operating band)	24		24.25	GHz
F_vco	VCO frequency	F_out/2			
V_Tune	Voltage Tuning range	1		6	V
	Tuning sensitivity	250	400	725	MHz/V
	Frequency drift rate		5		MHz/°C
H1	Harmonics 1/2 F_out			-20	dBc
H3	Harmonics 3/2 F_out			-40	dBc
H4	Harmonics 2 F_out			-20	dBc
PN	SSB Phase Noise given @ F_out @ 100 KHz		-90	-80	dBc/Hz
	Main Output (RF_Out) VSWR		2:1		
	Pulling into 2:1 VSWR for all phases			8	MHz
	Pushing @ within the V_tune range			250	MHz/V
P_out	Output Power on RF_out port	13	16	19	dBm
	Positive supply current		140	170	mA

#### Prescalar Part

Symbol	Parameters	Min	Typ	Max	Unit
IF_out	IF Output Frequency		F_out/16		GHz
	Output Power	-3	0		dBm
	Positive supply current		80	110	mA
	Prescalar Output (IF) VSWR		2:1		

#### General

Symbol	Parameters	Min	Typ	Max	Unit
VB,V1,VB1,V2,V B2,VD	Positive supply voltage		5		V
+I (IB1+IB2+I1+I2)	Total Positive supply current		220	280	mA
Top	Operating temperature range	-40		+100	°C

All the parameters are specified between 1V and 6V of Tuning Voltage

Remark :

The minimum and maximum values take into account the spread due to the operating temperature and process spread.

These performance has been obtained with the chip in QFN package assembled on the recommended boards (ref. 96348 B) described in this document. These performances are highly dependent on this environment.

## Absolute Maximum Ratings <sup>(1)</sup>

Symbol	Parameters	Values	Unit
V_tune	Positive Tuning voltage	10	V
+V	Positive supply voltage	6	V
+ID	Positive supply current (Prescalar)	120	mA
+IB1 / +IB2	Positive supply current (buffers 2 & 3)	50 / 55	mA
+I1 / +I2	Positive supply current (VCO+ buffer 1)	35 / 50	mA
+IB	Positive supply current (prescalar's buffer)	15	mA
Top	Operating temperature range (2)	-40 to +100	°C
Tstg	Storage temperature range	-55 to +125	°C

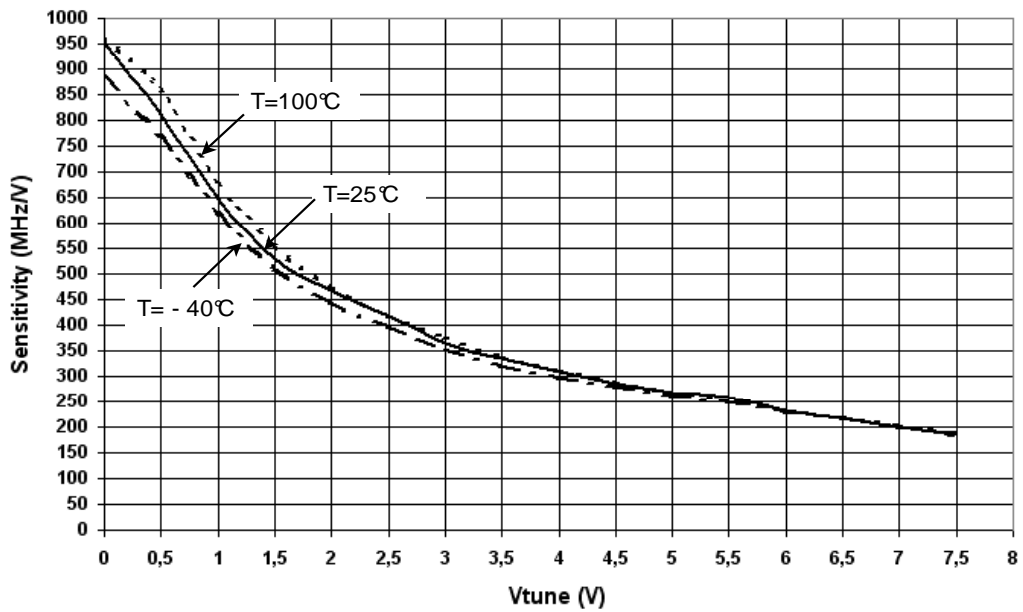
(1) Operation of this device above anyone of these parameters may cause permanent damage. Duration < 1s

(2) temperature of the back side of the QFN package

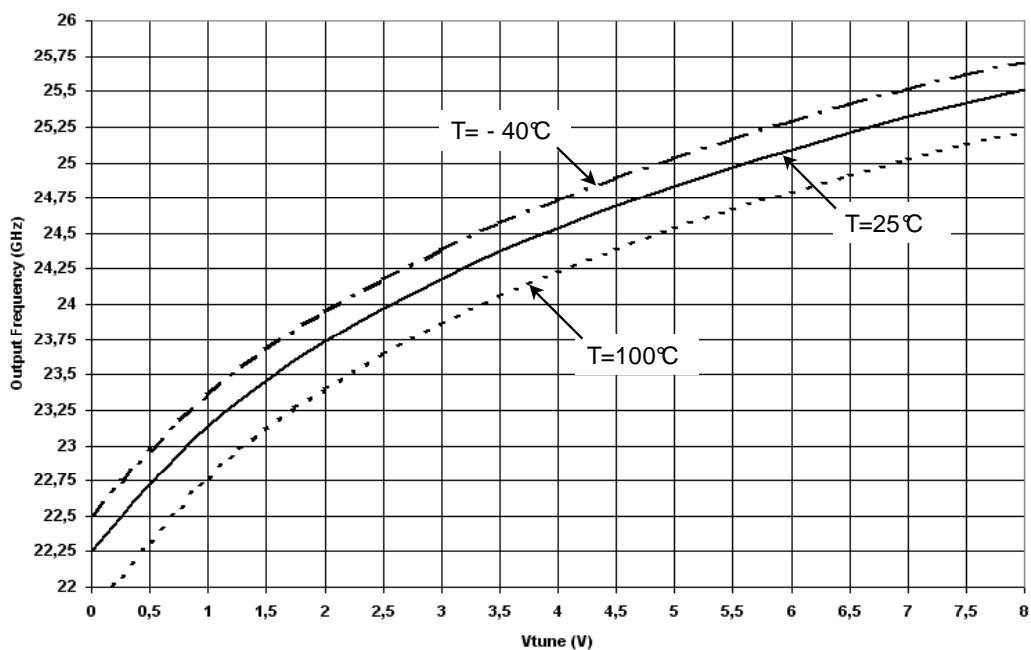
## Typical QFN measurements on board 95791 (QFN plan)

Remark : The temperature mentioned below is taken at the back side of the QFN package.

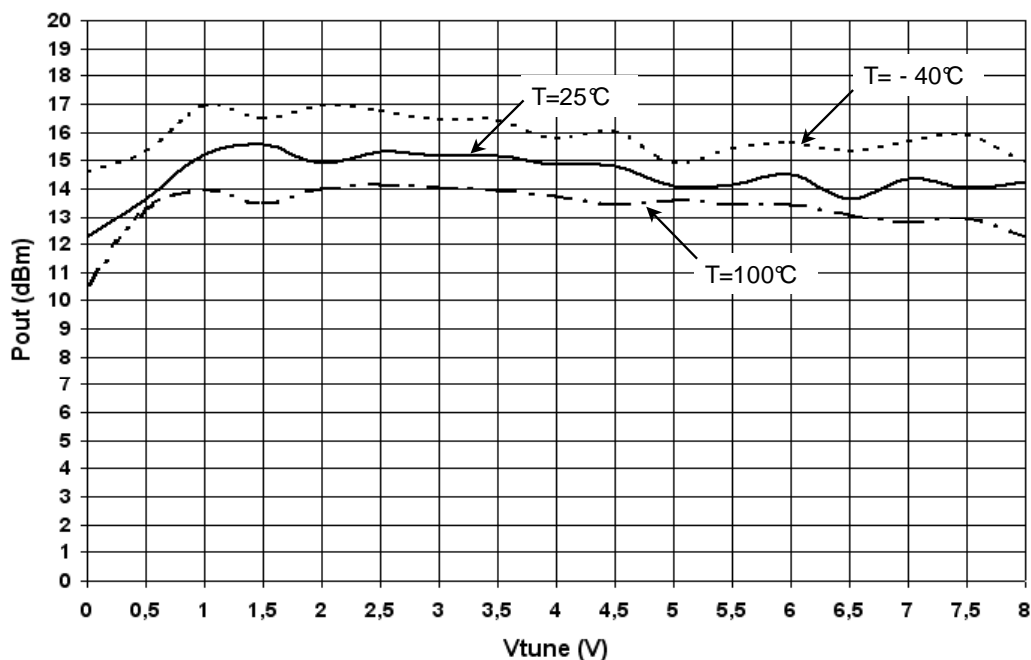
### Sensitivity versus Vtune



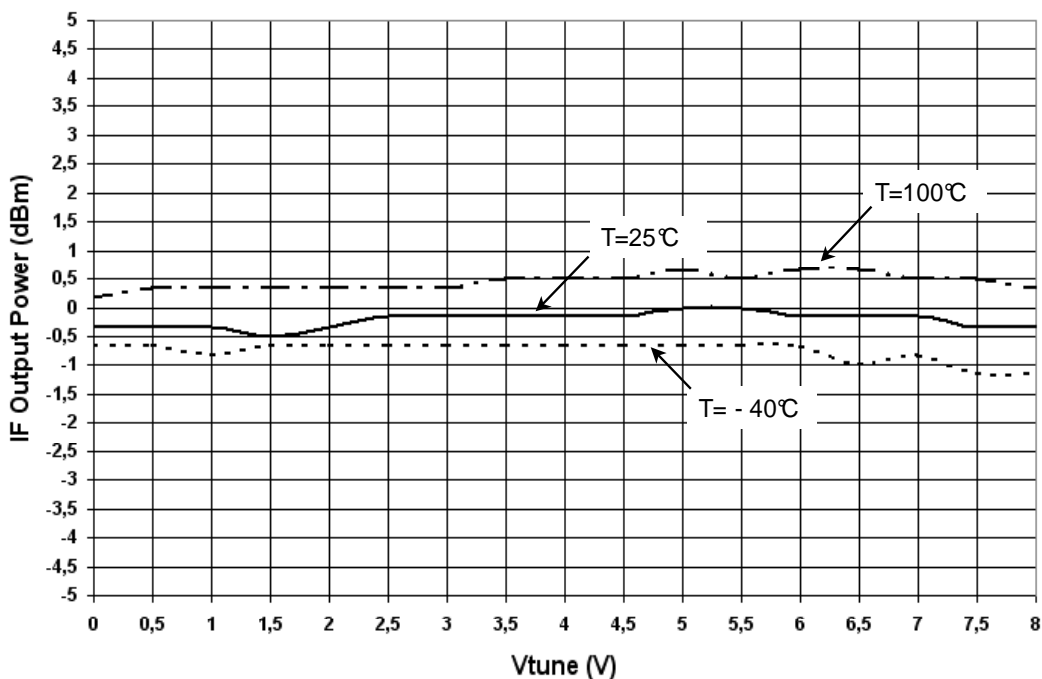
### Output Frequency versus Vtune



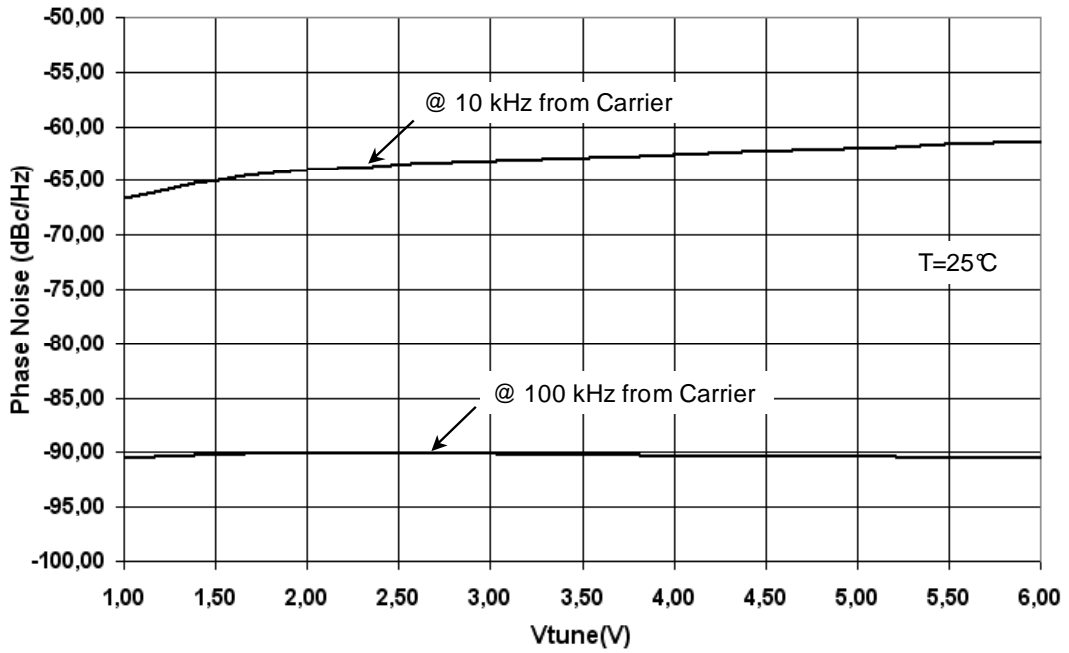
### Output Power @24GHz versus Vtune



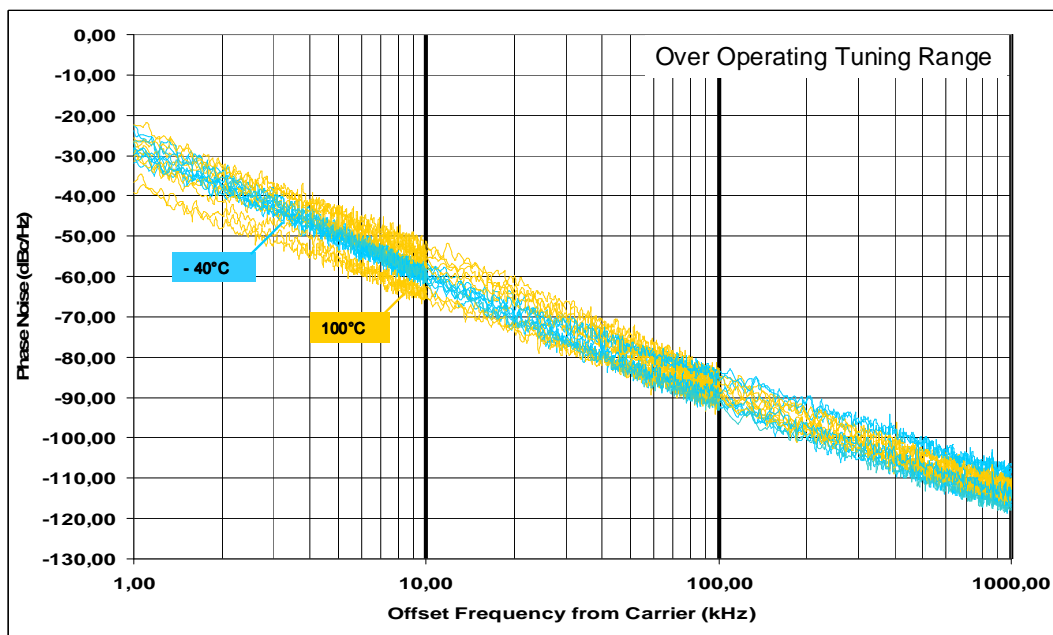
### IF Output Power versus Vtune



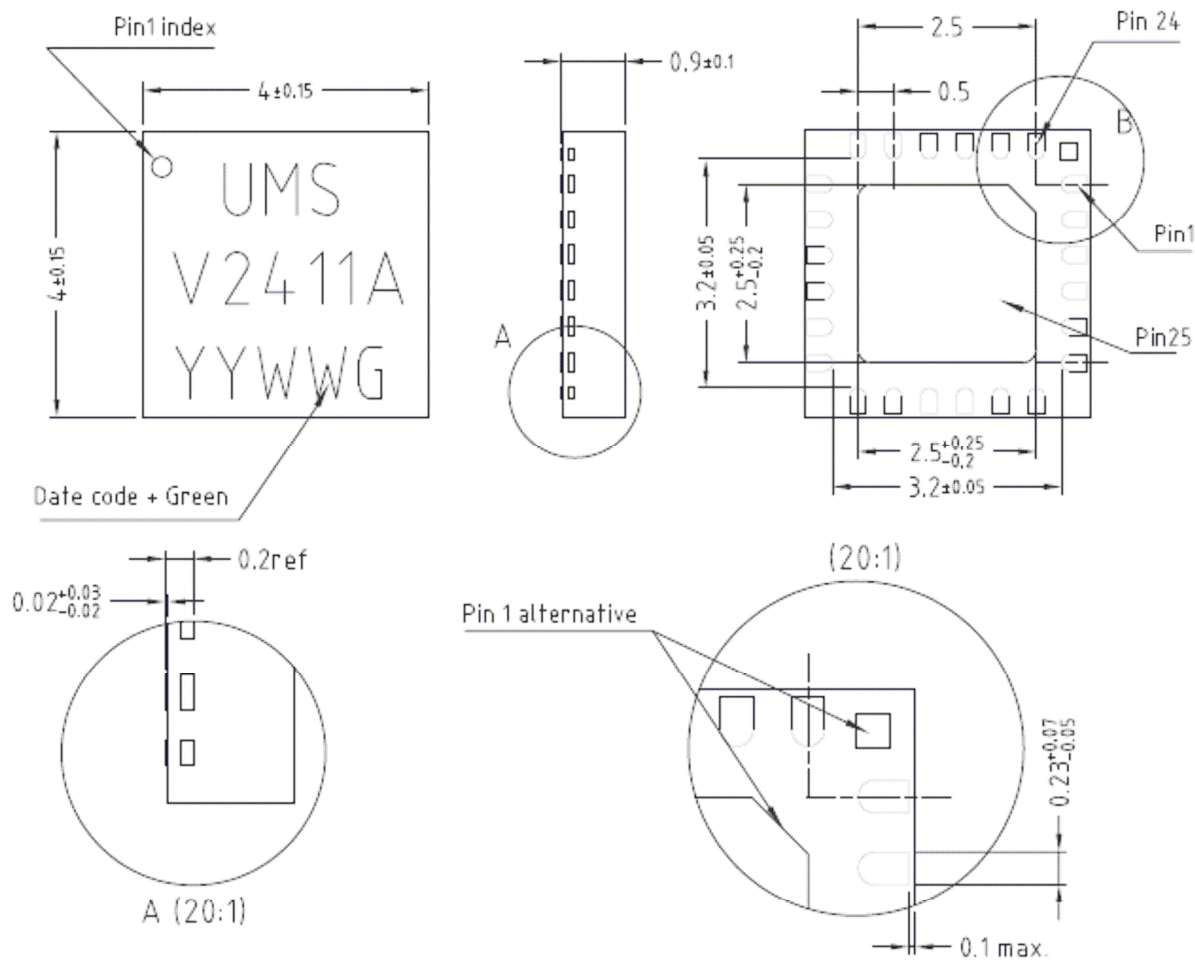
Phase Noise versus Vtune



Phase Noise versus Offset frequency from carrier



## QFN Outline



Units : mm

From the standard : JEDEC MO-220

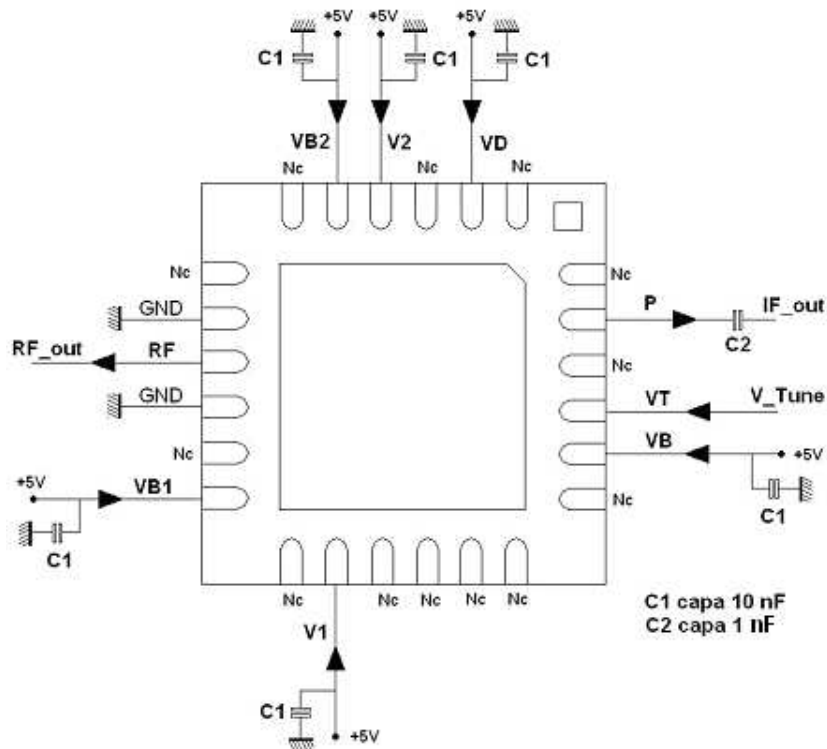
Matt tin, Lead free (Green)

1- Nc	13- VB1	25- Gnd
2- P	14- Nc	
3- Nc	15- Gnd	
4- VT	16- RF	
5- VB	17- Gnd	
6- Nc	18- Nc	
7- Nc	19- Nc	
8- Nc	20- VB2	
9- Nc	21- V2	
10- Nc	22- Nc	
11- V1	23- VD	
12- Nc	24- Nc	

## QFN Pin-out description

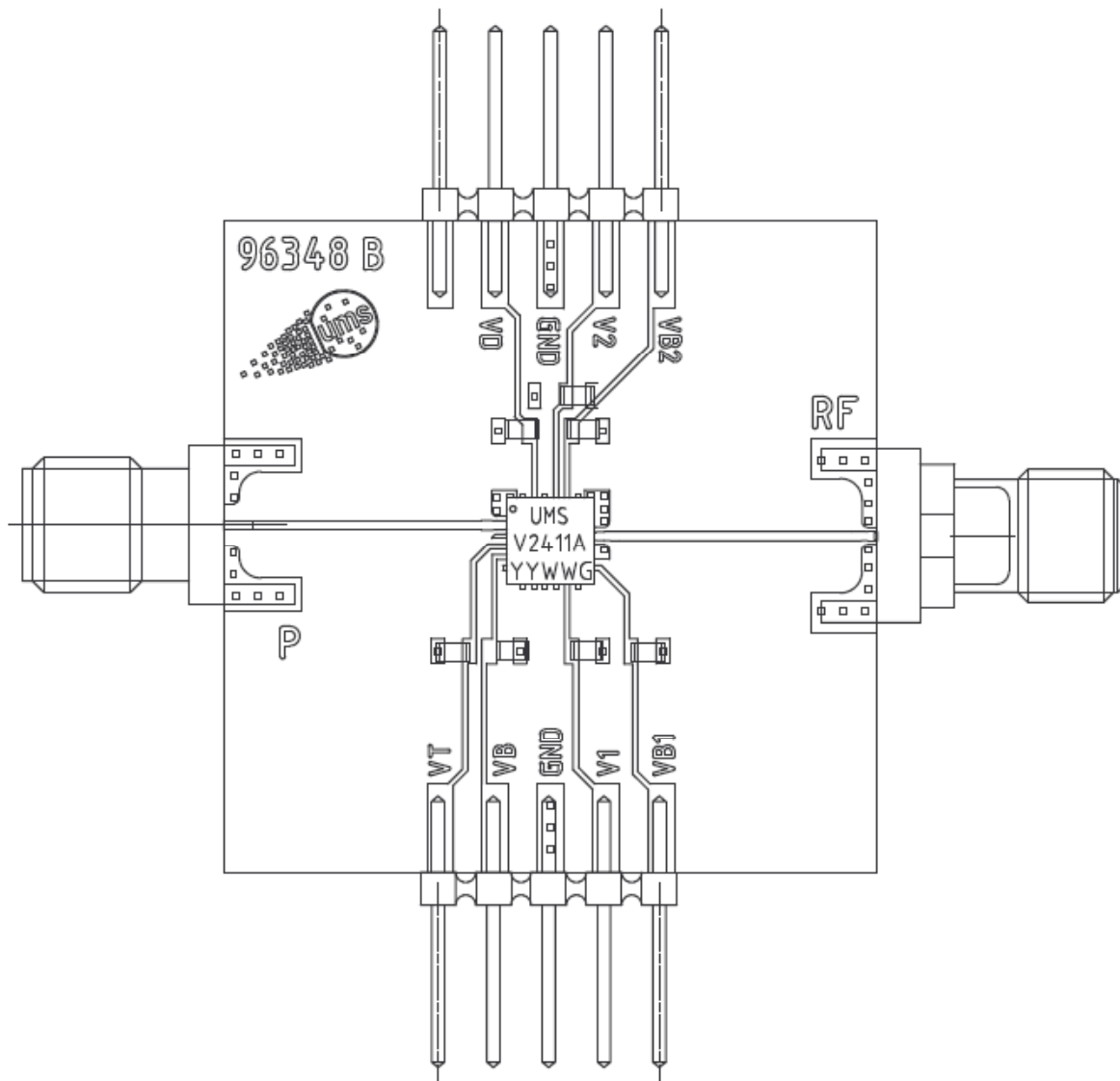
Pin number	Pin name	Symbol Name	Description
15,17	GND		Ground
2	P	IF_out	IF output at 1.5 GHz
4	VT	V_Tune	Frequency Tuning Port
5,11,13,20,21,23	VB, V1, VB1, VB2,V2, VD	+V	Positive supply voltage
5	VB		Positive supply voltage of 12 GHz prescalar's buffer
11,21	V1,V2		Positive supply voltage of the VCO core+1 <sup>st</sup> stage of the 24GHZ buffers
13	VB1		Positive supply voltage of the 2 <sup>nd</sup> & 3 <sup>rd</sup> stages of the 24GHZ buffers
20	VB2		Positive supply voltage of the 4 <sup>th</sup> stages of the 24GHZ buffers
23	VD		Positive supply voltage of the Prescalar
16	RF	F_out	RF output at 24 GHz
2	P	F_out/16	Prescalar output at 1.5 GHz
1,3,6,7,8,9,10,12,14,18,19,22,24	Nc		Not connected

## External Components and bias configuration (recommended)



**Important:** Need for a capacitor on the prescalar output port as a DC block (C2).

Recommended Test Fixture (Ref. 96348 B) for measurements over Temperature Range



## ESD sensitivity

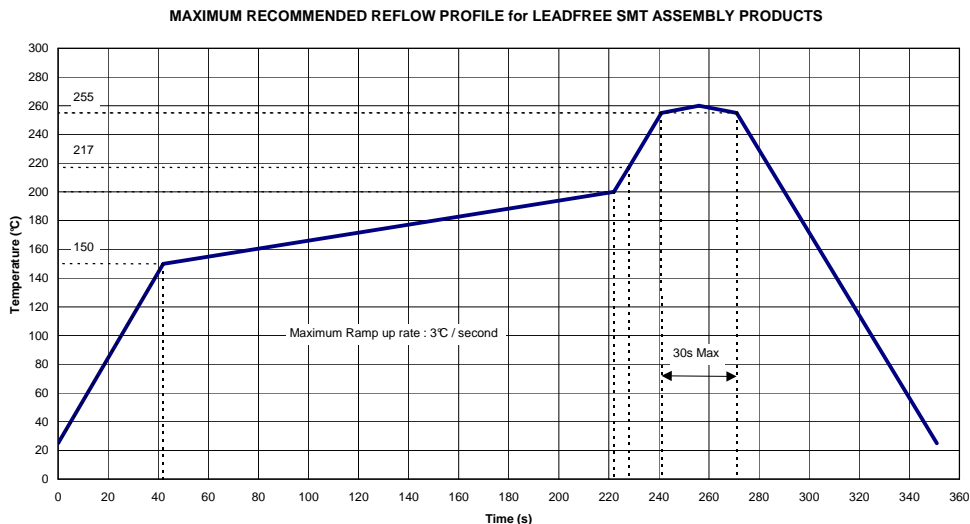
Norm	Value
MIL-STD-1686C	HBM Class 1 (<1000V)
ESD STM5.1-1998	HBM Class 0 (<250V)

## Package Information

Parameter	
Package body material	RoHS-compliant Low stress Injection Molded Plastic
Lead finish	100% matte Sn
MSL Rating	MSL1

## Recommended surface mount package assembly (see UMS AN0017)

For volume production the SMD type package can be treated as a standard surface mount component (please refer to the IPC/JEDEC J-STD-020C standard or equivalent). The assembly on the motherboard can be performed using a standard assembly process (e.g. stencil solder printing, standard pick-and-place machinery, and solder reflow oven). However, caution should be taken to perform a good and reliable contact over the whole pad area.



### Attention:

The solder thickness after reflow should be typical 50µm [2 mils] and the lateral alignment between the package and the motherboard should be within 50µm [2 mils].

It is important for the performance of the product that the whole overlapping area between the motherboard and package pads is connected. Voids or other improper connections, in particular, between the ground pads on motherboard and package will lead to a deterioration of the RF performance and the heat dissipation. The latter effect can reduce drastically reliability and lifetime of the product.

## Ordering Information

24L-QFN4x4 Lead Free Package : CHV2411aQDG/XY

Stick: XY=20                      Tape and reel: XY=21

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