# CMLDM8002A
# CMLDM8002AJ

## SURFACE MOUNT PICOmini™ DUAL P-CHANNEL ENHANCEMENT-MODE SILICON MOSFET

PICOmini™

SOT-563 CASE

**MARKING CODE: CMLDM8002A: C08**
**CMLDM8002AJ: CJ8**

Central™ Semiconductor Corp.

## DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLDM8002A and CMLDM8002AJ are dual chip Enhancement-mode P-Channel Field Effect Transistors, manufactured by the P-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM8002A utilizes the USA pinout configuration, while the CMLDM8002AJ, utilizing the Japanese pinout configuration, is available as a special order. These special Dual Transistor devices offer Low $R_{DS(on)}$ and Low $V_{DS(on)}$.

## FEATURES:

- Dual Chip Device
- Low $R_{DS(on)}$
- Low $V_{DS(on)}$
- Low Threshold Voltage
- Fast Switching
- Logic Level Compatible
- Small SOT-563 package

## APPLICATIONS:

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Powered Portable Equipment

## MAXIMUM RATINGS ($T_A$=25°C)

| | SYMBOL | | UNITS |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 50 | V |
| Drain-Gate Voltage | $V_{DG}$ | 50 | V |
| Gate-Source Voltage | $V_{GS}$ | 20 | V |
| Continuous Drain Current | $I_D$ | 280 | mA |
| Continuous Source Current (Body Diode) | $I_S$ | 280 | mA |
| Maximum Pulsed Drain Current | $I_{DM}$ | 1.5 | A |
| Maximum Pulsed Source Current | $I_{SM}$ | 1.5 | A |
| Power Dissipation | $P_D$ | 350 | mW (Note 1) |
| Power Dissipation | $P_D$ | 300 | mW (Note 2) |
| Power Dissipation | $P_D$ | 150 | mW (Note 3) |
| Operating and Storage Junction Temperature | $T_J$,$T_{stg}$ | -65 to +150 | °C |
| Thermal Resistance | $\Theta_{JA}$ | 357 | °C/W |

## ELECTRICAL CHARACTERISTICS PER TRANSISTOR ($T_A$=25°C unless otherwise noted)

| SYMBOL | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|
| $I_{GSSF}$ | $V_{GS}$=20V, $V_{DS}$=0V | | 100 | nA |
| $I_{GSSR}$ | $V_{GS}$=20V, $V_{DS}$=0V | | 100 | nA |
| $I_{DSS}$ | $V_{DS}$=50V, $V_{GS}$=0V | | 1.0 | μA |
| $I_{DSS}$ | $V_{DS}$=50V, $V_{GS}$=0V, $T_j$=125°C | | 500 | μA |
| $I_{D(ON)}$ | $V_{GS}$=10V, $V_{DS}$=10V | 500 | | mA |
| $BV_{DSS}$ | $V_{GS}$=0V, $I_D$=10μA | 50 | | V |

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0 mm²
(2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0 mm²
(3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4 mm²

R0 (24-January 2006)

**Central™**
**Semiconductor Corp.**

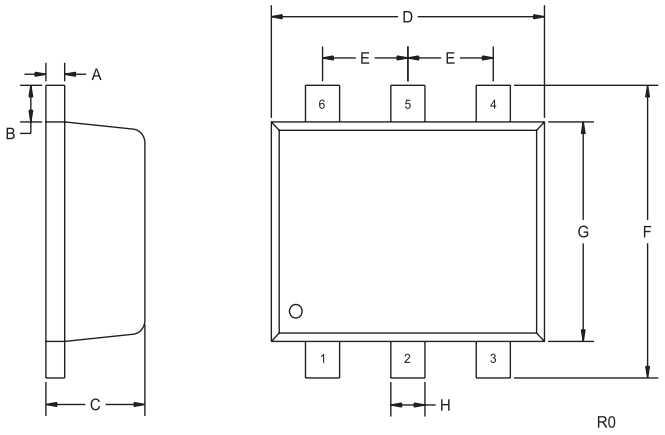
**CMLDM8002A**
**CMLDM8002AJ**

**SURFACE MOUNT PICOmini™**
**DUAL P-CHANNEL**
**ENHANCEMENT-MODE**
**SILICON MOSFET**

**ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued** ($T_A$=25°C unless otherwise noted)

| SYMBOL | TEST CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|
| $V_{GS(th)}$ | $V_{DS}$=$V_{GS}$, $I_D$=250μA | 1.0 | 2.5 | V |
| $V_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=500mA | | 1.5 | V |
| $V_{DS(ON)}$ | $V_{GS}$=5.0V, $I_D$=50mA | | 0.15 | V |
| $r_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=500mA | | 2.5 | Ω |
| $r_{DS(ON)}$ | $V_{GS}$=10V, $I_D$=500mA, $T_j$=125°C | | 4.0 | Ω |
| $r_{DS(ON)}$ | $V_{GS}$=5.0V, $I_D$=50mA | | 3.0 | Ω |
| $r_{DS(ON)}$ | $V_{GS}$=5.0V, $I_D$=50mA, $T_j$=125°C | | 5.0 | Ω |
| $Y_{fs}$ | $V_{DS}$ =10V, $I_D$=200mA | 200 | | msec |
| $C_{rss}$ | $V_{DS}$=25V, $V_{GS}$=0, f=1.0MHz | | 7.0 | pF |
| $C_{iss}$ | $V_{DS}$=25V, $V_{GS}$=0, f=1.0MHz | | 70 | pF |
| $C_{oss}$ | $V_{DS}$=25V, $V_{GS}$=0, f=1.0MHz | | 15 | pF |
| $t_{on}$ | $V_{DD}$=30V, $V_{GS}$=10V, $I_D$=200mA, | | 20 | ns |
| $t_{off}$ | $R_G$=25Ω, $R_L$=150Ω | | 20 | ns |
| $V_{SD}$ | $V_{GS}$=0V, $I_S$=115mA | | 1.3 | V |

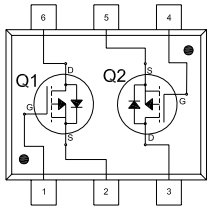
**SOT-563 CASE - MECHANICAL OUTLINE**




| DIMENSIONS | | | | |
|---|---|---|---|---|
| | INCHES | | MILLIMETERS | |
| SYMBOL | MIN | MAX | MIN | MAX |
| A | 0.004 | 0.007 | 0.10 | 0.18 |
| B | 0.008 | | 0.20 | |
| C | 0.022 | 0.024 | 0.56 | 0.60 |
| D | 0.059 | 0.067 | 1.50 | 1.70 |
| E | 0.020 | | 0.50 | |
| F | 0.061 | 0.067 | 1.55 | 1.70 |
| G | 0.047 | | 1.20 | |
| H | 0.006 | 0.012 | 0.15 | 0.30 |

SOT-563 (REV: R0)

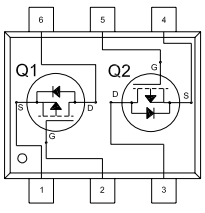
**CMLDM8002A** (USA Pinout)




**LEAD CODE:**
1) GATE Q1
2) SOURCE Q1
3) DRAIN Q2
4) GATE Q2
5) SOURCE Q2
6) DRAIN Q1

**MARKING CODE: C08**

**CMLDM8002AJ** (Japanese Pinout)




**LEAD CODE:**
1) SOURCE Q1
2) GATE Q1
3) DRAIN Q2
4) SOURCE Q2
5) GATE Q2
6) DRAIN Q1

**MARKING CODE: CJ8**

R0 (24-January 2006)