ANALOGIC TECH™

# AAT8543
## 20V P-Channel Power MOSFET

## General Description

The AAT8543 is a low threshold P-channel MOSFET designed for the battery, cell phone, and PDA markets. Using AnalogicTech's ultra-high-density MOSFET process and space-saving, small-outline, J-lead package, performance superior to that normally found in a TSOP-6 footprint has been squeezed into the footprint of an SC70JW-8 package.

## Applications

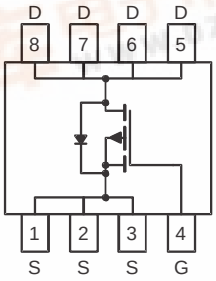
- Battery Packs
- Battery-Powered Portable Equipment
- Cellular and Cordless Telephones

## Features

- Drain-Source Voltage (max): -20V
- Continuous Drain Current[1] (max): -4.2A @ 25°C
- Low On-Resistance:
  - — 57mΩ @ $V_{GS}$ = -4.5V
  - — 104mΩ @ $V_{GS}$ = -2.5V

## SC70JW-8 Package

Top View




## Absolute Maximum Ratings

$T_A$ = 25°C, unless otherwise noted.

| Symbol | Description | | Value | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain-Source Voltage | | -20 | V |
| $V_{GS}$ | Gate-Source Voltage | | ±12 | |
| $I_D$ | Continuous Drain Current @ $T_J$ = 150°C[1] | $T_A$ = 25°C | ±4.2 | A |
| | | $T_A$ = 70°C | ±3.3 | |
| $I_{DM}$ | Pulsed Drain Current[2] | | ±20 | |
| $I_S$ | Continuous Source Current (Source-Drain Diode)[1] | | -1.2 | |
| $T_J$ | Operating Junction Temperature Range | | -55 to 150 | °C |
| $T_{STG}$ | Storage Temperature Range | | -55 to 150 | °C |

## Thermal Characteristics[1]

| Symbol | Description | | Typ | Max | Units |
|---|---|---|---|---|---|
| $R_{\theta JA}$ | Typical Junction-to-Ambient Steady State | | 100 | 124 | °C/W |
| $R_{\theta JA2}$ | Maximum Junction-to-Ambient t<5 Seconds | | 62 | 76 | °C/W |
| $R_{\theta JF}$ | Typical Junction-to-Foot | | 35 | 42 | °C/W |
| $P_D$ | Maximum Power Dissipation | $T_A$ = 25°C | | 1.6 | W |
| | | $T_A$ = 70°C | | 1.0 | |

1. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF} + R_{\theta FA} = R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.
2. Pulse test: Pulse Width = 300µs.

## Electrical Characteristics

$T_J$ = 25°C, unless otherwise noted.

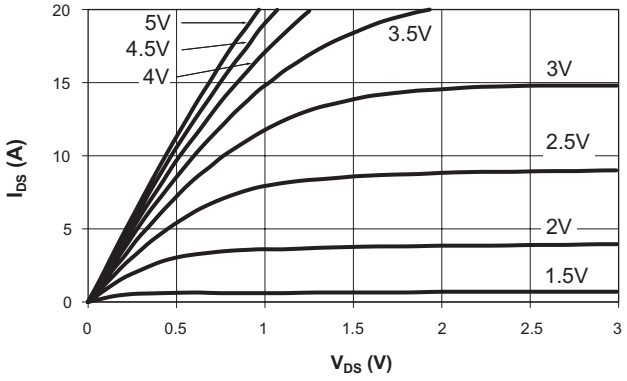
| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **DC Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$ = 0V, $I_D$ = -250µA | -20 | | | V |
| $R_{DS(ON)}$ | Drain-Source On-Resistance[1] | $V_{GS}$ = -4.5V, $I_D$ = -4.2A | | 45 | 57 | mΩ |
| | | $V_{GS}$ = -2.5V, $I_D$ = -3.1A | | 80 | 104 | |
| $I_{D(ON)}$ | On-State Drain Current[1] | $V_{GS}$ = -4.5V, $V_{DS}$ = -5V (pulsed) | -20 | | | A |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = -250µA | -0.6 | | | V |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$ = ±12V, $V_{DS}$ = 0V | | | ±100 | nA |
| $I_{DSS}$ | Drain Source Leakage Current | $V_{GS}$ = 0V, $V_{DS}$ = -20V | | | -1 | µA |
| | | $V_{GS}$ = 0V, $V_{DS}$ = -16V, $T_J$ = 70°C[2] | | | -5 | |
| $g_{fs}$ | Forward Transconductance[1] | $V_{DS}$ = -5V, $I_D$ = -4.2A | | 7 | | S |
| **Dynamic Characteristics[2]** | | | | | | |
| $Q_G$ | Total Gate Charge | $V_{DS}$ = -10V, $R_D$ = 2.4Ω, $V_{GS}$ = -4.5V | | 8.5 | | nC |
| $Q_{GS}$ | Gate-Source Charge | $V_{DS}$ = -10V, $R_D$ = 2.4Ω, $V_{GS}$ = -4.5V | | 1.5 | | |
| $Q_{GD}$ | Gate-Drain Charge | $V_{DS}$ = -10V, $R_D$ = 2.4Ω, $V_{GS}$ = -4.5V | | 2.8 | | |
| $t_{D(ON)}$ | Turn-On Delay | $V_{DS}$ = -10V, $R_D$ = 2.4Ω, $V_{GS}$ = -4.5V, $R_G$ = 6Ω | | 10 | | ns |
| $t_R$ | Turn-On Rise Time | $V_{DS}$ = -10V, $R_D$ = 2.4Ω, $V_{GS}$ = -4.5V, $R_G$ = 6Ω | | 32 | | |
| $t_{D(OFF)}$ | Turn-Off Delay | $V_{DS}$ = -10V, $R_D$ = 2.4Ω, $V_{GS}$ = -4.5V, $R_G$ = 6Ω | | 61 | | |
| $t_F$ | Turn-Off Fall Time | $V_{DS}$ = -10V, $R_D$ = 2.4Ω, $V_{GS}$ = -4.5V, $R_G$ = 6Ω | | 38 | | |
| **Source-Drain Diode Characteristics** | | | | | | |
| $V_{SD}$ | Source-Drain Forward Voltage[1] | $V_{GS}$ = 0, $I_S$ = -4.2A | | | -1.3 | V |
| $I_S$ | Continuous Diode Current[3] | | | | -1.2 | A |

1. Pulse test: Pulse Width = 300µs.
2. Guaranteed by design. Not subject to production testing.
3. Based on thermal dissipation from junction to ambient while mounted on a 1" x 1" PCB with optimized layout. A 5-second pulse on a 1" x 1" PCB approximates testing a device mounted on a large multi-layer PCB as in most applications. $R_{\theta JF}$ + $R_{\theta FA}$ = $R_{\theta JA}$ where the foot thermal reference is defined as the normal solder mounting surface of the device's leads. $R_{\theta JF}$ is guaranteed by design; however, $R_{\theta CA}$ is determined by the PCB design. Actual maximum continuous current is limited by the application's design.

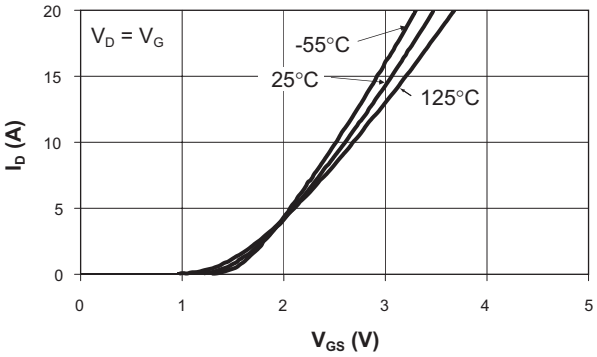
## Typical Characteristics

$T_J$ = 25ºC, unless otherwise noted.

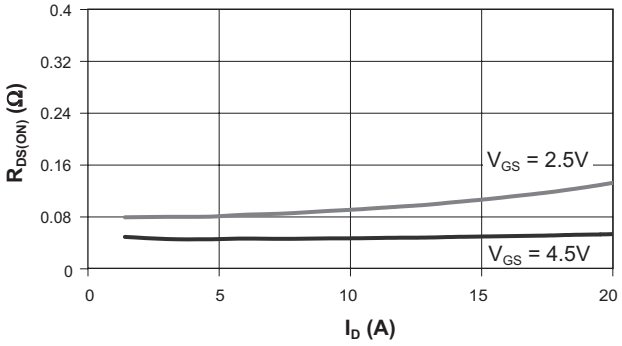
### Output Characteristics



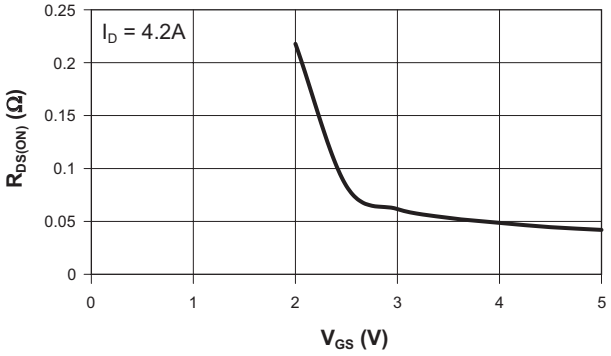

### Transfer Characteristics



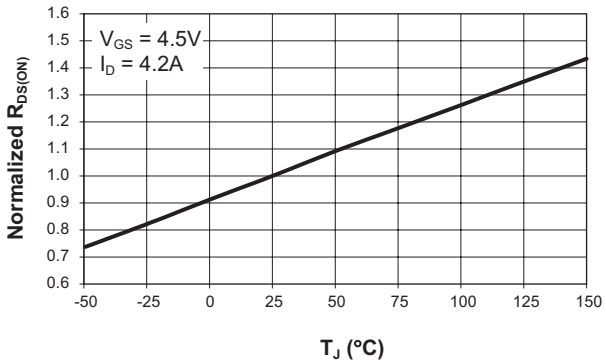

### On-Resistance vs. Drain Current



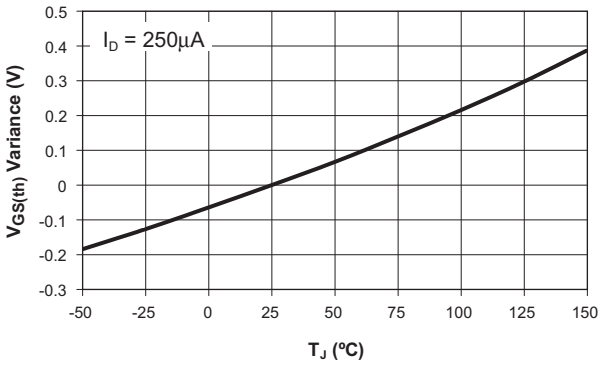

### On-Resistance vs. Gate-to-Source Voltage




### On-Resistance vs. Junction Temperature



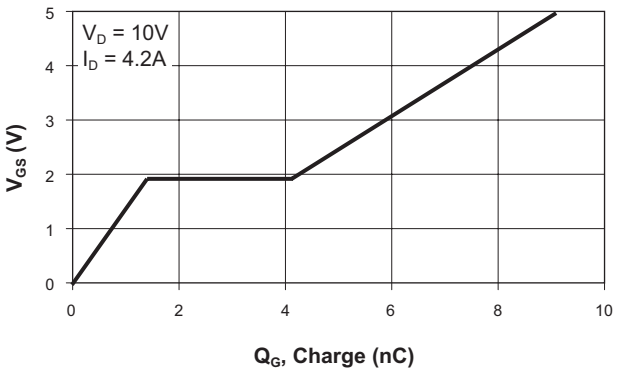

### Threshold Voltage



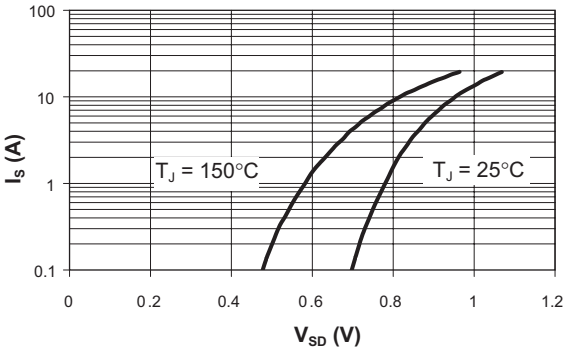
## Typical Characteristics

$T_J$ = 25ºC, unless otherwise noted.

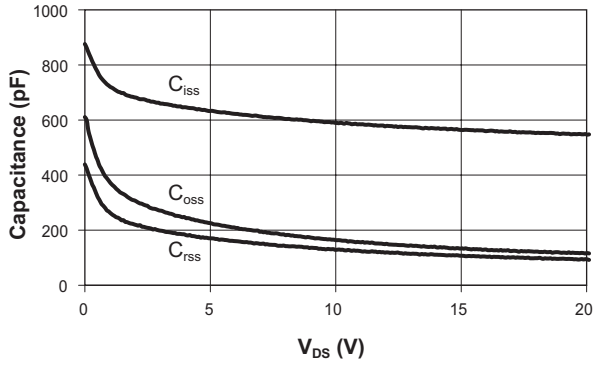
### Gate Charge



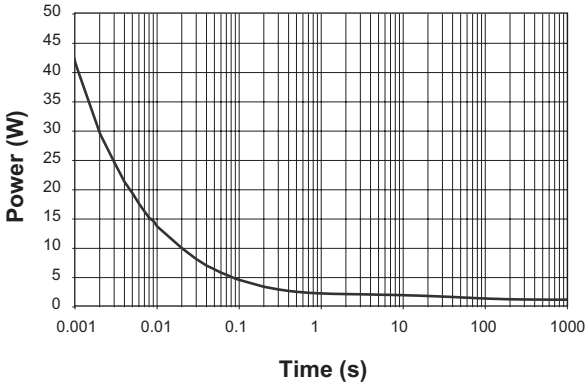

### Source-Drain Diode Forward Voltage



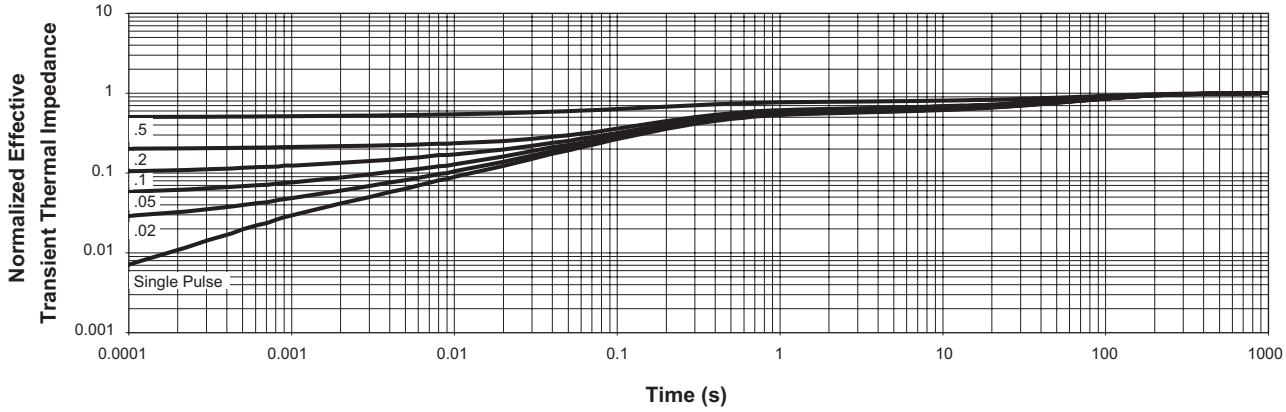

### Capacitance




### Single Pulse Power, Junction to Ambient




### Transient Thermal Response, Junction to Ambient

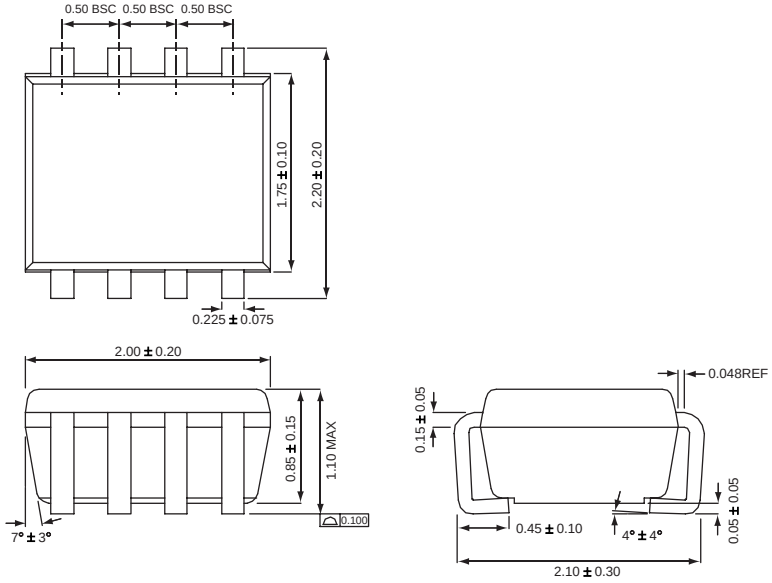


## Ordering Information

| Package | Marking[1] | Part Number (Tape and Reel)[2] |
|---|---|---|
| SC70JW-8 | JTXYY | **AAT8543IJS-T1** |

## Package Information

**SC70JW-8**




All dimensions in millimeters.

1. XYY = assembly and date code.
2. Sample stock is generally held on part numbers listed in **BOLD**.

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