SKYWORKS®

DATA SHEET

AA109-310, AA109-310LF: GaAs IC 5-Bit Digital Attenuator With Serial-to-Parallel Driver 0.5–2.5 GHz

Features

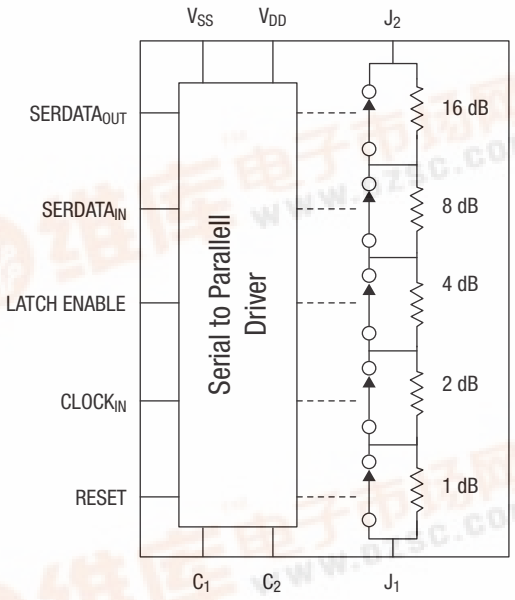
- Positive voltage operation (5 V)
- QFN 5 x 5 mm leadless package
- Integrated silicon serial-to-parallel driver
- Attenuation 1 dB steps to 31 dB
- Available lead (Pb)-free and RoHS-compliant MSL-1 @ 260 °C per JEDEC J-STD-020

Description

The AA109-310 is a GaAs FET IC 5-bit digital attenuator with a serial-to-parallel driver packaged in a 32-leadless exposed pad plastic package. It is particularly suited where high attenuation accuracy, low insertion loss, and low intermodulation products are required. Typical applications include base station, wireless and wireless local loop gain control circuits.

NEW Skyworks offers lead (Pb)-free, RoHS (Restriction of Hazardous Substances)-compliant packaging.

Simplified Schematic



Electrical Specifications at 25 °C

V_{DD} = 5 V, Z_0 = 50 Ω, unless otherwise specified

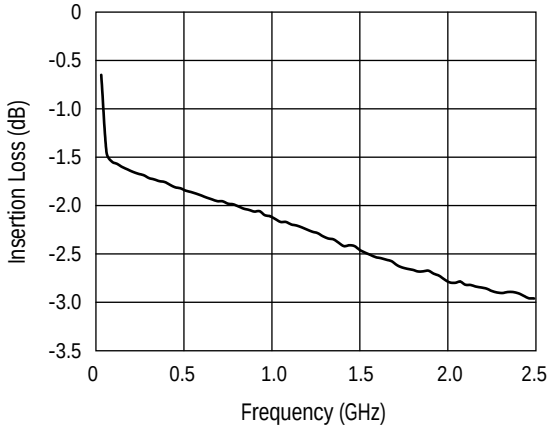
Parameter	Condition	Frequency	Min.	Typ.	Max.	Unit
Insertion loss		0.5–1.0 GHz 1.0–2.0 GHz 2.0–2.5 GHz		2.0 2.7 3.1	2.4 3.1 3.6	dB dB dB
Attenuation range[1, 2]				31		dB
Attenuation accuracy[1, 2]		0.5–1.0 GHz 1.0–2.0 GHz 2.0–2.5 GHz		± (0.2 + 3% of attenuation setting in dB) ± (0.3 + 5% of attenuation setting in dB) ± (0.3 + 6% of attenuation setting in dB)		dB dB dB
VSWR (I/O)		0.5–2.5 GHz		1.5:1	2.2:1	
Switching characteristics Rise, fall On, off Video feedthru	 10/90% or 90/10% RF 50% CTL to 90/10% RF T_{RISE} = 1 ns, BW = 500 MHz			 100 300 70		 µs µs mV
Input power for 1 dB compression	V_S = 3 V V_S = 5 V	0.9–2.5 GHz 0.9–2.5 GHz		21 27		dBm dBm
Intermodulation intercept point (IP3)	For two-tone input power +5 dBm V_S = 3 V V_S = 5 V	 0.9–2.5 GHz 0.9–2.5 GHz		 41 45		 dBm dBm

1. Attenuation value referenced above insertion loss.
2. Exposed pad must be connected to RF ground to obtain specified attenuation.

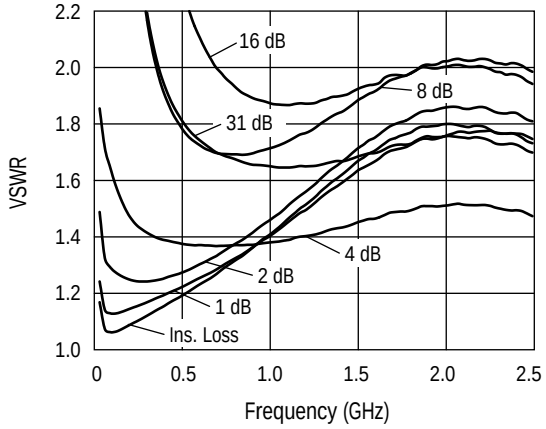
DC Electrical Characteristics at 25 °C (V_{DD} = 5 V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Input voltage high	V_{IH} (1)		3.5	5	V
Input voltage low	V_{IL} (0)	0	0.5		V
Input leakage current	I_L		±0.5		µA
Quiescent current	I_{DD}		500		µA
Supply voltages	V_{DD}		5		V

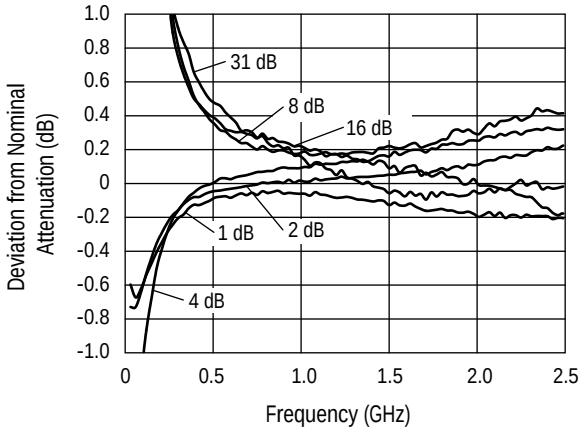
Typical Performance Data (V_{DD} = 5 V, Z_0 = 50 Ω)



Insertion Loss vs. Frequency



VSWR vs. Frequency



Attenuation Accuracy vs. Frequency

Absolute Maximum Ratings

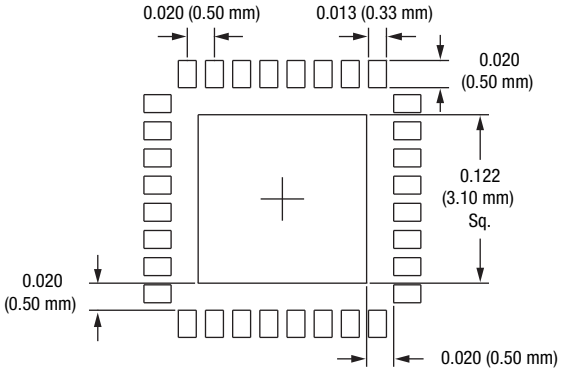
Characteristic	Value
Supply voltage (V_{DD})	-0.5 to +6 V
Input voltage (V_I)	-0.5 – Vcc + 0.5 V
Power dissipation (P_D)	500 mW
Storage temperature (T_{ST})	-65 °C to +150 °C
Operating temperature (T_{OP})	-40 °C to +85 °C

Performance is guaranteed only under the conditions listed in the specifications table and is not guaranteed under the full range(s) described by the Absolute Maximum specifications. Exceeding any of the absolute maximum/minimum specifications may result in permanent damage to the device and will void the warranty.

CAUTION: *Although this device is designed to be as robust as possible, ESD (Electrostatic Discharge) can damage this device. This device must be protected at all times from ESD. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD precautions must be employed at all times.*

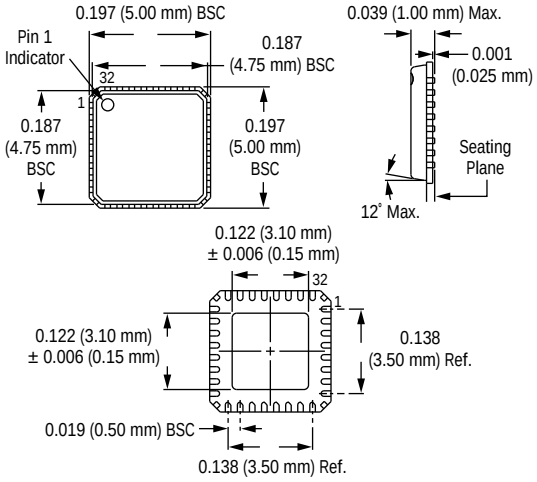
Surface Mount Land Pattern

5 x 5 mm QFN 32-Lead



Dimensions in inches (mm).

QFN 5 x 5 (-310)



Recommended Solder Reflow Profiles

Refer to the *"Recommended Solder Reflow Profile"* Application Note.

Tape and Reel Information

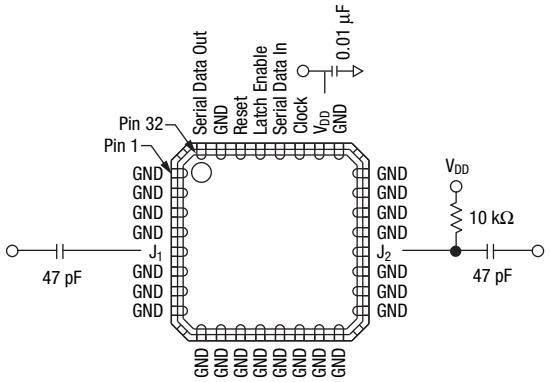
Refer to the *"Discrete Devices and IC Switch/Attenuators Tape and Reel Package Orientation"* Application Note.

Truth Table

Reset	Serial Data Input					J_1–J_2 Attenuation
	1 dB	2 dB	4 dB	8 dB	16 dB	
1	1	1	1	1	1	Insertion Loss
1	0	1	1	1	1	1 dB
1	1	0	1	1	1	2 dB
1	1	1	0	1	1	4 dB
1	1	1	1	0	1	8 dB
1	1	1	1	1	0	16 dB
1	0	0	0	0	0	31 dB
0	X	X	X	X	X	31 dB

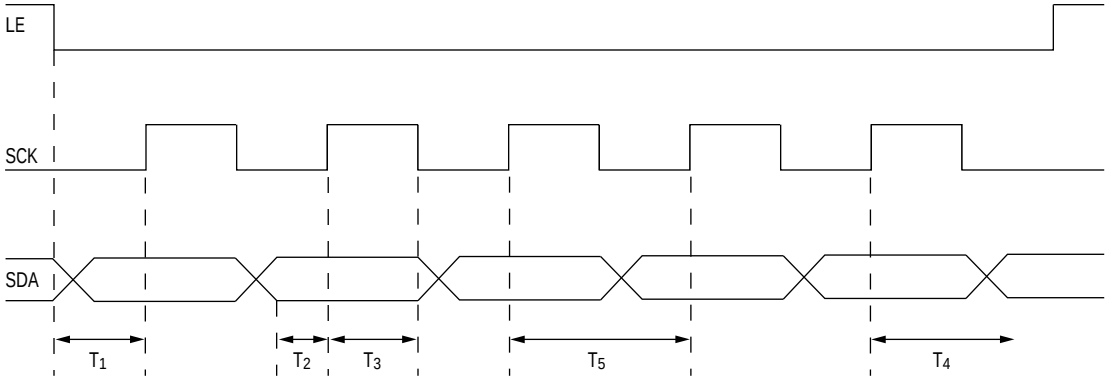
V_{IL} (0) = 0 to 0.5 V.
V_{IH} (1) = 3.5 to 5 V.
X = Don't Care.

Pin Out



Pin	Symbol	Function
1–4	GND	Ground
5	J_1	RF input/output
6–19	GND	Ground
20	J_2	RF input/output
21–25	GND	Ground
26	V_{DD}	Supply voltage
27	Clock In	Serial clock input
28	Serial data in	Serial data input
29	LE	Latch enable
30	Reset	Reset
31	GND	Ground
32	Serial data out	Serial data output

Timing Diagram



Parameter	Symbol	Min.	Typ.	Max.	Unit
LE setup time	T_1	5	15		ns
SDA setup time	T_2	5	15		ns
SDA hold time	T_3	5	10		ns
LE hold time	T_4	5	10		ns
Clock frequency	f_{CLK}		16	100	MHz
Clock period	T_5		$1/f_{CLK}$		

Serial data (SDA) is shifted into the register on the rising edge of the clock (SCK), most significant bit (MSB) first. The attenuator will change states on the rising edge of the latch enable (LE) signal, according to the most recent 5 bits of shifted data accepted since the previous falling edge of the LE signal.

Power-up sequence:
0. Connect ground
1. Apply VDD
2. Set all inputs (SCK, SDA, LE)

Power-down sequence should be the reverse of above.