捷多邦,专业PCB打样工厂**SN54A0533**,SN74AC533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

SCAS555C - NOVEMBER 1995 - REVISED OCTOBER 2003

- 2-V to 6-V V_{CC} Operation
- Inputs Accept Voltages to 6 V
- Max t_{pd} of 10.5 ns at 5 V
- 3-State Inverting Outputs Drive Bus Lines Directly
- Full Parallel Access for Loading

description/ordering information

The 'AC533 devices are octal transparent D-type latches with 3-state outputs. When the latch-enable (LE) input is high, the $\overline{\mathbb{Q}}$ outputs follow the complements of the data (D) inputs. When LE is taken low, the $\overline{\mathbb{Q}}$ outputs are latched at the inverse logic levels set up at the D inputs.

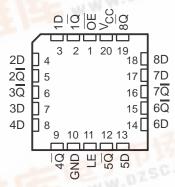
A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

OE does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

SN54AC533 . . . J OR W PACKAGE SN74AC533 . . . DB, DW, N, NS, OR PW PACKAGE (TOP VIEW)



SN54AC533 . . . FK PACKAGE (TOP VIEW)



To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

ORDERING INFORMATION

TA	PACKAGE	<u>=</u> †	ORDERABLE PART NUMBER	TOP-SIDE MARKING
	PDIP – N	Tube	SN74AC533N	SN74AC533N
	0010 PW	Tube	SN74AC533DW	40500
-40°C to 85°C	SOIC - DW	Tape and reel	SN74AC533DWR	AC533
	SOP - NS	Tape and reel	SN74AC533NSR	AC533
	SSOP - DB	Tape and reel	SN74AC533DBR	AC533
	TOOOD DW	Tube	SN74AC533PW	40500
100	TSSOP – PW	Tape and reel	SN74AC533PWR	AC533
_a (B)	CDIP – J	Tube	SNJ54AC533J	SNJ54AC533J
–55°C to 125°C	CFP – W	Tube	SNJ54AC533W	SNJ54AC533W
	LCCC - FK	Tube	SNJ54AC533FK	SNJ54AC533FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

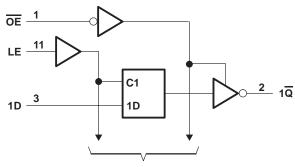


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FUNCTION TABLE (each latch)

	INPUTS		OUTPUT
OE	LE	D	Q
L	Н	Н	L
L	Н	L	Н
L	L	Χ	\overline{Q}_0
Н	X	Χ	Z

logic diagram (positive logic)



To Seven Other Channels

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}		–0.5 V to 7 V
Input voltage range, V _I (see Note 1)		$1.000 - 0.5 \text{ V}$ to $V_{CC} + 0.5 \text{ V}$
Output voltage range, VO (see Note 1)		$1.000 - 0.5 \text{ V}$ to $V_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$).		±20 mA
Output clamp current, IOK (VO < 0 or VO > VCO	C)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})		±50 mA
Continuous current through V _{CC} or GND		±200 mA
Package thermal impedance, θ _{JA} (see Note 2):	: DB package	70°C/W
	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
	PW package	83°C/W
Storage temperature range, T _{stg}		–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54 <i>A</i>	C533	SN74A	C533	
			MIN	MAX	MIN	MAX	UNIT
VCC	Supply voltage		2	6	2	6	V
		V _{CC} = 3 V	2.1		2.1		
٧ıн	High-level input voltage	$V_{CC} = 4.5 \text{ V}$	3.15		3.15		V
		V _{CC} = 5.5 V	3.85		3.85		
		VCC = 3 V		0.9		0.9	
V _{IL}	Low-level input voltage	V _{CC} = 4.5 V		1.35		1.35	V
		V _{CC} = 5.5 V		1.65		1.65	
VI	Input voltage		0	Vcc	0	VCC	V
VO	Output voltage		0	VCC	0	VCC	V
		VCC = 3 V	200	-12		-12	
lOH	High-level output current	V _{CC} = 4.5 V	Q.	-24		-24	mA
		V _{CC} = 5.5 V		-24		-24	
		V _{CC} = 3 V		12		12	
lOL	Low-level output current	$V_{CC} = 4.5 \text{ V}$		24		24	mA
		V _{CC} = 5.5 V		24		24	
Δt/Δν	Input transition rise or fall rate			8		8	ns/V
TA	Operating free-air temperature		-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

24244555	TEGT GOLDITIONS	\ ,,	T,	գ = 25°C	SN54	AC533	SN74A	C533		
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP MA	K MIN	MAX	MIN	MAX	UNIT	
		3 V	2.9		2.9		2.9			
	I _{OH} = -50 μA	4.5 V	4.4		4.4		4.4			
		5.5 V	5.4		5.4		5.4		V	
VOH	I _{OH} = -12 mA	3 V	2.56		2.4	3	2.46		V	
	1	4.5 V	3.86		3.7	N.	3.76			
	$I_{OH} = -24 \text{ mA}$	5.5 V	4.86		4.7	77	4.76			
		3 V		0.	1 4	0.1		0.1		
	I _{OL} = 50 μA	4.5 V		0.	1 2	0.1		0.1	v	
.,		5.5 V		0.	1 0	0.1		0.1		
VOL	I _{OL} = 12 mA	3 V		0.3	6	0.5		0.44	V	
	24 = 4	4.5 V		0.3	6	0.5		0.44		
	$I_{OL} = 24 \text{ mA}$	5.5 V		0.3	6	0.5		0.44		
loz	$V_O = V_{CC}$ or GND	5.5 V		±0.2	5	±5		±2.5	μΑ	
lį	$V_I = V_{CC}$ or GND	5.5 V		±0.	1	±1		±1	μΑ	
lcc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4	80		40	μΑ	
C _i	V _I = V _{CC} or GND	5 V		4.5					pF	



SN54AC533, SN74AC533 OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

			T _A = 25°C		SN54AC533		SN74AC533	
		MIN	MAX	MIN	MAX	MIN	MAX	UNIT
t _W	Pulse duration, LE high	6		8	El P	6.5		ns
t _{su}	Setup time, data before LE↓	5.5		7.5		6		ns
th	Hold time, data after LE↓	1.5		2.5	C	1		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			25°C	SN54AC533	SN74AC533		LINUT
		MIN	MAX	MIN MAX	MIN	MAX	UNIT
t _W	Pulse duration, LE high	4.5		6.55	5		ns
t _{su}	Setup time, data before LE↓	4		74	4.5		ns
t _h	Hold time, data after LE↓	1.5		2.50	1		ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	T _A = 25°C		SN54A	C533	SN74AC533		UNIT
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNII
t _{PLH}	D	Ια	2	14	1	17.5	1.5	16	20
^t PHL	U	α	2	13	1	16	1.5	14.5	ns
^t PLH	- [Ια	2	14.5	1	18	1.5	16.5	
^t PHL	LE	Q	2	13	1,	16	1.5	14.5	ns
^t PZH	<u>ol</u>	ρl	2	12.5	377	15.5	1.5	14	
t _{PZL}	OE	α	2	12.5	91	15.5	1.5	14	ns
^t PHZ	ŌĒ	ā	2	13	y 1	16	1.5	14.5	20
t _{PLZ}	OE	ά	2	13	1	16	1.5	14.5	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	T _A = 25°C		SN54A	C533	SN74A	C533	
PARAMETER	(INPUT)	(OUTPUT)	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
^t PLH	6	Ια	2	10	1	12.5	1.5	11	
^t PHL	D	α	2	9.5	1	12	1.5	10.5	ns
^t PLH		Ια	2	10.5	1	13	1.5	11.5	
t _{PHL}	LE	α	2	10	1,0	13	1.5 11		ns
^t PZH	OE	Ια	2	9.5	(b)	12	1.5	10.5	
t _{PZL}	OE .	α	2	9.5	Q1	12	1.5	10.5	ns
t _{PHZ}	ŌĒ	Īα	2	10	3 1	12.5	1.5	11	20
^t PLZ	OE	ά	2	10	1	12.5	1.5	11	ns

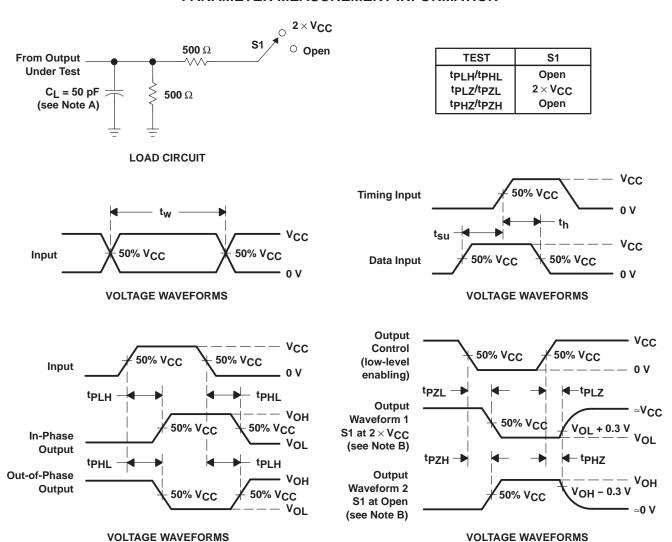
operating characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

	PARAMETER	TEST C	TYP	UNIT	
C _{pd}	Power dissipation capacitance	$C_L = 50 \text{ pF},$	f = 1 MHz	40	pF



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PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_f \leq$ 2.5 ns, $t_f \leq$ 2.5 ns.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms







m 4-Jun-2007

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AC533DBLE	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI
SN74AC533DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533DBRG4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533DWG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533DWRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AC533NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AC533NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533NSRG4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533PW	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533PWE4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533PWG4	ACTIVE	TSSOP	PW	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533PWLE	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI
SN74AC533PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AC533PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.



PACKAGE OPTION ADDENDUM

4-Jun-2007

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

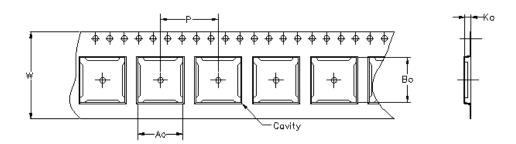
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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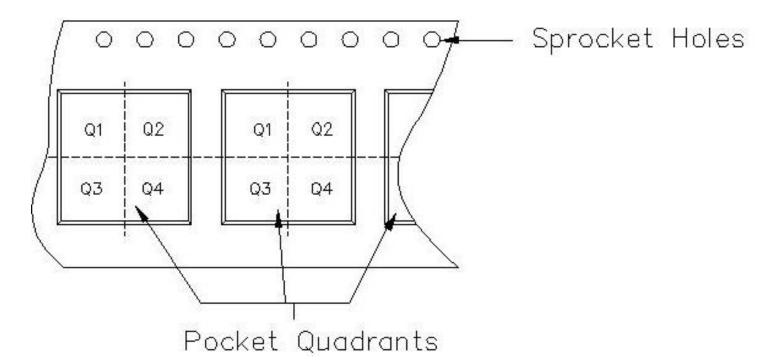
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Carrier tape design is defined largely by the component lentgh, width, and thickness.

				accommodate						
Bo =	Dimension	designed	to	accommodate	the	component	length.			
Ko =	Dimension	designed	to	accommodate	the	component	thickness.			
W = 1	W = Overall width of the carrier tape.									
P = F	P = Pitch between successive cavity centers.									



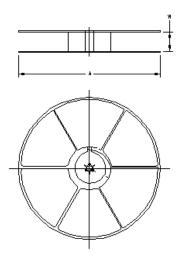
TAPE AND REEL INFORMATION



PACKAGE MATERIALS INFORMATION

19-May-2007

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AC533DBR	DB	20	MLA	330	16	8.2	7.5	2.5	12	16	Q1
SN74AC533DWR	DW	20	MLA	330	24	10.8	13.0	2.7	12	24	Q1
SN74AC533NSR	NS	20	MLA	330	24	8.2	13.0	2.5	12	24	Q1
SN74AC533PWR	PW	20	MLA	330	16	6.95	7.1	1.6	8	16	Q1



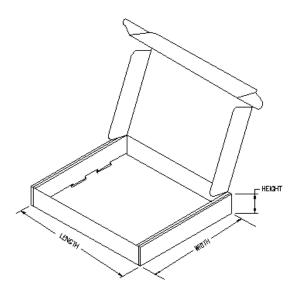
TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AC533DBR	DB	20	MLA	342.9	336.6	28.58
SN74AC533DWR	DW	20	MLA	333.2	333.2	31.75
SN74AC533NSR	NS	20	MLA	333.2	333.2	31.75
SN74AC533PWR	PW	20	MLA	342.9	336.6	28.58



PACKAGE MATERIALS INFORMATION

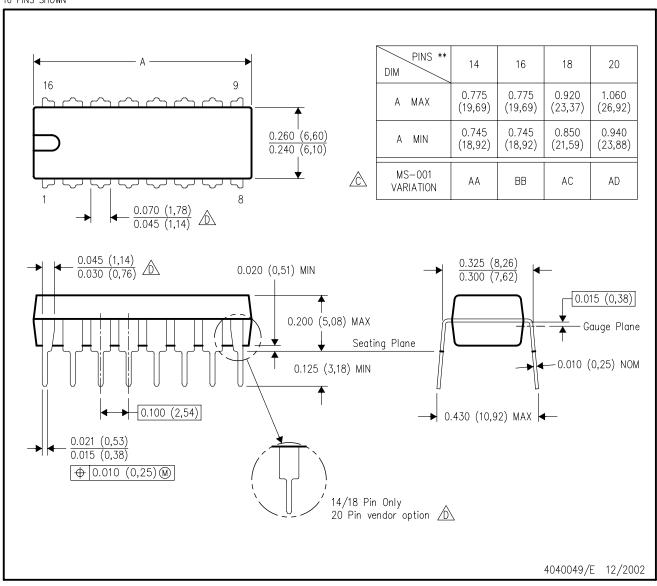
19-May-2007



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

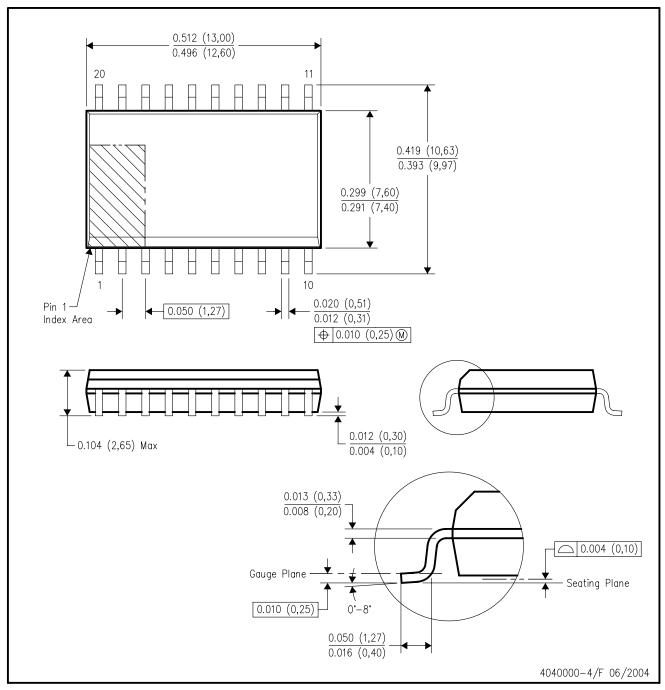


NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

DW (R-PDSO-G20)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

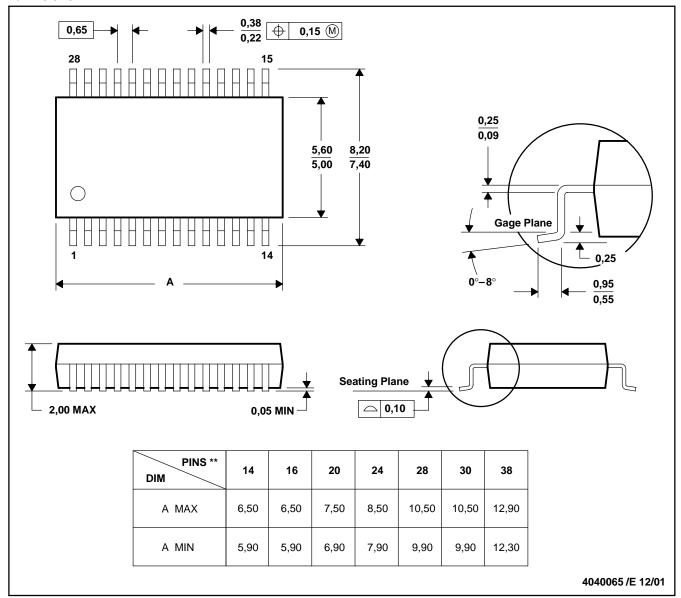
- . All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



PW (R-PDSO-G**)

14 PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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