ADC-800
15-Bit Plus Sign A/D Converter with Microprocessor Interface

DATEL

FEATURES

- 15-Bits Plus Sign Bit
- Parallel or Serial Bus Interface
- Three State Outputs
- High Impedance Differential Input
- UART Control Signals
- Low Noise

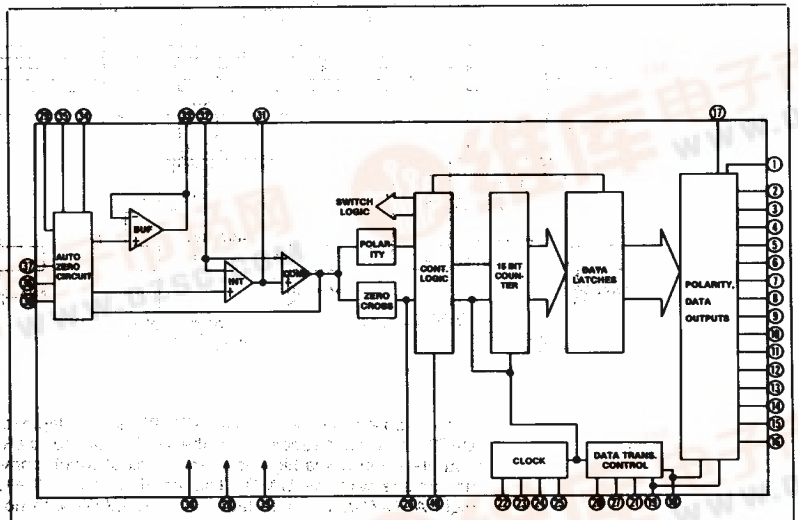
GENERAL DESCRIPTION

DATEL's ADC-800 is a low power, 15-bit plus sign integrating A/D converter. Microprocessor interface signals allow 16-bit, single byte or 8-bit, two byte parallel data transfer or data may be transmitted serially via industry standard UART in the "handshake" mode. Conversion time is typically 2.5 conv/sec with a maximum differential linearity error of ±½ LSB.

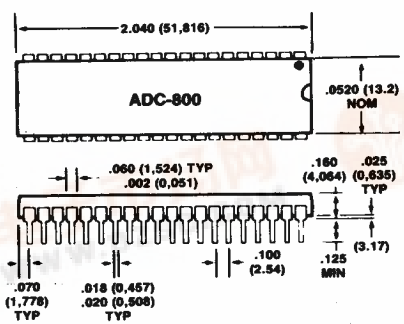
The ADC-800 uses an improved dual slope conversion technique which incorporates system zero and integrator output zero phases. Offset error sources are automatically zeroed. The externally adjustable clock allows integration periods which are integral multiples of 50 or 60 Hz for maximum power-line noise rejection. By using the 2.4576 MHz crystal oscillator mode, 50, 60 and 400 Hz signals are rejected. A serial count output can be derived by gating the clock signal with data valid (DVD). The count output pulses may be used in serial fiber optic transmission systems.

Other important features of the ADC-800 include: high impedance differential inputs, 5 pA typical input bias current, 15 μV peak-to-peak typical input noise, 20 mW power dissipation and static discharge protected inputs. the combination of low cost, high accuracy and low power consumption make the ADC-800 an ideal choice for process control, data logging and intelligent measurement system applications.

The ADC-800 operates over the commercial, 0°C to +70°C temperature range and is packaged in a 40-pin plastic DIP.



MECHANICAL DIMENSIONS INCHES (MM)



INPUT/OUTPUT CONNECTIONS

PIN	FUNCTION	PIN	FUNCTION
1	SGN	21	BUS/HAND
2	DB15 (MSB)	22	OSC IN
3	DB14	23	OSC OUT
4	DB13	24	OSC CON
5	DB12	25	BUF OSC
6	DB11	26	CONVERT/STOP
7	DB10	27	DRQST
8	DB9	28	$-V_S$
9	DB8	29	V_{REF}
10	DB7	30	COM
11	DB6	31	V_{INT}
12	DB5	32	C_{SZ}
13	DB4	33	V_{BUF}
14	DB3	34	$-C_R$
15	DB2	35	$+C_R$
16	DB1 (LSB)	36	$-V_{IN}$
17	TEST	37	$+V_{IN}$
18	LBEN/LBFLG	38	$+V_S$
19	HBEN/HBFLG	39	DIG GND
20	CE/LDSTRB	40	DVD

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ABSOLUTE MAXIMUM RATINGS	
Positive Supply Voltage ($+V_S$ to gnd)	+6.2V
Negative Supply Voltage ($-V_S$ to gnd)	−9.0V
Analog Input Voltage Range (+ or − Vin)	$+V_S$ to $-V_S$
Reference Input Voltage Range (Vref)	$+V_S$ to $-V_S$
Digital Input Voltage Range	$+V_S$ +0.3V to gnd −0.3V
Power Dissipation (package)	0.5W to 70°C

FUNCTIONAL SPECIFICATIONS

Typical at 25°C, ±5V supplies, 2.5 conv/sec. conversion speed, 2.4576 MHz crystal, 3.2768V full-scale voltage unless otherwise noted.

ANALOG INPUTS	
Type Analog Input	Differential
Zero-Scale Error, max.[1]	±0.5 LSB
Input Current,[2] max.	15 pA
Common Mode Input Range	$-V_S$ + 1.5V to $+V_S$ − 1.0V
Common Mode Rejection Ratio[3]	80 μV/V
Input Noise[4]	15 μV peak-to-peak

DIGITAL INPUTS	
Control Input Pull-Up Current[5]	5 μA
Input Voltage, (Pins 18-21, 26, 27)	
High Min.	2.5V
Low Max.	2V
Input Pull-up Current[6] (pins 26, 27)	5 μA
(pins 17, 24)	25 μA
Input Pin Pulldown Current[7] (pin 21)	5 μA
Input Capacitance, max. (pins 18, 19)	50 pF
BUS/Hand Control Pulse Width, min.[8]	70 nsec.
Byte Enable Pulse Width, min.[8]	350 nsec.
Chip Enable Pulse Width, min.[8]	500 nsec.
Byte Enable Access Time, max.[8]	350 nsec.
Chip Enable Access Time, max.[8]	400 nsec.
Data Hold from Byte Enable Change, max.[8]	300 nsec.
Data Hold from Chip Enable Change, max.[8]	400 nsec.

OUTPUTS	
Output Voltage, high min.	3.5V at 100 mA
low max.[9]	0.4V at 1.6 mA
Output Leakage Current (high Z state), max.	1 μA
Oscillator Output Current, (V_0 = 2.5V)	1 mA
Buffered Oscillator Output Current (V_0 = 2.5V)	5 mA

PERFORMANCE	
Resolution	15-bits plus sign
Linearity Error,[10] max.	2 LSB
Differential Linearity, max.	±0.5 LSB
Conversion Time	2.5 conv/sec. (400 msec.)
Full-Scale Gain Tempco[11] max.	5 ppm/°C
Zero-Scale Error Tempco, max.	2 μV/°C
Full-Scale Magnitude Symmetry Error, max.[12]	2 LSB

POWER REQUIREMENTS	
Supply Voltage	±5V
Supply Current, max.	±3.5 mA
typical	±2.0 mA

PHYSICAL/ENVIRONMENTAL	
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−55°C to +150°C
Lead Temperature (soldering 60 sec)	+300°C
Package	40-pin Plastic DIP

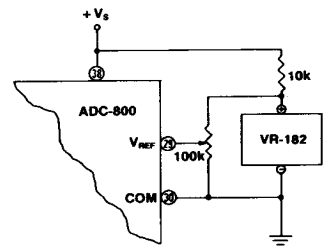
FOOTNOTES:

1. Vin = 0V
2. At 25°C, Vin = 0V. For 0°C to +70°C, Iin = 125 pA.
3. Vcm = ±1V.
4. Not exceeded 95% of the time.
5. Pin 18, 19, 20, 21 = 0V. Vout = 2V.
6. V = 2V.
7. V = 3V.
8. Parallel data transfer. ($\overline{BUS}$/Hand = 0)
9. For pins 18, 19, 20. Iout = 750 μA.
10. −F.S. ≤ Vin ≤ +F.S., best straight line. End point is typically 2.8 LSB.
11. External Reference Tempco = 0 ppm/°C 0°C ≤ T_A ≤ +70°C.
12. Vin = 3.27V.
13. Static sensitive device. Unused units must be stored in conductive material. Protect devices from static discharge and static fields.

TECHNICAL NOTES

1. The internal class A output stage amplifiers will supply a 20 μA drive current with minimal linearity error. R_{INT} is calculated for a 20 μA full-scale current using the following expression: R_{INT} (MΩ) = Full-Scale Input Voltage (V)/20.
2. The integrating capacitor should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.4V from either supply). With a 20 μA full-scale buffer output current, the integrating capacitor (C_{INT}) is calculated as follows: C_{INT} (μF) = 16.384 (1/F_{CLK} (kHz) (20 μA)/Integrator Output Voltage Swing (V). With an external 2.4576 MHz crystal, the clock frequency will be 163.8 kHz and conversion time is 2.5 CONV/SEC. A 0.47 μF C_{INT} is recommended with low dielectric absorption such as polypropylene to prevent roll-over errors. The outer foil of C_{INT} should be connected to Pin 31.
3. A 1.0 μF polypropylene capacitor is recommended for C_{SZ}. (System Zero Capacitor.) The inner foil should be connected to Pin 32.
4. For the reference capacitor, a 1.0 μF is recommended. Larger values may be used to limit roll-over errors. Low leakage capacitors, such as polypropylene should be used.
5. The analog input required to generate the 32,768 8 full-scale count is 2 V_{REF}. The reference voltage source should be selected for temperature stability. The ADC-800 will provide 30 ppm resolution. With a 5 ppm/°C reference, a 6° change in temperature will introduce a 1-bit absolute error. A stable reference must be used where ambient temperature is controlled and accurate absolute measurements are needed. The reference voltage input must be a positive voltage with respect to analog common. A reference circuit is shown below.
6. The R_S (delay resistor) in combination with C_{INT} compensate for comparator delay time. With a 0.47 μF C_{INT}, a 20Ω series resistor is recommended.

REFERENCE VOLTAGE CIRCUIT



PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	SGN	Sign Bit: Logic "1" indicates positive input. Input signal polarity is determined at the end of the signal integrate phase.
2	DB15 (MSB)	Data Bits. Three-State Outputs
3	DB14	
4	DB13	
5	DB12	
6	DB11	
7	DB10	
8	DB9	
9	DB8	
10	DB7	
11	DB6	
12	DB5	
13	DB4	
14	DB3	
15	DB2	
16	DB1 (LSB)	
17	TEST	Test: Logic "0" forces data bits to Logic "1" and disables clock. Logic "1" enables counter latches.
18	$\overline{\text{LBEN}}$/$\overline{\text{LBFLG}}$ (Input/Output)	Low data byte enable input or flag output depending on $\overline{\text{BUS}}$/HAND (Pin 21) status. With $\overline{\text{BUS}}$/HAND (Pin 21) low and $\overline{\text{CE}}$/$\overline{\text{LDSTRB}}$ (Pin 20) low, DB8 through DB1 (low data byte) are output, when input $\overline{\text{LBEN}}$ is low. With $\overline{\text{BUS}}$/HAND high, valid data (DB8-DB1) is indicated by the flag output $\overline{\text{LBFLG}}$ when low.
19	$\overline{\text{HBEN}}$/$\overline{\text{HBFLG}}$ (Input/Output)	High data byte enable input or flag output depending on $\overline{\text{BUS}}$/HAND (Pin 21) status. With $\overline{\text{BUS}}$/HAND (Pin 21) low and $\overline{\text{CE}}$/$\overline{\text{LDSTRB}}$ low, the sign bit and DB15-DB9 (high data byte) are output, when input $\overline{\text{HBEN}}$ is low. With $\overline{\text{BUS}}$/HAND (Pin 21) high, valid data (sign and DB15-DB9) is indicated by the flag output $\overline{\text{HBFLG}}$ when low.
20	$\overline{\text{CE}}$/$\overline{\text{LDSTRB}}$ (Input/Output)	With $\overline{\text{BUS}}$/HAND (Pin 21) low, $\overline{\text{CE}}$ (Pin 20) is the master CHIP ENABLE. When $\overline{\text{CE}}$ input is high, the sign bit and DB15-DB1 are in the high impedance state. With $\overline{\text{CE}}$ low, data is transferred under control of $\overline{\text{LBEN}}$ and $\overline{\text{HBEN}}$ input signals as follows: $\overline{\text{CE}}$ $\overline{\text{LBEN}}$ $\overline{\text{HBEN}}$ FUNCTION 0 0 1 Low data byte output 0 1 0 High data byte output 0 0 0 Low and high data byte output 0 1 1 High impedance state With $\overline{\text{BUS}}$/HAND high (Pin 21), $\overline{\text{LDSTRB}}$ Pin 20) is a load strobe output sign and a low output signal instructs the receiving device to accept data.

PIN	SYMBOL	DESCRIPTION
21	$\overline{\text{BUS}}$/HAND	Input low, yields parallel output data mode. The $\overline{\text{CE}}$, $\overline{\text{HBEN}}$ and $\overline{\text{LBEN}}$ (Pins 20, 19, 18) are inputs and directly control the 16 data bits. Input pulsed HIGH causes immediate entry into handshake data transfer mode for UART interfacing. $\overline{\text{LDSTRB}}$, $\overline{\text{LBFLG}}$ and $\overline{\text{HBFLG}}$ are TTL compatible outputs in this mode.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC CON	Selects internal oscillator structure. Input high: RC oscillator. Internal clock frequency is same frequency and duty cycle as BUF OSC (Pin 25). Input Low: Crystal oscillator. Internal clock frequency is frequency at BUS OSC ÷ 15.
25	BUF OSC	Buffered oscillator output
26	CONVERT/$\overline{\text{STOP}}$	Input high: Performs continuous conversion. Input low: Stops conversion process 7 counts before entering signal integrate phase. Conversion in progress is completed.
27	DRQST	Data output request signal. Input used in the handshake mode to indicate an external device is ready to accept data.
28	$-V_S$	Negative supply (−5V)
29	V_{REF}	Voltage reference input
30	COM	Analog common. The device is auto-zeroed to the analog common potential.
31	V_{INT}	Integrator output
32	C_{SZ}	System zero capacitor
33	V_{BUF}	Input signal buffer output
34	−CR	Negative reference capacitor connection
35	+CR	Positive reference capacitor connection
36	$-V_{IN}$	Negative differential analog input
37	$+V_{IN}$	Positive differential analog input
38	$+V_S$	Positive supply (+5V)
39	DIG GND	Ground return for all digital logic
40	$\overline{\text{DVD}}$	Data valid signal: high during signal integrate and reference integrate phases until data is latched. Low when in auto zero phase. Data does not change when $\overline{\text{DVD}}$ = 0

TIMING AND OPERATION

THE CONVERSION PROCESS

The conventional dual-slope converter measurement cycle has two distinct phases: Input signal Integration, and Reference Voltage Integration (deintegration).

The analog input signal is integrated for a fixed time period which is measured by counting clock pulses. An opposite polarity constant reference voltage is then integrated until the integrator output returns to zero. The reference voltage integration time is directly proportional to the input signal. A complete conversion requires the integrator output to "ramp-up" and "ramp-down".

The ADC-800's accuracy is unrelated to the integrating resistor and capacitor values as long as they are stable during a measurement cycle. An inherent advantage in the dual-slope converter is noise immunity. Noise spikes are integrated or averaged to zero during the integration periods.

The following equation relates the input signal, reference voltage and integration time:

$$\frac{1}{RC}\int_0^{T_{SI}} Vin(t)\,dt = \frac{V_R\,T_{RI}}{RC}$$

Where: V_R = Reference Voltage
T_{SI} = Signal Integration Time (fixed)
T_{RI} = Reference Voltage Integration Time (variable)

For a constant Vin: $Vin = V_R\left[\frac{T_{RI}}{T_{SI}}\right]$

ANALOG INPUT DESCRIPTION

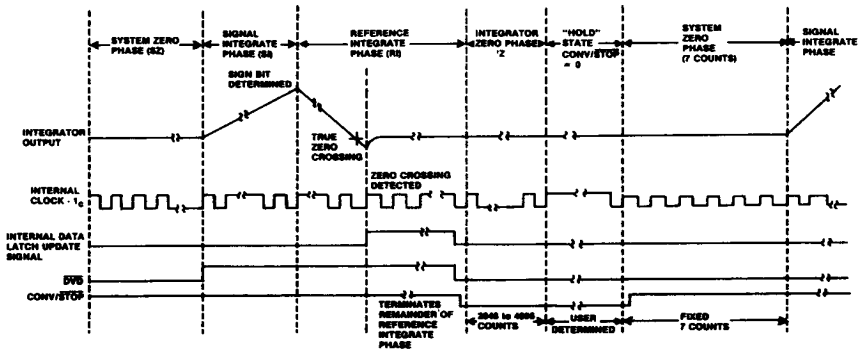
System Zero Phase: Errors due to buffer, integrator and comparator offset voltages are compensated for by charging C_{SZ} with a compensating error voltage.

Input Signal Integration Phase: The differential voltage between the inputs is integrated. The differential voltage must be within the specified common-mode range. The input signal is integrated for 16,384 clock cycles. The polarity is determined at the end of the phase.

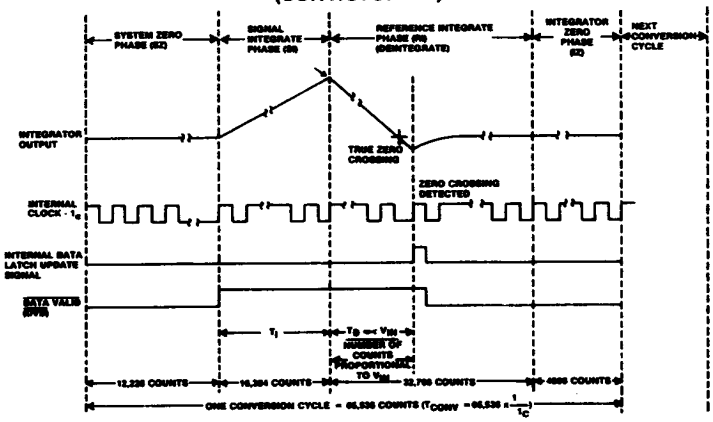
Reference Voltage Integration: C_R (Reference Capacitor), which was previously charged is connected with proper polarity to ramp the integrator output back to zero. The time for the output to return to zero is proportional to the input signal magnitude. This phase lasts for a maximum of 32,768 clock periods.

Integrator Output Zero: This phase guarantees the integrator output is at zero volts when the system zero phase is entered and that the true system offset voltages are compensated for. This phase lasts for 4096 clock cycles.

CONVERT ON COMMAND OPERATION
(CONV/$\overline{STOP}$ = 0 AFTER ZERO CROSSING IS DETECTED)



CONTINUOUS CONVERSION
(CONV/$\overline{STOP}$ = 1)



TIMING AND OPERATION (CONT.)

PARALLEL MODE DATA TRANSFER

With BUS/HAND at logic "0", the sign and data bits are controlled by the CE/LDSTRB (Pin 20), LBEN/LBFLG (Pin 18) and HBEN/HBFLG (Pin 19) inputs. These inputs include internal pull-up resistors. Inactive data bits are in the high impedance state.

The HBEN/HBFLG signal controls the most significant data byte (SGN, DB15-DB9) and LBEN/LBFLG (Pin 18) controls the least significant data byte (DB8-DB1). See adjacent TRUTH TABLE.

These input signals are asynchronous with the internal clock. Output data is immediately available. To avoid accessing data as it is updated, the DATA VALID (Pin 40) can be used to control data access. Data will not change if DVD = 0.

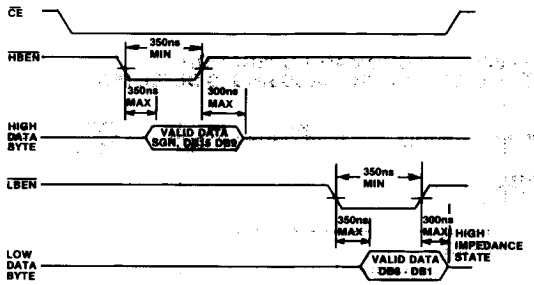
TRUTH TABLE

CE/LDSTRB (Pin 20)	HBEN/HBFLG (Pin 19)	LBEN/LBFLG (Pin 18)	HIGH DATA BYTE (SGN,DB15-DB9)	LOW DATA BYTE (DB8-DB1)
1	X	X	Inactive	Inactive
0	0	0	Active	Active
0	0	1	Active	Inactive
0	1	0	Inactive	Active
0	1	1	Inactive	Inactive

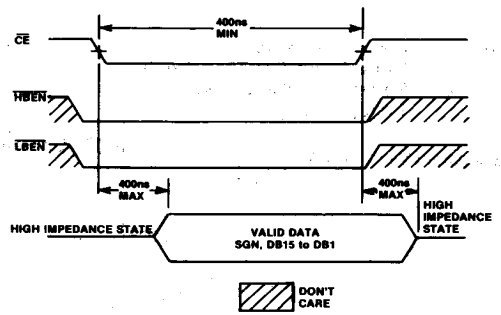
Inactive = High "Z" state
"X" = 1 or 0

PARALLEL DATA TRANSFER

TWO 8-BIT BYTES



SINGLE 16-BIT BYTE

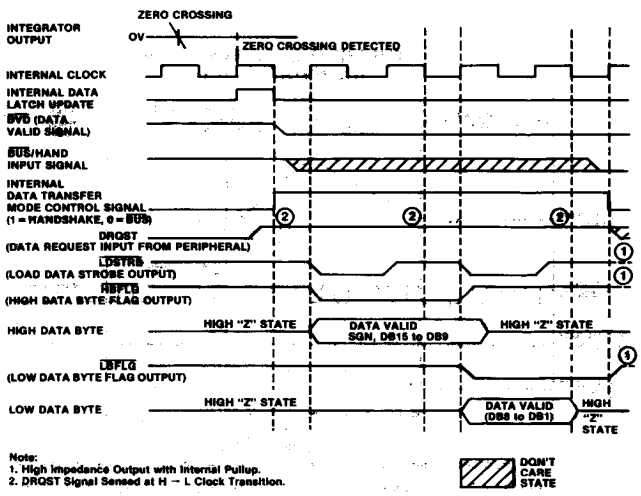


HANDSHAKE MODE DATA TRANSFER

The ADC-800 actively controls the data transfer to peripherals through the handshake data transfer mode. In this mode LBEN/LBFLG, HBEN/HBFLG and CE/LDSTRB (Pins 18, 19, 20) are TTL compatible outputs. The LDSTRB signal indicates valid data is available for the peripheral. The LBFLG and HBFLG signals indicate which data byte is being transferred. DRQST (Pin 27) informs the A/D that a peripheral is ready to accept data. A complete cycle transfers two 8-bit bytes.

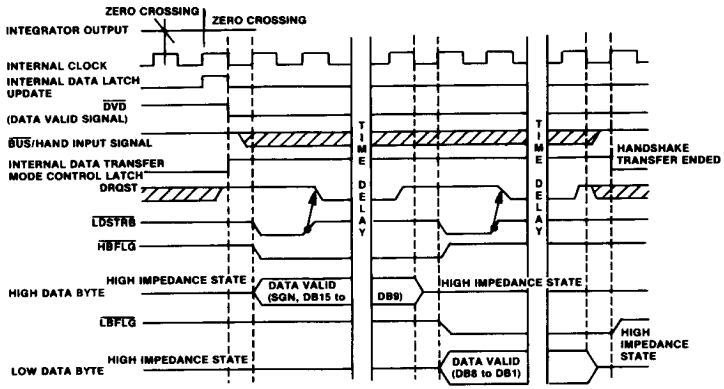
A logic "1" on BUS/HAND (Pin 21) enters the handshake mode after data is stored in the output data latches. Once the handshake mode internal latch is set, the BUS/HAND signal is ignored, the DRQST signal controls data transfer to the external requesting peripheral. (See adjacent diagram.)

This diagram shows the timing for the data transfer with BUS/HAND at logic "1" (throughout the transfer). Note that the DRQST is at logic "1" throughout the transfer. The transfer rate is set by the internal clock. A complete data transfer occurs in 4 clock periods after a DRQST logic "1" is detected on a high to low clock edge transition.



TIMING AND OPERATION (CONT.)

TYPICAL UART INTERFACE TIMING



For peripherals that are unable to accept data at the ADC-800 clock rate, the DRQST input signal can be used to delay the transmit sequence. This mode is useful in interfacing to UART's. (See above Timing Diagram.)

The UART data transfer sequence begins with a logic "1" on DRQST. This indicates the UART transmitter buffer register is empty (TBMT = 1). $\overline{\text{LDSTRB}}$ and $\overline{\text{HBFLG}}$ become active when DRQST is sensed synchronously. The high order data byte is stored in the UART transmitter buffer register when $\overline{\text{LDSTRB}}$ is logic "1". This occurs one clock period after DRQST is sensed. The DRQST signal (TBMT) goes low, stopping the cycle with the SGN and DB15-DB9 data bits active. After the UART transfers the received data to the transmitter register, the DRQST input (TBMT) again goes high. On the first high to low internal clock transition, the high data byte is disabled and one-half clock period later $\overline{\text{HBFLG}}$ goes to logic "1". Concurrently, $\overline{\text{LDSTRB}}$ is logic "0" and DB8-DB1 become active. One clock pulse later, $\overline{\text{LDSTRB}}$ is logic "1" and the low data byte is clocked into the UART transmitter buffer register. DRQST goes low.

When DRQST returns high, it will be sensed on the first internal clock high to low edge transition, thus causing all outputs to be disabled. One half clock period later, the internal handshake mode latch is cleared and $\overline{\text{LDSTRB}}$ = $\overline{\text{HBFLG}}$ = $\overline{\text{LBFLG}}$ = logic "1". The outputs remain active as long as the $\overline{\text{BUS}}$/HAND (Pin 21) is high.

NOTES:

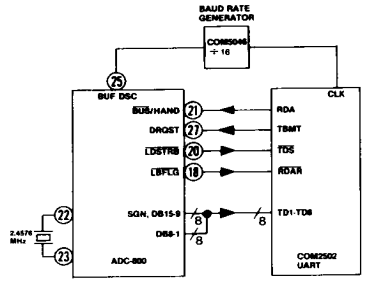
RDA = Receiver Data Available. Set high when character received & transferred to receiver buffer register.

TBMT = Transmitter Buffer Empty. Set high when transmitter buffer register is available for loading with new data.

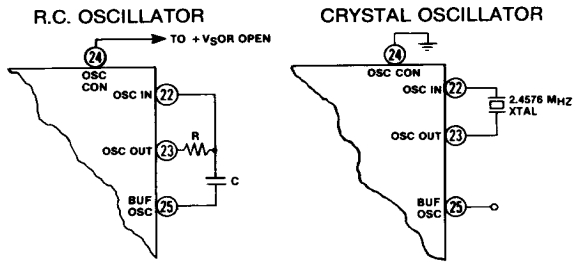
TDS = Transmitter Data Strobe. Low level input transfers data into transmitter register.

RDAR = Receiver Data Available Reset. Low level resets RDA output to logic "0".

TYPICAL CONNECTION TO UART



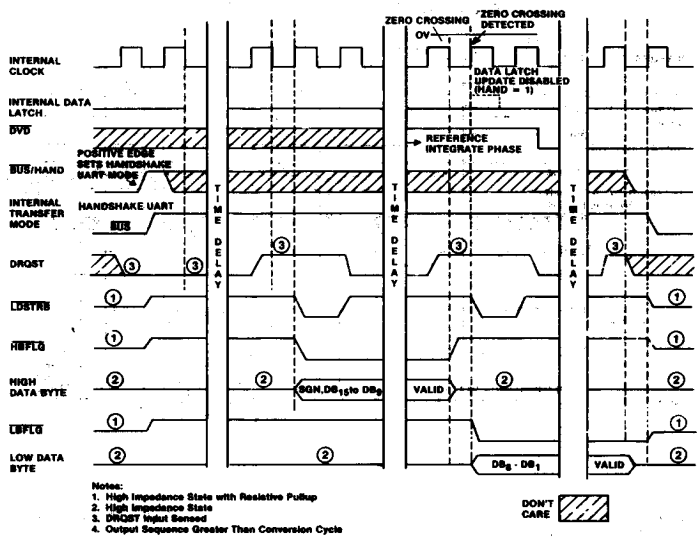
OSCILLATOR OPERATION



OSC TYP	OSC CON (PIN 24)	INT. CLK FREQUENCY	SIGNAL INTEG. TIME	CONVERSION TIME
RC	+ Vs or open	.45/RC	16384(RC/.45)	65536(RC/.45)
XTAL	GROUND	FXTAL/15	16384(15/FXTAL)	65536(15/FXTAL)

TIMING, CONNECTION AND APPLICATION

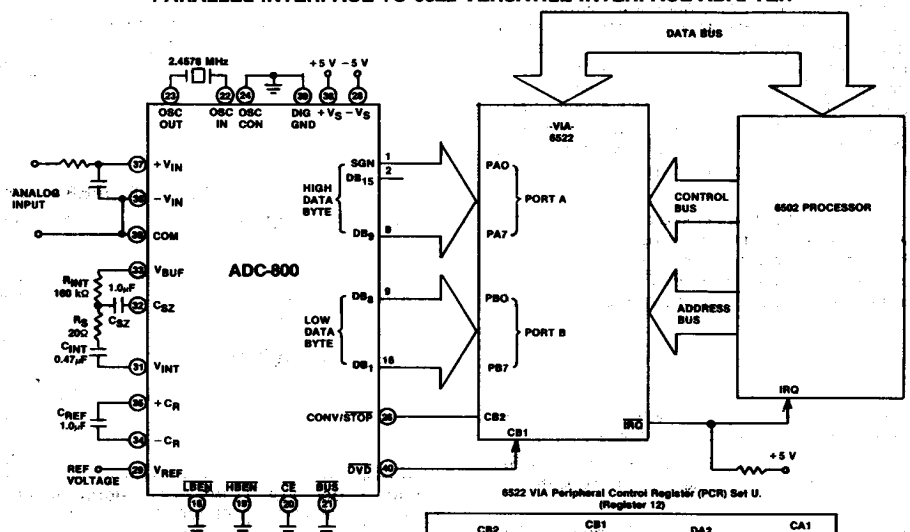
HANDSHAKE OUTPUT ON COMMAND



The ADC-800 will output every conversion with $\overline{BUS}$/HAND at logic "1" (except those completed during a handshake transfer). Handshake output sequences on demand are possible by triggering the $\overline{BUS}$/HAND control input with a low to high edge. The diagram, "HANDSHAKE OUTPUT ON COMMAND" shows a typical data transfer.

The output cycle is controlled by the DRQST input signal. The complete two byte data transfer can take any length of time. Conversions are performed and the $\overline{DVD}$ and CONV/$\overline{STOP}$ inputs function normally but new data will not be latched until the handshake mode is ended.

PARALLEL INTERFACE TO 6522 VERSATILE INTERFACE ADAPTER



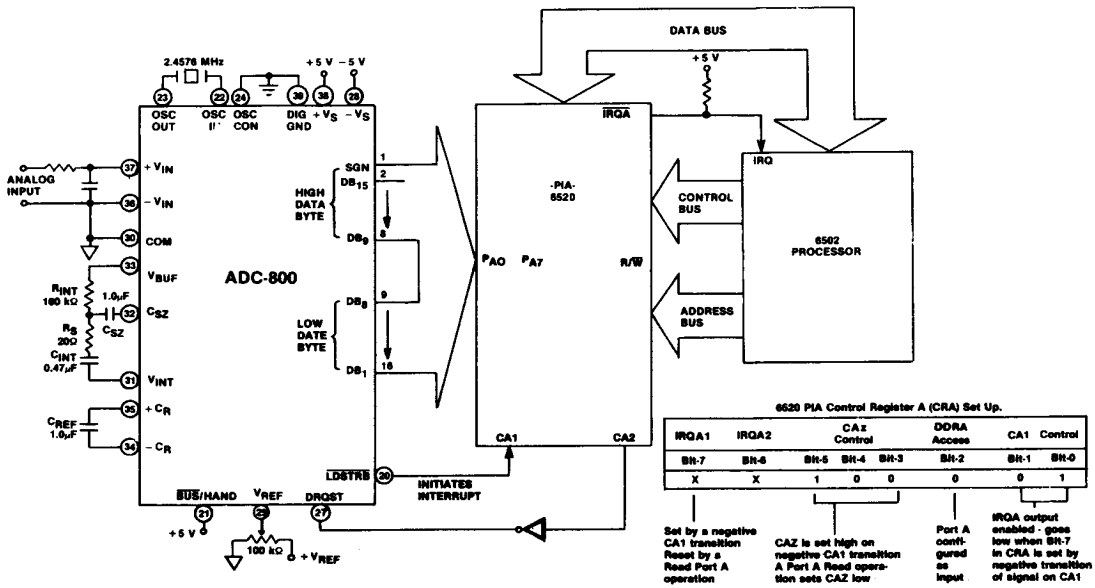
6522 VIA Peripheral Control Register (PCR) Set U. (Register 12)

CB2 Control			CB1 Interrupt Control	DA2 Control			CA1 Interrupt Control
BIT-7	BIT-6	BIT-5	BIT-4	BIT-3	BIT-2	BIT-1	BIT-0
1	1	0/1*0	—	—	—	—	—

*May be programmed for convert on command or continuous conversions

APPLICATION

INTERFACE TO 6520 PIA



6520 PIA Control Register A (CRA) Set Up.

IRQA1	IRQA2	CAz Control			DDRA Access	CA1 Control	
BH-7	BH-6	BH-5	BH-4	BH-3	BH-2	BH-1	BH-0
X	X	1	0	0	0	0	1

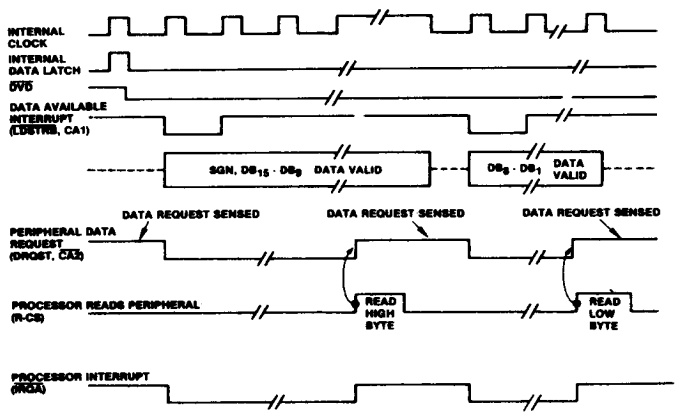
Set by a negative CA1 transition Reset by a Read Port A operation

CAZ is set high on negative CA1 transition A Port A Read operation sets CAZ low

Port A configured as input

IRQA output enabled - goes low when BH-7 in CRA is set by negative transition of signal on CA1

HANDSHAKE TIMING DIAGRAM



Note: Data from every conversion is transmitted in two bytes (Data read cycle is less than conversion time)

HIGH "Z" STATE.--------

ORDERING INFORMATION

MODEL NO.
ADC-800