



September 2007

## ADC1175-50

### 8-Bit, 50 MSPS, 125 mW A/D Converter

#### General Description

The ADC1175-50 is a low power, 50 MSPS analog-to-digital converter that digitizes signals to 8 bits while consuming just 125 mW (typ). The ADC1175-50 uses a unique architecture that achieves 6.8 Effective Bits at 25 MHz input and 50 MHz clock frequency. Output formatting is straight binary coding.

The excellent DC and AC characteristics of this device, together with its low power consumption and +5V single supply operation, make it ideally suited for many video and imaging applications, including use in portable equipment. Furthermore, the ADC1175-50 is resistant to latch-up and the outputs are short-circuit proof. The top and bottom of the ADC1175-50's reference ladder is available for connections, enabling a wide range of input possibilities. The low input capacitance (7 pF, typical) makes this device easier to drive than conventional flash converters and the power down mode reduces power consumption to less than 5 mW.

The ADC1175-50 is offered in TSSOP and is designed to operate over the extended commercial temperature range of -20°C to +75°C.

#### Features

- Internal Track-and-Hold function
- Single +5V operation
- Internal reference bias resistors
- Industry standard pinout
- Power-down mode (<5 mW)

#### Key Specifications

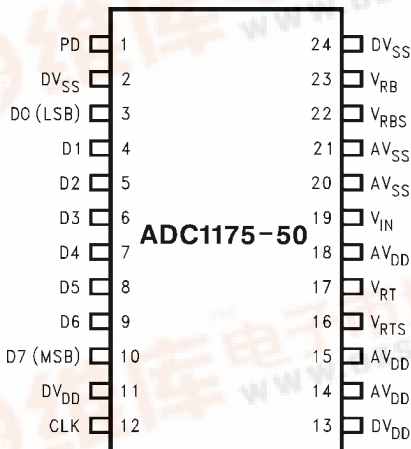
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|---|----------------------------|
| ■ Resolution                                      | 8 Bits                     |
| ■ Maximum Sampling Frequency                      | 50 MSPS (min)              |
| ■ THD   | 54 dB (typ)                |
| ■ DNL   | 0.7 LSB (typ)              |
| ■ ENOB @ $f_{IN} = 25$ MHz                        | 6.8 Bits (typ)             |
| ■ Guaranteed No Missing Codes                     |                            |
| ■ Power Consumption (Excluding Reference Current) | 125 mW (typ), 190 mW (max) |

#### Applications

- Digital Still Cameras
- CCD Imaging
- Electro-Optics
- Video Digitization
- Multimedia

#### Connection Diagrams

24-pin SOIC and TSSOP

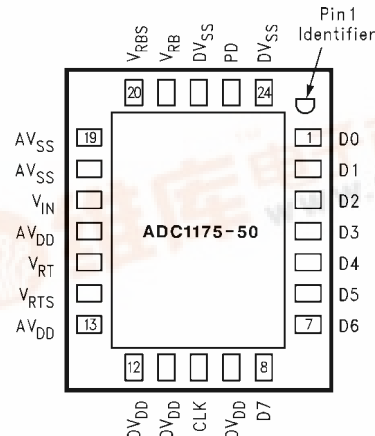


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Top View

SOIC obsolete. Shown for reference only

24-pin LLP (CSP)



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Bottom View

ADC1175-50 8-Bit, 50 MSPS, 125 mW A/D Converter

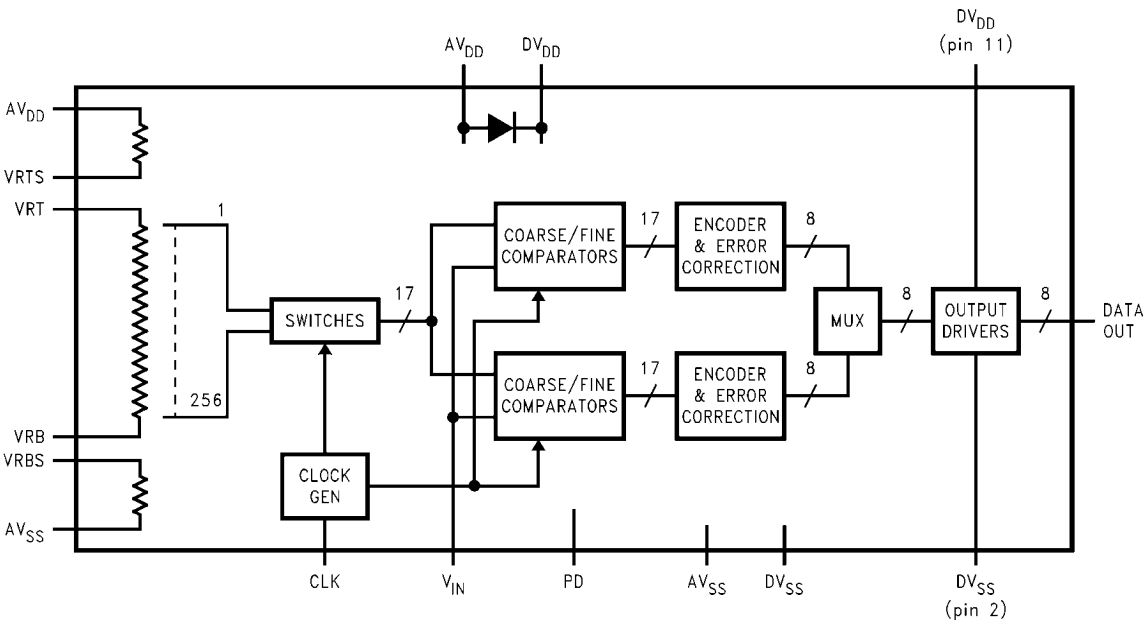


Ordering Information

Order Code	Temperature Range	Description
ADC1175-50CIJM *	-20°C to +70°C	SOIC (EIAJ)
ADC1175-50CIJMX *	-20°C to +70°C	SOIC (EIAJ) tape and reel
ADC1175-50CIMT	-20°C to +70°C	TSSOP
ADC1175-50CIMTX	-20°C to +70°C	TSSOP (tape and reel)
ADC1175-50CILQ *	-20°C to +70°C	LLP tape and reel (1,000 units)
ADC1175-50CILQX *	-20°C to +70°C	LLP tape and reel (4,500 units)
ADC1175-50EVAL *		Evaluation Board

Obsolete in the SOIC (EIAJ) and LLP packages. The Evaluation Board is also discontinued. Shown for reference only.

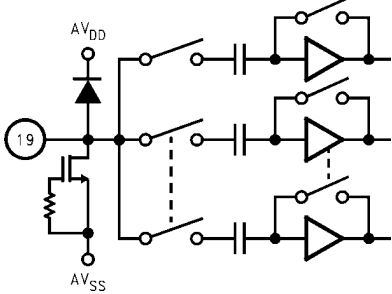
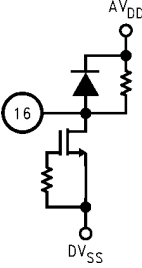
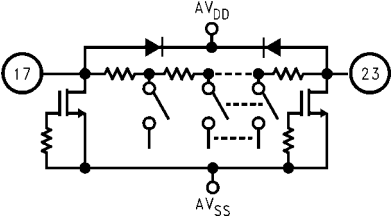
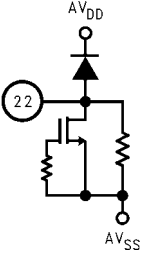
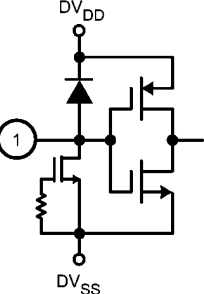
Block Diagram

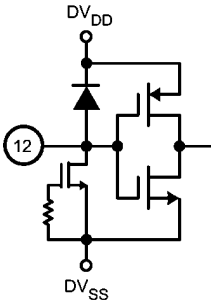
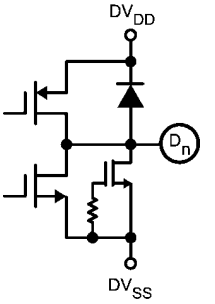


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## Pin Descriptions and Equivalent Circuits

(LLP pins in parentheses)

Pin No.	Symbol	Equivalent Circuit	Description
19 (17)	$V_{IN}$		Analog signal input. Conversion range is $V_{RT}$ to $V_{RB}$ .
16 (14)	$V_{RTS}$		Reference Top Bias with internal pull up resistor. Short this pin to $V_{RT}$ to self-bias the reference ladder.
17 (15)	$V_{RT}$		Analog input that is the high (top) side of the reference ladder of the ADC. Voltages on $V_{RT}$ and $V_{RB}$ inputs define the $V_{IN}$ conversion range. Bypass well. See Section 2.0 for more information.
23 (21)	$V_{RB}$		Analog input that is the low (bottom) side of the reference ladder of the ADC. Nominal range is 0.0V to 4.0V, with optimized value of 0.6V. Voltage on $V_{RT}$ and $V_{RB}$ inputs define the $V_{IN}$ conversion range. Bypass well. See Section 2.0 for more information.
22 (20)	$V_{RBS}$		Reference Bottom Bias with internal pull down resistor. Short to $V_{RB}$ to self-bias the reference ladder. Bypass well (unless grounded). See Section 2.0 for more information.
1 (23)	PD		CMOS/TTL compatible Digital input that, when high, puts the ADC1175-50 into a power-down mode where total power consumption is typically less than 5 mW. With this pin low, the device is in the normal operating mode.

Pin No.	Symbol	Equivalent Circuit	Description
12 (10)	CLK		CMOS/TTL compatible digital clock input. $V_{IN}$ is sampled on the falling edge of CLK input.
3 thru 10 (1 thru 8)	D0–D7		Conversion data digital Output pins. D0 is the LSB, D7 is the MSB. Valid data is output just after the rising edge of the CLK input. These pins are in a high impedance mode when the PD pin is low.
11, 13, 14 (9, 11, 12)	DV <sub>DD</sub>		Positive digital supply pin. Connect to a quiet voltage source of +5V. $AV_{DD}$ and $DV_{DD}$ should have a common source and be separately bypassed with a 10 $\mu$ F capacitor and a 0.1 $\mu$ F ceramic chip capacitor. See Section 4.0 for more information.
2, 24 (22, 24)	DV <sub>SS</sub>		The ground return for the digital supply. $AV_{SS}$ and $DV_{SS}$ should be connected together close to the ADC1175-50.
15, 18 (13, 16)	AV <sub>DD</sub>		Positive analog supply pin. Connect to a quiet voltage source of +5V. $AV_{DD}$ and $DV_{DD}$ should have a common source and be separately bypassed with a 10 $\mu$ F capacitor and a 0.1 $\mu$ F ceramic chip capacitor. See Section 4.0 for more information.
20, 21 (18, 19)	AV <sub>SS</sub>		The ground return for the analog supply. $AV_{SS}$ and $DV_{SS}$ should be connected together close to the ADC1175-50 package.

## Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $AV_{DD}$ , $DV_{DD}$ )	6.5V
Voltage on Any Input or Output Pin	-0.3V to +6.5V
Reference Voltage ( $V_{RT}$ , $V_{RB}$ )	$AV_{SS}$ to $V_{DD}$
CLK, PD Voltage Range	-0.5 to ( $AV_{DD}$ +0.5V)
Digital Output Voltage ( $V_{OH}$ , $V_{OL}$ )	$V_{SS}$ to $V_{DD}$
Input Current at Any Pin (Note 3)	$\pm 25$ mA
Package Input Current (Note 3)	$\pm 50$ mA
Power Dissipation at $T_A = 25^\circ\text{C}$	See (Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	2000V
Machine Model	250V
Soldering Temperature, Infrared, (10 sec.) (Note 6)	235°C
Storage Temperature	-65°C to +150°C
Short Circuit Duration (Single High Output to Ground)	1 Second

## Operating Ratings (Notes 1, 2)

Operating Temperature Range	$-20^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$
Supply Voltage ( $AV_{DD}$ , $DV_{DD}$ )	+4.75V to +5.25V
$AV_{DD} - DV_{DD}$	<0.5V
Ground Difference $IDV_{SS} - AV_{SS}$	0V to 100 mV
Pin 11 to Pin 13 Voltage	<0.5V
Upper Reference Voltage ( $V_{RT}$ )	1.0V to $V_{DD}$
Lower Reference Voltage ( $V_{RB}$ )	0V to 4.0V
$V_{RT} - V_{RB}$	1V to 2.8V
$V_{IN}$ Voltage Range	$V_{RB}$ to $V_{RT}$

## Package Thermal Resistance

Package	$\theta_{JA}$
TSSOP-24	92°C / W
LLP-24	40°C / W

## Converter Electrical Characteristics

The following specifications apply for  $AV_{DD} = DV_{DD} = +5.0$  V<sub>DC</sub>, PD = 0V,  $V_{RT} = +2.6$ V,  $V_{RB} = 0.6$ V,  $C_L = 20$  pF,  $f_{CLK} = 50$  MHz at 50% duty cycle. **Boldface limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = 25^\circ\text{C}$  (Notes 7, 8).

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
<b>DC ACCURACY</b>					
INL	Integral Non Linearity Error	$V_{IN} = 0.6\text{V to } 2.6\text{V}$	$\pm 0.8$	<b><math>\pm 1.95</math></b>	LSB (max)
DNL	Differential Non-Linearity	$V_{IN} = 0.6\text{V to } 2.6\text{V}$	+0.7	<b>+1.75</b>	LSB (max)
			-0.7	<b>-1.0</b>	LSB (min)
	Resolution for No Missing Codes			<b>8</b>	Bits
$E_{OT}$	Top Offset Voltage		-12		mV
$E_{OB}$	Bottom Offset Voltage		+10		mV
<b>VIDEO ACCURACY</b>					
DP	Differential Phase Error	$f_{IN} = 4.43$ MHz Modulated Ramp	0.5		deg
DG	Differential Gain Error	$f_{IN} = 4.43$ MHz Modulated Ramp	1.0		%
<b>ANALOG INPUT AND REFERENCE CHARACTERISTIC</b>					
$V_{IN}$	Input Range		2.0	$V_{RB}$	V (min)
				$V_{RT}$	V (max)
$C_{IN}$	$V_{IN}$ Input Capacitance	$V_{IN} = 1.5\text{V}$ +0.7 Vrms	(CLK LOW)	4	pF
			(CLK HIGH)	7	pF
$R_{IN}$	$R_{IN}$ Input Resistance		>1		M $\Omega$
BW	Full Power Bandwidth		120		MHz
$R_{RT}$	Top Reference Resistor		320		$\Omega$
$R_{REF}$	Reference Ladder Resistance	$V_{RT}$ to $V_{RB}$	270	<b>200</b> <b>350</b>	$\Omega$ (min) $\Omega$ (max)
$R_{RB}$	Bottom Reference Resistor		80		$\Omega$
$I_{REF}$	Reference Ladder Current	$V_{RT} = V_{RTS}$ , $V_{RB} = V_{RBS}$	7	<b>5.4</b>	mA (min)
				<b>10.8</b>	mA (max)
		$V_{RT} = V_{RTS}$ , $V_{RB} = AV_{SS}$	8	<b>6.1</b>	mA (min)
				<b>12.3</b>	mA (max)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
V <sub>RT</sub>	Reference Top Self Bias Voltage	V <sub>RT</sub> Connected to V <sub>RTS</sub> , V <sub>RB</sub> Connected to V <sub>RBS</sub>	2.6		V (min) V (max)
V <sub>RB</sub>	Reference Bottom Self Bias Voltage	V <sub>RT</sub> Connected to V <sub>RTS</sub> , V <sub>RB</sub> Connected to V <sub>RBS</sub>	0.6	<b>0.55</b> <b>0.70</b>	V (min) V (max)
V <sub>RTS</sub> – V <sub>RBS</sub>	Self Bias Voltage Delta	V <sub>RT</sub> Connected to V <sub>RTS</sub> , V <sub>RB</sub> Connected to V <sub>RBS</sub>	2	<b>1.89</b> <b>2.20</b>	(V (min) V (max)
		V <sub>RT</sub> Connected to V <sub>RTS</sub> , V <sub>RB</sub> Connected to AV <sub>SS</sub>	2.3		V
V <sub>RT</sub> – V <sub>RB</sub>	Reference Voltage Differential		2	<b>1.0</b> <b>2.8</b>	V (min) V (max)
CONVERTER DYNAMIC CHARACTERISTICS					
ENOB	Effective Number of Bits	f <sub>IN</sub> = 4.4 MHz, f <sub>CLK</sub> = 40 MHz	7.2	<b>6.7</b>	Bits (min)
		f <sub>IN</sub> = 19.9 MHz, f <sub>CLK</sub> = 40 MHz	7.0	<b>6.4</b>	Bits (min)
		f <sub>IN</sub> = 1.3 MHz, f <sub>CLK</sub> = 50 MHz	7.3		Bits
		f <sub>IN</sub> = 4.4 MHz, f <sub>CLK</sub> = 50 MHz	7.2		Bits
		f <sub>IN</sub> = 24.9 MHz, f <sub>CLK</sub> = 50 MHz	6.8	<b>6.1</b>	Bits (min)
SINAD	Signal-to-Noise & Distortion	f <sub>IN</sub> = 4.4 MHz, f <sub>CLK</sub> = 40 MHz	45	<b>42</b>	dB (min)
		f <sub>IN</sub> = 19.9 MHz, f <sub>CLK</sub> = 40 MHz	44	<b>40</b>	dB (min)
		f <sub>IN</sub> = 1.3 MHz, f <sub>CLK</sub> = 50 MHz	46		dB
		f <sub>IN</sub> = 4.4 MHz, f <sub>CLK</sub> = 50 MHz	45		dB
		f <sub>IN</sub> = 24.9 MHz, f <sub>CLK</sub> = 50 MHz	43	<b>38.4</b>	dB (min)
SNR	Signal-to-Noise Ratio	f <sub>IN</sub> = 4.4 MHz, f <sub>CLK</sub> = 40 MHz	46	<b>42.5</b>	dB (min)
		f <sub>IN</sub> = 19.9 MHz, f <sub>CLK</sub> = 40 MHz	44	<b>41</b>	dB (min)
		f <sub>IN</sub> = 1.3 MHz, f <sub>CLK</sub> = 50 MHz	48		dB
		f <sub>IN</sub> = 4.4 MHz, f <sub>CLK</sub> = 50 MHz	45		dB
		f <sub>IN</sub> = 24.9 MHz, f <sub>CLK</sub> = 50 MHz	44	<b>40</b>	dB (min)
SFDR	Spurious Free Dynamic Range	f <sub>IN</sub> = 1.3 MHz	57		dB
		f <sub>IN</sub> = 4.4 MHz	56		dB
		f <sub>IN</sub> = 24.9 MHz	51		dB
THD	Total Harmonic Distortion	f <sub>IN</sub> = 1.3 MHz	–55		dB
		f <sub>IN</sub> = 4.4 MHz	–54		dB
		f <sub>IN</sub> = 24.9 MHz	–51		dB
POWER SUPPLY CHARACTERISTICS					
IA <sub>DD</sub>	Analog Supply Current	DV <sub>DD</sub> = AV <sub>DD</sub> = 5.25V	13		mA
ID <sub>DD</sub>	Digital Supply Current	DV <sub>DD</sub> = AV <sub>DD</sub> = 5.25V	11		mA
IA <sub>DD</sub> + ID <sub>DD</sub>	Total Operating Current	DV <sub>DD</sub> = AV <sub>DD</sub> = 5.25V, f <sub>CLK</sub> = 50 MHz	25	<b>36</b>	mA (max)
		DV <sub>DD</sub> = AV <sub>DD</sub> = 5.25V, CLK Inactive (low)	14		mA
	Power Consumption	PD pin low	125	<b>190</b>	mW (max)
	Power Consumption	PD pin high	<5 mW		mW
CLK, PD DIGITAL INPUT CHARACTERISTICS					
V <sub>IH</sub>	Logical High Input Voltage			<b>2.0</b>	V (min)
V <sub>IL</sub>	Logical Low Input Voltage			<b>0.8</b>	V (max)
I <sub>IH</sub>	Logical High Input Current	V <sub>IH</sub> = DV <sub>DD</sub> = AV <sub>DD</sub> = +5.25V		<b>±5</b>	µA (max)
I <sub>IL</sub>	Logical Low Input Current	V <sub>IL</sub> = 0V, DV <sub>DD</sub> = AV <sub>DD</sub> = +5.25V		<b>±5</b>	µA (max)
C <sub>IN</sub>	Digital Input Capacitance		4		pF
DIGITAL OUTPUT CHARACTERISTICS					
I <sub>OH</sub>	Output Current, Logic HIGH	DV <sub>DD</sub> = 4.75V, V <sub>OH</sub> = 4.0V		<b>–1.1</b>	mA (min)
I <sub>OL</sub>	Output Current, Logic LOW	DV <sub>DD</sub> = 4.75V, V <sub>OL</sub> = 0.4V		<b>1.8</b>	mA (min)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 9)	Units (Limits)
$I_{OZH}, I_{OZL}$	TRI-STATE® Output Current	$DV_{DD} = 5.25V$ , $PD = DV_{DD}$ , $V_{OL} = DV_{DD}$ , or $V_{OL} = 0V$	$\pm 20$		$\mu A$

**AC ELECTRICAL CHARACTERISTICS**

$f_{C1}$	Maximum Conversion Rate		55	<b>50</b>	MHz (min)
$f_{C2}$	Minimum Conversion Rate		1		MHz
$t_{OD}$	Output Delay	CLK high to data valid	14	<b>5</b>	ns (min)
				<b>20</b>	ns (max)
	Pipeline Delay (Latency)		2.5		Clock Cycles
$t_{DS}$	Sampling (Aperture) Delay	CLK low to acquisition of data	3		ns
$t_{AJ}$	Aperture Jitter		10		ps rms
$t_{OH}$	Output Hold Time	CLK high to data invalid	10		ns
$t_{EN}$	PD Low to Data Valid	Loaded as in <i>Figure 2</i>	140		ns

**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

**Note 2:** All voltages are measured with respect to  $GND = AV_{SS} = DV_{SS} = 0V$ , unless otherwise specified.

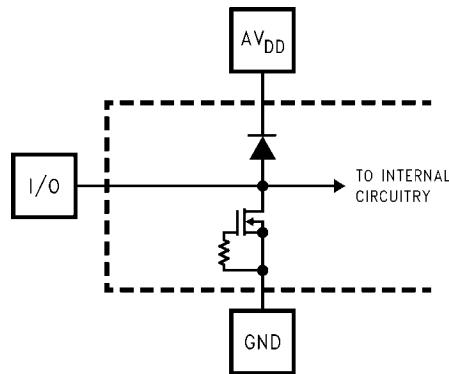
**Note 3:** When the input voltage at any pin exceeds the power supplies (that is, less than  $AV_{SS}$  or  $DV_{SS}$ , or greater than  $AV_{DD}$  or  $DV_{DD}$ ), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 25 mA to two.

**Note 4:** The absolute maximum junction temperature ( $T_J$  max) for this device is 150°C. The maximum allowable power dissipation is dictated by  $T_J$  max, the junction-to-ambient thermal resistance ( $\theta_{JA}$ ) and the ambient temperature ( $T_A$ ), and can be calculated using the formula  $P_D \text{ max} = (T_J \text{ max} - T_A)/\theta_{JA}$ . The values for maximum power dissipation listed above will be reached only when the ADC1175-50 is operated in a severe fault condition (e.g., when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Obviously, such conditions should always be avoided.

**Note 5:** Human body model is 100 pF capacitor discharged through a 1.5 k $\Omega$  resistor. Machine model is 220 pF discharged through 0 $\Omega$ .

**Note 6:** See AN-450, "Surface Mounting Methods and Their Effect on Product Reliability", or the section entitled "Surface Mount" found in any post 1986 National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

**Note 7:** The analog inputs are protected as shown below. Input voltage magnitudes up to 6.5V or 500 mV below GND will not damage this device. However, errors in the A/D conversion can occur if the input goes above  $V_{DD}$  or below GND by more than 50 mV. As an example, if  $AV_{DD}$  is 4.75  $V_{DC}$ , the full-scale input voltage must be  $\leq 4.80 V_{DC}$  to ensure accurate conversions.

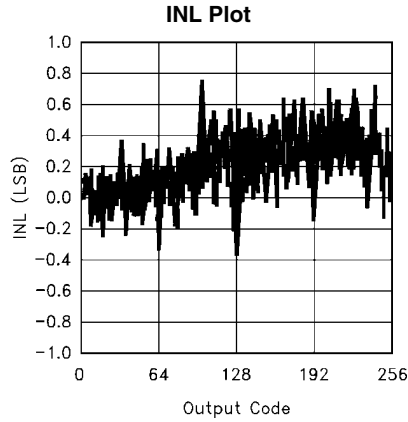


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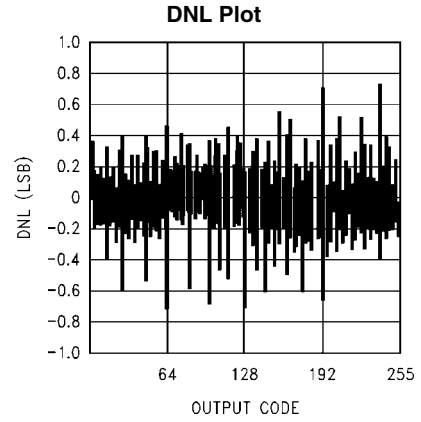
**Note 8:** To guarantee accuracy, it is required that  $AV_{DD}$  and  $DV_{DD}$  be well bypassed. Each  $V_{DD}$  pin must be decoupled with separate bypass capacitors.

**Note 9:** Typical figures are at  $T_J = 25^\circ C$ , and represent most likely parametric norms. Test limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

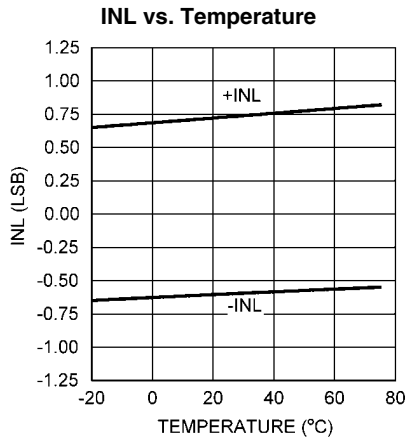
# Typical Performance Characteristics $AV_{DD} = DV_{DD} = 5V$ , $f_{CLK} = 50\text{ MHz}$ , unless otherwise stated.



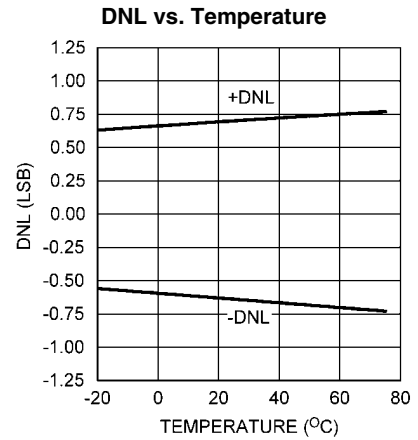
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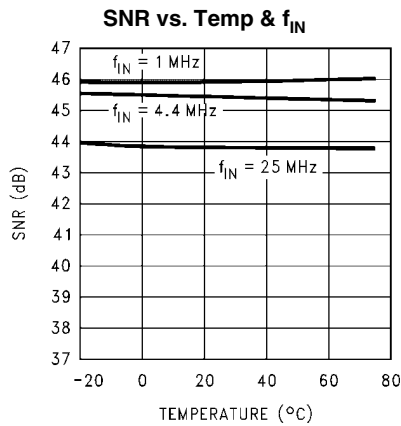
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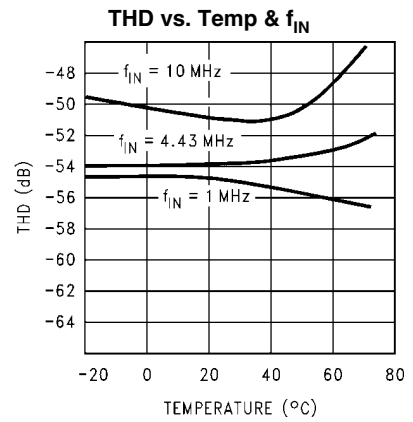
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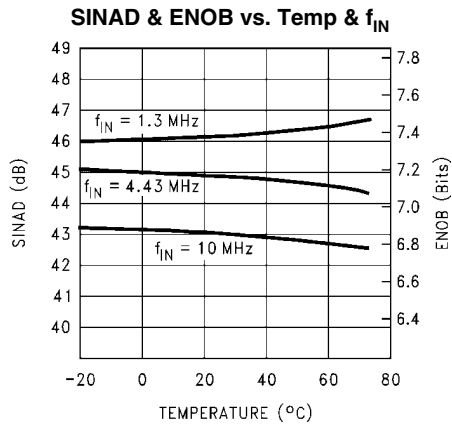


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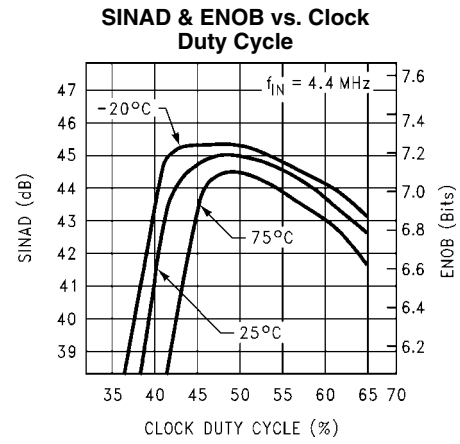


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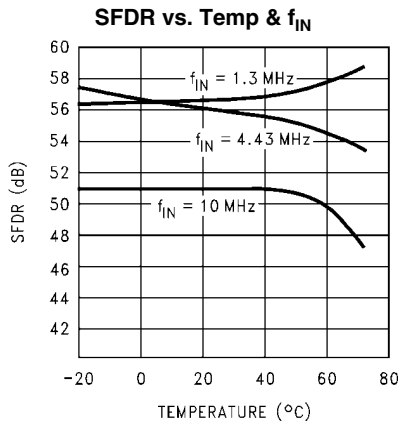




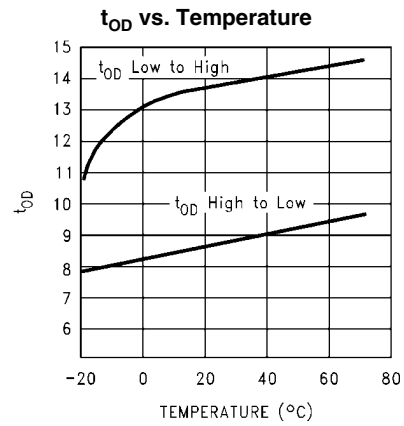
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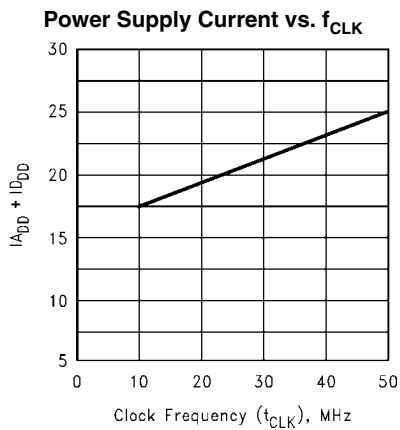
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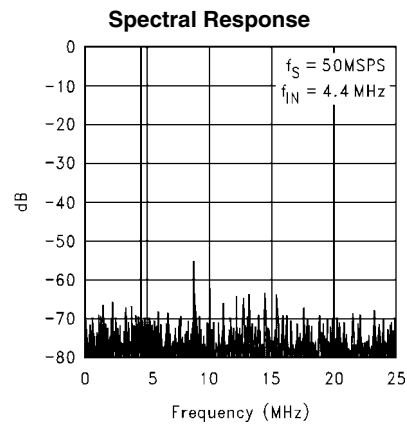
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## Specification Definitions

**ANALOG INPUT BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input. The test is performed with  $f_{IN}$  equal to 100 kHz plus integer multiples of  $f_{CLK}$ . The input frequency at which the output is -3 dB relative to the low frequency input signal is the full power bandwidth.

**APERTURE JITTER** is the time uncertainty of the sampling point ( $t_{DS}$ ), or the range of variation in the sampling delay.

**BOTTOM OFFSET** is the difference between the input voltage that just causes the output code to transition to the first code and the negative reference voltage. Bottom Offset is defined as  $E_{OB} = V_{ZT} - V_{RB}$ , where  $V_{ZT}$  is the first code transition input voltage. Note that this is different from the normal Zero Scale Error.

**DIFFERENTIAL GAIN ERROR** is the percentage difference between the output amplitudes of a high frequency reconstructed sine wave at two different d.c. levels.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB. DNL is measured at the rated clock frequency with a ramp input.

**DIFFERENTIAL PHASE ERROR** is the difference in the output phase of a reconstructed small signal sine wave at two different d.c. levels.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion Ratio, or SINAD. ENOB is defined as  $(SINAD - 1.76) / 6.02$  and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual codes from a line drawn from zero scale (1/2 LSB below the first code transition) through positive full scale (1/2 LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value. The end point test method is used. INL is measured at rated clock frequency with a ramp input.

**OUTPUT DELAY** is the time delay after the rising edge of the input clock before the data update is present at the output pins.

**OUTPUT HOLD TIME** is the length of time that the output data is valid after the rise of the input clock.

**PIPELINE DELAY (LATENCY)** is the number of clock cycles between initiation of conversion and when that data is presented to the output stage. Data for any given sample is available the Pipeline Delay plus the Output Delay after that sample is taken. New data is available at every clock cycle, but the data lags the conversion by the pipeline delay.

**SAMPLING (APERTURE) DELAY**, or  $t_{DS}$ , is the time required after the falling edge of the clock for the sampling switch to open (in other words, for the Sample/Hold circuit to go from the "sample" mode into the "hold" mode). The Sample/Hold circuit effectively stops capturing the input signal and goes into the "hold" mode  $t_{DS}$  after the clock goes low.

**SIGNAL TO NOISE RATIO (SNR)** is the ratio of the rms value of the input signal to the rms value of the other spectral components below one-half the sampling frequency, not including harmonics or d.c.

**SIGNAL TO NOISE PLUS DISTORTION (S/(N+D) or SINAD)** is the ratio of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the rms values of the input signal and the peak spurious signal, where a spurious signal is any signal present in the output spectrum that is not present at the input.

**TOP OFFSET** is the difference between the positive reference voltage and the input voltage that just causes the output code to transition to full scale and is defined as  $E_{OT} = V_{FT} - V_{RT}$ . Where  $V_{FT}$  is the full scale transition input voltage. Note that this is different from the normal Full Scale Error.

**TOTAL HARMONIC DISTORTION (THD)** is the ratio of the rms total of the first six harmonic components to the rms value of the input signal.

## Timing Diagram

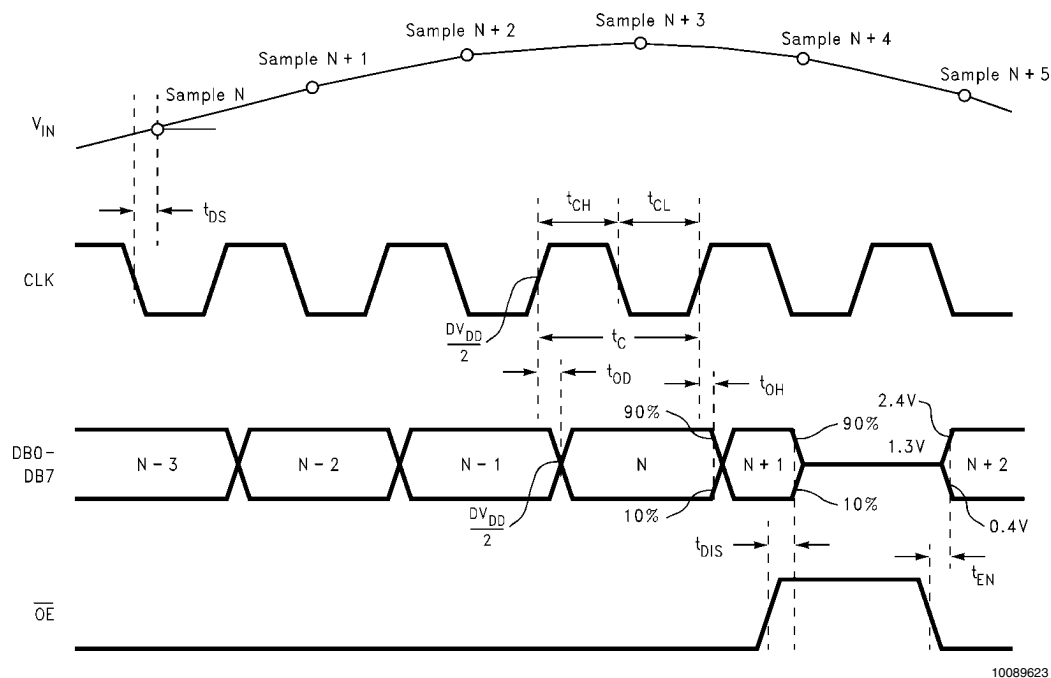
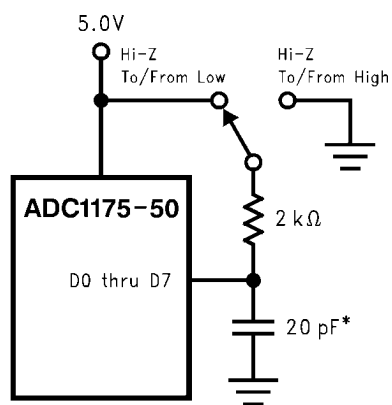


FIGURE 1. ADC1175-50 Timing Diagram



\* Includes stray and distributed capacitance

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FIGURE 2.  $t_{EN}$ ,  $t_{DIS}$  Test Circuit

## Functional Description

The ADC1175-50 maintains superior dynamic performance with input frequencies up to 1/2 the clock frequency, achieving 6.8 effective bits with a 50 MHz sampling rate and 25 MHz input frequency.

The analog signal at  $V_{IN}$  that is within the voltage range set by  $V_{RT}$  and  $V_{RB}$  are digitized to eight bits at up to 55 MSPS. Input voltages below  $V_{RB}$  will cause the output word to consist of all zeroes. Input voltages above  $V_{RT}$  will cause the output word to consist of all ones. While the ADC1175-50 is specified for top and bottom reference voltages ( $V_{RT}$  and  $V_{RB}$ ) or 2.6V and 0.6V, respectively, and will give best performance at these values,  $V_{RT}$  has a range of 1.0V to the analog supply voltage,  $AV_{DD}$ , while  $V_{RB}$  has a range of 0V to 4.0V.  $V_{RT}$  should always be at least 1.0V more positive than  $V_{RB}$ . With  $V_{RT}$  voltages above 2.8V, it is necessary to reduce the clock frequency to maintain SINAD performance.  $V_{RT}$  should always be between 1.0V and 2.8V more positive than  $V_{RB}$ .

If  $V_{RT}$  and  $V_{RTS}$  are connected together and  $V_{RB}$  and  $V_{RBS}$  are connected together, the nominal values of  $V_{RT}$  and  $V_{RB}$  are 2.6V and 0.6V, respectively. If  $V_{RT}$  and  $V_{RTS}$  are connected together and  $V_{RB}$  is grounded, the nominal value of  $V_{RT}$  is 2.3V.

Data is acquired at the falling edge of the clock and the digital equivalent of that data is available at the digital outputs 2.5 clock cycles plus  $t_{OD}$  later. The ADC1175-50 will convert as long as the clock signal is present at the CLK pin. The PD pin, when high, puts the device into the Power Down mode. When the PD pin is low, the device is in the normal operating mode.

The Power Down pin (PD), when high, puts the ADC1175-50 into a power down mode where power consumption is typi-

cally less than 5 mW. When the part is powered down, the digital output pins are in a high impedance TRI-STATE. It takes about 140 ns for the part to become active upon coming out of the power down mode.

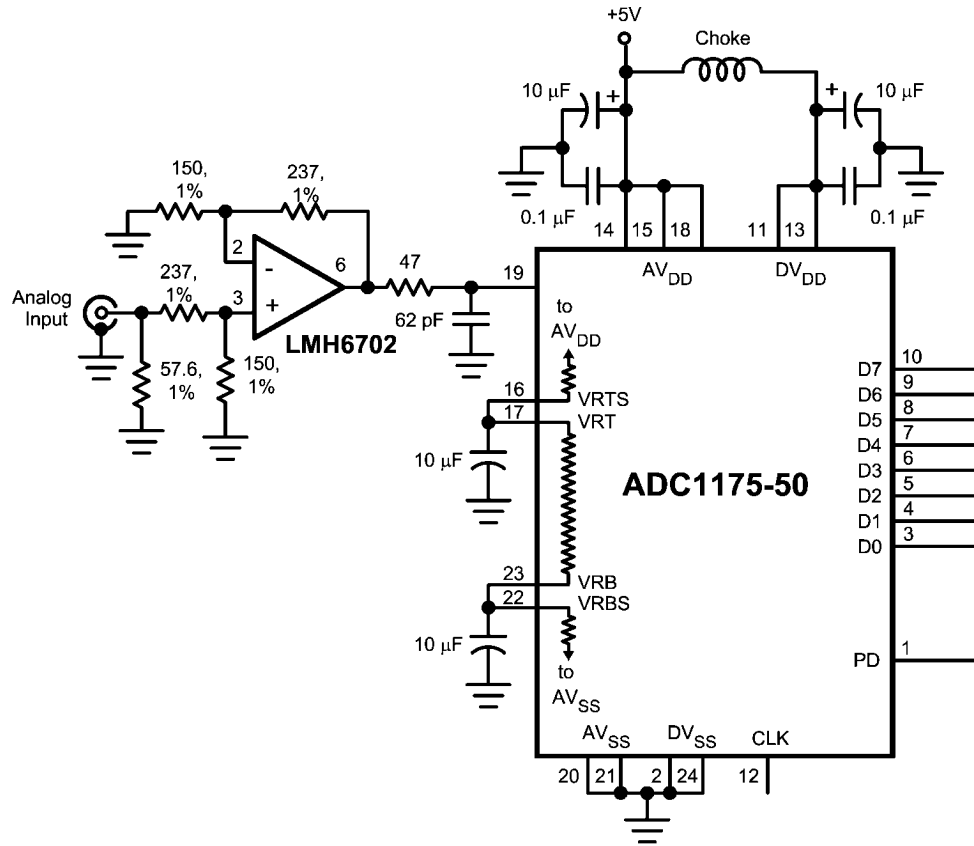
## Applications Information

(All Schematic pin numbers refer to the TSSOP.)

### 1.0 THE ANALOG INPUT

The analog input of the ADC1175-50 is a switch followed by an integrator. That is, a switched capacitor input, appearing as 4 pF when the clock is low, and 7 pF when the clock is high. Switched capacitor inputs produce voltage spikes at the input pin at the ADC sample rate. There should be no attempt to eliminate these spikes, but they should settle out during the sample period (the clock high time). An RC at the ADC analog input pin, as shown in *Figure 3*, will help. For Nyquist applications, the capacitor should be about 10 times ADC track mode input capacitance and the pole frequency of this RC should be about the ADC sample rate. The LMH6702, and the LMH6609 have been found to be excellent amplifiers for driving the ADC1175-50. Do not drive the input beyond the supply rails. *Figure 3* shows an example of an input circuit using the LMH6702.

Driving the analog input with input signals up to 2.8  $V_{P-P}$  will result in normal behavior where signals above  $V_{RT}$  will result in a code of FFh and input voltages below  $V_{RB}$  will result in an output code of zero. Input signals above 2.8  $V_{P-P}$  may result in odd behavior where the output code is not FFh when the input exceeds  $V_{RT}$ .



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FIGURE 3. Driving the ADC1175-50. Choose an op-amp that can drive a dynamic capacitance.

The reference ladder can be self-biased by connecting  $V_{RT}$  to  $V_{RTS}$  and connecting the  $V_{RB}$  to  $V_{RBS}$  to provide top and bottom reference voltages of approximately 2.6V and 0.6V, respectively, with  $V_{CC} = 5.0V$ . This connection is shown in *Figure 3*. If  $V_{RT}$  and  $V_{RTS}$  are tied together, but  $V_{RB}$  is tied to analog ground, a top reference voltage of approximately 2.3V is generated. The top and bottom of the ladder should be bypassed with 10  $\mu F$  tantalum capacitors located close to the reference pins.

By forcing a little current into or out of the top and bottom of the ladder, as shown in *Figure 4*, the top and bottom reference voltages can be trimmed and performance improved over the self-bias method of *Figure 3*. The resistive divider at the amplifier inputs can be replaced with potentiometers, if desired. The LMC662 amplifier shown was chosen for its low offset voltage and low cost. Note that a negative power supply is

If reference voltages are desired that are more than a few tens of millivolts from the self-bias values, the circuit of *Figure 5* will allow forcing the reference voltages to whatever levels are desired. This circuit provides the best performance because of the low source impedance of the transistors. Note that the  $V_{RTS}$  and  $V_{RRS}$  pins are left floating.

The ADC1175-50 is designed to operate with top and bottom references of 2.6V and 0.6V, respectively. However, it will function with reduced performance with a top reference voltage as high as  $AV_{DD}$  and a bottom reference voltage as low as ground.

$V_{RT}$  can be anywhere between  $V_{RB} + 1.0V$  and the analog supply voltage, and  $V_{RB}$  can be anywhere between ground and  $1.0V$  below  $V_{RT}$ . To minimize noise effects and ensure accurate conversions, the total reference voltage range ( $V_{RT} - V_{RB}$ ) should be a minimum of  $1.0V$  and a maximum of about  $2.8V$ . If  $V_{RB}$  is not required to be below about  $+700mV$ , the  $-5V$  points in *Figure 5* can be returned to ground and the negative supply eliminated.



**FIGURE 4. Better Defining the ADC Reference Voltage.** Self bias is still used, but the reference voltages are trimmed by providing a small trim current with the operational amplifiers.

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necessary to have sufficient capacitance between the power and ground planes.

If separate analog and digital ground planes are used, the analog and digital grounds may be in the same layer, but should be separated from each other. If separate analog and digital ground layers are used, they should *never overlap* each other.

Capacitive coupling between a typically noisy digital ground plane and the sensitive analog circuitry can lead to poor performance that may seem impossible to isolate and remedy. The solution is to keep the analog circuitry well separated from the digital circuitry.

Digital circuits create substantial supply and ground current transients. The logic noise thus generated could have significant impact upon system noise performance. The best logic family to use in systems with A/D converters is one which employs non-saturating transistor designs, or has low noise characteristics, such as the 74LS and the 74HC(T) families. The worst noise generators are logic families that draw the largest supply current transients during clock or signal edges, like the 74F family. In general, slower logic families will produce less high frequency noise than do high speed logic families.

Since digital switching transients are composed largely of high frequency components, total ground plane copper weight will have little effect upon the logic-generated noise. This is because of the skin effect. Total surface area is more important than is total ground plane volume.

An effective way to control ground noise is by using a single, solid ground plane and splitting the power plane into analog and digital areas and to have power and ground planes in adjacent board layers. There should be no traces within either the power or the ground layers of the board. The analog and digital power planes should reside in the same board layer so that they can not overlap each other. The analog and digital power planes define the analog and digital areas of the board.

Mount digital components and run digital lines only in the digital areas of the board. Mount the analog components and run analog lines only in the analog areas of the board. Be sure to treat all digital lines greater than one inch for each nanosecond of rise time as transmission lines. That is, they should be of constant, controlled impedance, be properly terminated at the source end and run from one point to another single point.

The back of the LLP package has a large metal area inside the area bounded by the pins. This metal area is connected to the die substrate (ground). This pad may be left floating if desired. If it is connected to anything, it should be to ground near the connection between analog and digital ground planes. Soldering this metal pad to ground will help keep the die cooler and could yield improved performance because of the lower impedance between die and board grounds. However, a poor layout could compromise performance.

Generally, analog and digital lines should cross each other at 90° to avoid getting digital noise into the analog path. In high frequency systems, however, avoid crossing analog and digital lines altogether. Clock lines should be isolated from ALL other lines, analog AND digital. Even the generally accepted 90° crossing should be avoided as even a little coupling can cause problems at high frequencies. Best performance at high frequencies and at high resolution is obtained with a straight signal path.

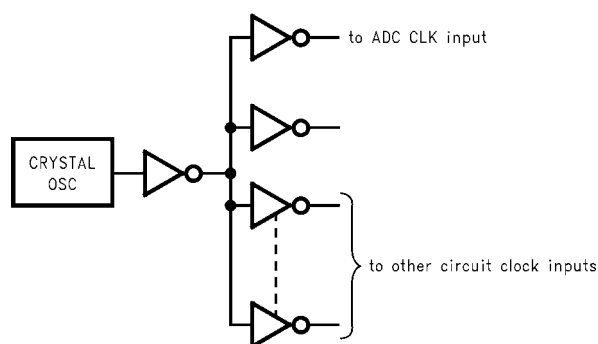
Be especially careful with the layout of inductors. Mutual inductance can change the characteristics of the circuit in which they are used. Inductors should not be placed side by side

with each other, not even with just a small part of their bodies beside each other.

The analog input should be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (e.g., a filter capacitor) connected between the converter's input and ground should be connected to a very clean point in the ground plane.

## 7.0 DYNAMIC PERFORMANCE

The ADC1175-50 is a.c. tested and its dynamic performance is guaranteed. To meet the published specifications, the clock source driving the CLK input must be free of jitter. For best a.c. performance, isolating the ADC clock from any digital circuitry should be done with adequate buffers, as with a clock tree. See Figure 6.



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FIGURE 6. Isolating the ADC Clock from Digital Circuitry

It is good practice to keep the ADC clock line as short as possible and to keep it well away from any other signals. Other signals can introduce jitter into the clock signal.

## 8.0 COMMON APPLICATION PITFALLS

**Driving the inputs (analog or digital) beyond the power supply rails.** For proper operation, all inputs should not go more than 50 mV below the ground pins or 50 mV above the supply pins. Exceeding these limits on even a transient basis may cause faulty or erratic operation. It is not uncommon for high speed digital circuits to exhibit undershoot that goes more than a volt below ground due to improper termination. A resistor of about 50Ω to 100Ω in series with the offending digital input, located close to the signal source, will usually eliminate the problem.

Care should be taken not to overdrive the inputs of the ADC1175-50. Such practice may lead to conversion inaccuracies and even to device damage.

**Attempting to drive a high capacitance digital data bus.** The more capacitance the output drivers have to charge for each conversion, the more instantaneous digital current is required from DV<sub>DD</sub> and DGND. These large charging current spikes can couple into the analog section, degrading dynamic performance. Buffering the digital data outputs (with a 74AC541, for example) may be necessary if the data bus to be driven is heavily loaded. Dynamic performance can also be improved by adding 47Ω series resistors at each digital output, reducing the energy coupled back into the converter output pins.

**Using an inadequate amplifier to drive the analog input.** As explained in Section 1.0, the ADC input is a switched capacitor one and there are voltage spikes present there. This type of input is more difficult to drive than is a fixed capacitance, and should be considered when choosing a driving



device. The LMH6702 and the LMH6609 have been found to be an excellent device for driving the ADC1175-50. Also remember to use the RC between the driving source and the ADC input, as explained in Section 1.0.

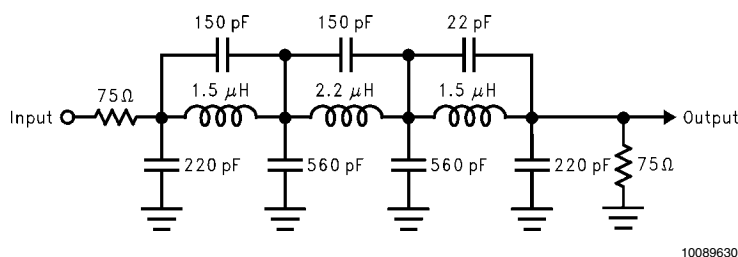
**Driving the  $V_{RT}$  pin or the  $V_{RB}$  pin with devices that can not source or sink the current required by the ladder.** As mentioned in Section 2.0, care should be taken to see that any driving devices can source sufficient current into the  $V_{RT}$  pin and sink sufficient current from the  $V_{RB}$  pin. If these pins are not driven with devices that can handle the required current, these reference pins will not be stable, resulting in a reduction of dynamic performance.

**Using a clock source with excessive jitter, using excessively long clock signal trace, or having other signals coupled to the clock signal trace.** This will cause the sampling interval to vary, causing excessive output noise and a reduction in SNR performance. Simple gates with RC timing is generally inadequate as a clock source.

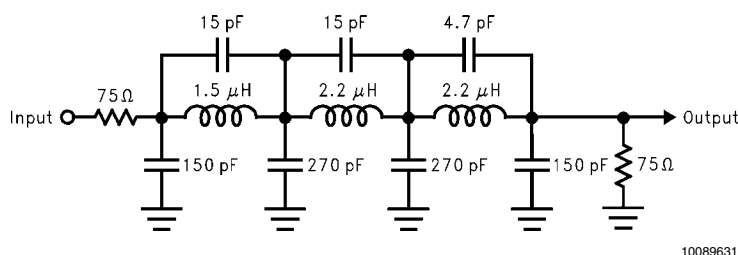
**Input test signal contains harmonic distortion that interferes with the measurement of dynamic signal to noise ratio.** Harmonic and other interfering signals can be removed by inserting a filter at the signal input. Suitable filters are

shown in *Figure 7* and *Figure 8*. The circuit of *Figure 7* has a cutoff of about 5.5 MHz and is suitable for input frequencies of 1 MHz to 5 MHz. The circuit of *Figure 8* has a cutoff of about 11 MHz and is suitable for input frequencies of 5 MHz to 10 MHz. These filters should be driven by a generator of 75 $\Omega$  source impedance and terminated with a 75 $\Omega$  resistor.

**Not considering the effect on a driven CMOS digital circuit(s) when the ADC1175-50 is in the power down mode.** Because the ADC1175-50 output goes into a high impedance state when in the power down mode, any CMOS device connected to these outputs will have their inputs floating when the ADC is in power down. Should the inputs of the circuit being driven by the ADC digital outputs float to a level near 2.5V, a CMOS device could exhibit relative large supply currents as the input stage toggles rapidly. The solution is to use pull-down resistors at the ADC outputs. The value of these resistors is not critical, as long as they do not cause excessive currents in the outputs of the ADC1175-50. Low pull-down resistor values could result in degraded SNR and SINAD performance of the ADC1175-50. Values between 5 k $\Omega$  and 10 k $\Omega$  should work well.

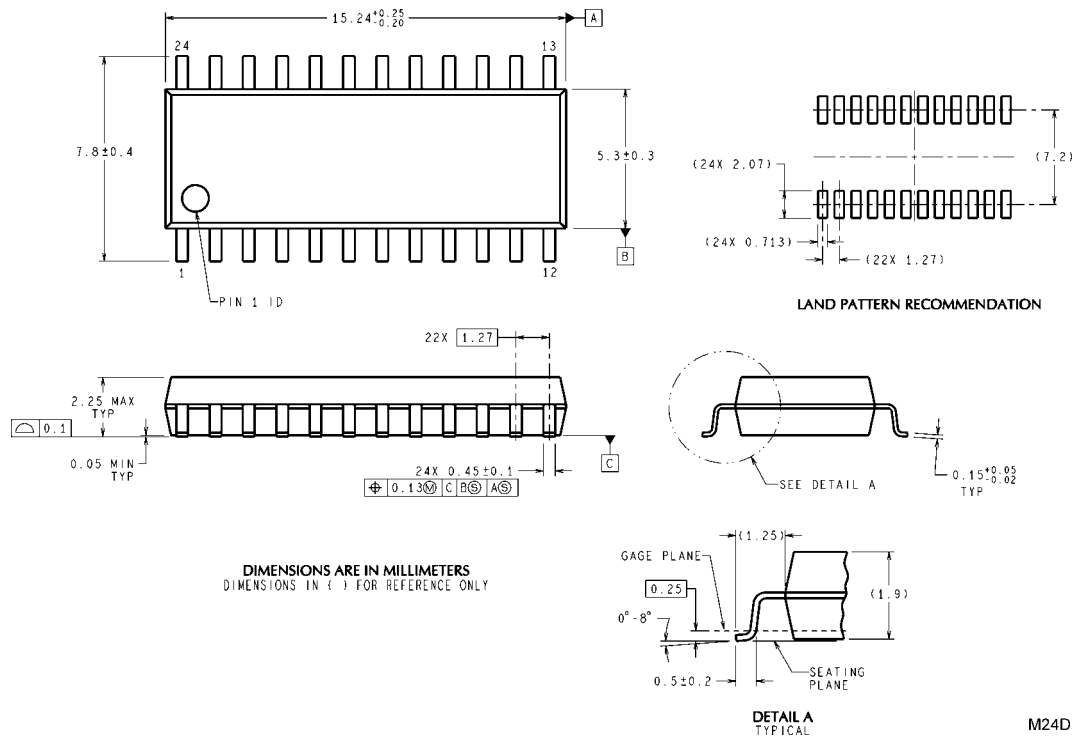


**FIGURE 7. A 5.5 MHz Low Pass filter to eliminate harmonics at the signal input. Use with maximum input frequencies of 1 MHz to 5 MHz.**



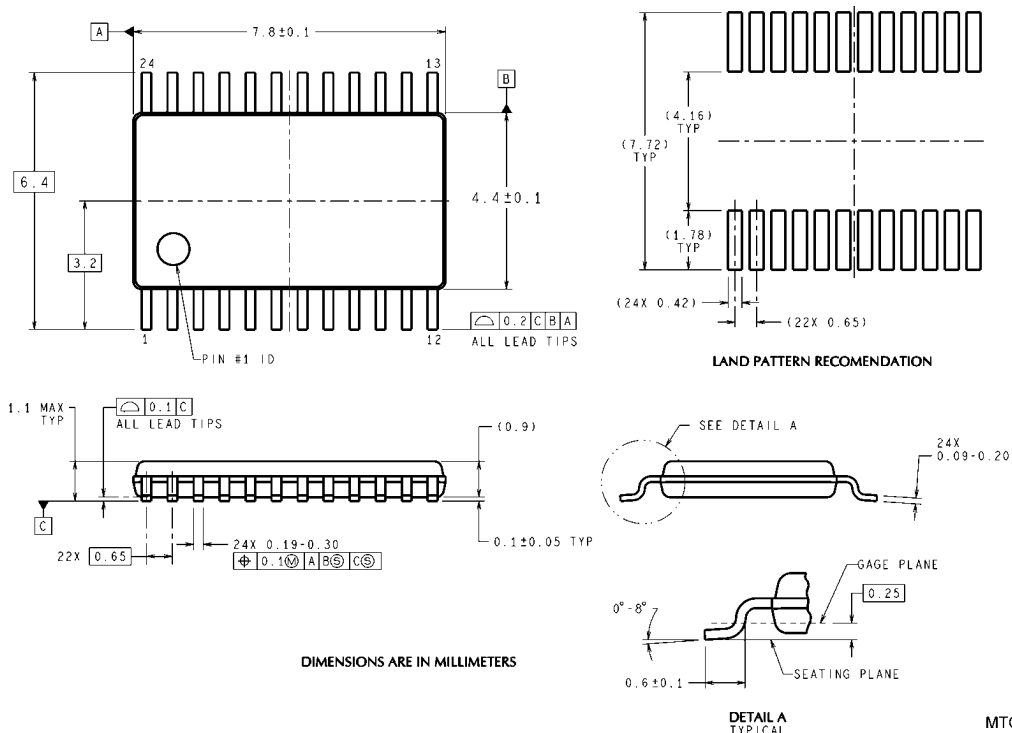
**FIGURE 8. An 11 MHz Low Pass filter to eliminate harmonics at the signal input. Use with maximum input frequencies of 5 MHz to 10 MHz**

# Physical Dimensions inches (millimeters) unless otherwise noted



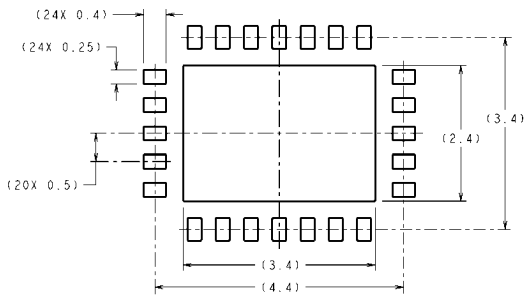
M24D (Rev B)

**24-Lead Package JM**  
**Order Number ADC1175-50CIJM**  
**Product in the SOIC (EIAJ) package is obsolete. Shown for reference only.**  
**NS Package Number M24D**

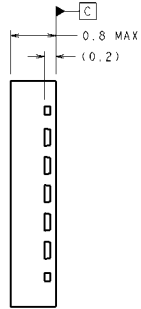
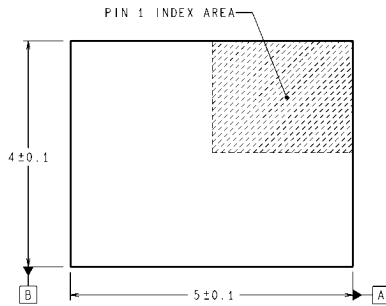


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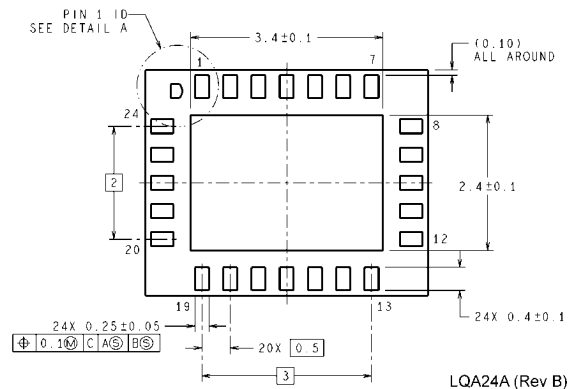
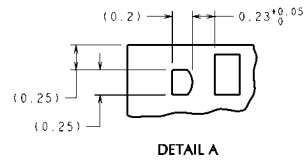
**24-Lead Package TC**  
**Order Number ADC1175-50CIMT**  
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