

# ADC80MAH-12

## Monolithic 12-Bit ANALOG-TO-DIGITAL CONVERTER

### FEATURES

- INDUSTRY-STANDARD 12-BIT ADC
- MONOLITHIC CONSTRUCTION
- LOW COST
- $\pm 0.012\%$  LINEARITY
- $25\mu\text{s}$  max CONVERSION TIME
- $\pm 12\text{V}$  OR  $\pm 15\text{V}$  OPERATION
- NO MISSING CODES:  $-25^\circ\text{C}$  to  $+85^\circ\text{C}$
- HERMETIC 32-PIN PACKAGE
- PARALLEL OR SERIAL OUTPUTS
- $705\text{mW}$  max DISSIPATION

### DESCRIPTION

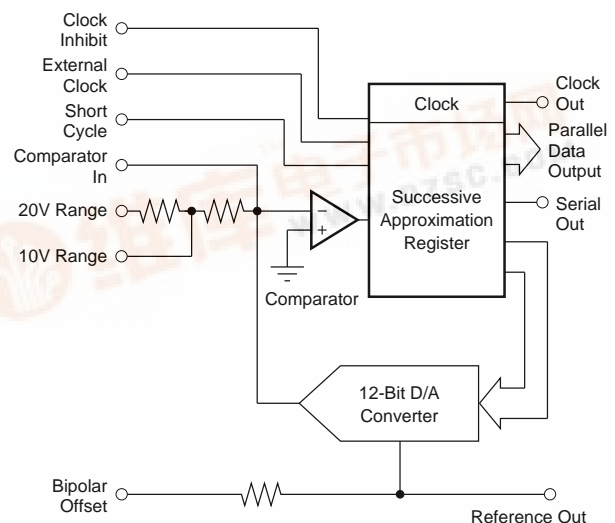
The ADC80MAH-12 is a 12-bit single-chip successive-approximation analog-to-digital converter for low cost converter applications. It is complete with a comparator, a 12-bit DAC which includes a 6.3V reference laser-trimmed for minimum temperature coefficient, a successive approximation register (SAR), clock, and all other associated logic functions.

Internal scaling resistors are provided for the selection of analog input signal ranges of  $\pm 2.5\text{V}$ ,  $\pm 5\text{V}$ ,  $\pm 10\text{V}$ , 0 to  $+5\text{V}$ , or 0 to  $+10\text{V}$ . Gain and offset errors may be externally trimmed to zero, enabling initial end-point accuracies of better than  $\pm 0.12\%$  ( $\pm 1/2\text{LSB}$ ).

The maximum conversion time of  $25\mu\text{s}$  makes the ADC80MAH-12 ideal for a wide range of 12-bit applications requiring system throughput sampling rates up to  $40\text{kHz}$ . In addition, this A/D converter may be short-cycled for faster conversion speed with reduced resolution, and an external clock may be used to synchronize the converter to the system clock or to obtain higher-speed operation. The convert command

circuits have been redesigned to allow simplified free-running operation with internal or external clock.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are TTL/LSTTL-compatible, with internal pull-up resistors included on all digital inputs to eliminate the need for external pull-up resistors on digital inputs not requiring connection. The ADC80MAH-12 operates equally well with either  $\pm 15\text{V}$  or  $\pm 12\text{V}$  analog power supplies, and also requires use of a  $+5\text{V}$  logic power supply. However, unlike many ADC80-type products, a  $+5\text{V}$  analog power supply is not required. It is packaged in a hermetic 32-pin side-braced ceramic dual-in-line package.



# SPECIFICATIONS

## ELECTRICAL

At  $T_A = +25^\circ\text{C}$ ,  $\pm V_{CC} = 12\text{V}$  or  $15\text{V}$ ,  $V_{DD} = +5\text{V}$ , unless otherwise specified.

PARAMETER	ADC80MAH-12			UNITS
	MIN	TYP	MAX	
<b>RESOLUTION</b>	12			Bits
<b>INPUT</b>				
<b>ANALOG</b>				
Voltage Ranges: Unipolar		0 to +5, 0 to +10		V
Bipolar		$\pm 2.5, \pm 5, \pm 10$		V
Impedance: 0 to +5V, $\pm 2.5\text{V}$	2.45	2.5	2.55	k $\Omega$
0 to +10V, $\pm 5\text{V}$	4.9	5	5.1	k $\Omega$
$\pm 10\text{V}$	9.8	10	10.2	k $\Omega$
<b>DIGITAL</b>				
Logic Characteristics (Over specification temperature range)				
$V_{IH}$ (Logic "1")	2		5.5	V
$V_{IL}$ (Logic "0")	-0.3		+0.8	V
$I_{IH}$ ( $V_{IN} = +2.7\text{V}$ )			20	$\mu\text{A}$
$I_{IL}$ ( $V_{IN} = +0.4\text{V}$ )	-20			$\mu\text{A}$
Convert Command Pulse Width <sup>(1)</sup>	100ns		20	$\mu\text{s}$
<b>TRANSFER CHARACTERISTICS</b>				
<b>ACCURACY</b>				
Gain Error <sup>(2)</sup>		$\pm 0.01$	$\pm 0.3$	% of FSR <sup>(3)</sup>
Offset Error <sup>(2)</sup> : Unipolar		$\pm 0.05$	$\pm 0.2$	% of FSR
Bipolar		$\pm 0.1$	$\pm 0.3$	% of FSR
Linearity Error			$\pm 0.012$	% of FSR
Differential Linearity Error		$\pm 1/2$	$\pm 3/4$	LSB
Inherent Quantization Error		$\pm 1/2$		LSB
<b>POWER SUPPLY SENSITIVITY</b>				
$11.4\text{V} \leq \pm V_{CC} \leq 16.5\text{V}$		$\pm 0.003$	$\pm 0.009$	% of FSR/ $\%V_{CC}$
$+4.5\text{V} \leq \pm V_{DD} \leq +5.5\text{V}$		$\pm 0.002$	$\pm 0.005$	% of FSR/ $\%V_{DD}$
<b>DRIFT</b>				
Total Accuracy, Bipolar <sup>(4)</sup>		$\pm 10$	$\pm 23$	ppm/ $^\circ\text{C}$
Gain		$\pm 15$	$\pm 30$	ppm/ $^\circ\text{C}$
Offset: Unipolar		$\pm 3$		ppm of FSR/ $^\circ\text{C}$
Bipolar		$\pm 7$	$\pm 15$	ppm of FSR/ $^\circ\text{C}$
Linearity Error Drift		$\pm 1$	$\pm 3$	ppm of FSR/ $^\circ\text{C}$
Differential Linearity over Temperature Range			$\pm 3/4$	LSB
No Missing Code Temperature Range	-25		$\pm 85$	$^\circ\text{C}$
Monotonicity Over Temperature Range		Guaranteed		
<b>CONVERSION TIME<sup>(5)</sup></b>		22	25	$\mu\text{s}$
<b>OUTPUT</b>				
<b>DIGITAL</b> (Bits 1-12, Clock Out, Status, Serial Out)				
Output Codes <sup>(6)</sup>				
Parallel: Unipolar		CSB		
Bipolar		COB, CTC		
Serial (NRZ) <sup>(7)</sup>		CSB, COB		
Logic Levels: Logic 0 ( $I_{SINK} \leq 3.2\text{mA}$ )			+0.4	V
Logic 1 ( $I_{SOURCE} \leq 80\mu\text{A}$ )	+2.4			V
Internal Clock Frequency		520		kHz
<b>INTERNAL REFERENCE VOLTAGE</b>				
Voltage	+6.20	+6.3	+6.40	V
Source Current Available for External Loads <sup>(8)</sup>	200			$\mu\text{A}$
Temperature Coefficient		$\pm 10$	$\pm 30$	ppm/ $^\circ\text{C}$

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# SPECIFICATIONS (CONT)

## ELECTRICAL

At  $T_A = +25^\circ\text{C}$ ,  $\pm V_{CC} = 12\text{V}$  or  $15\text{V}$ ,  $V_{DD} = +5\text{V}$ , unless otherwise specified.

PARAMETER	ADC80MAH-12			UNITS
	MIN	TYP	MAX	
<b>POWER SUPPLY REQUIREMENTS</b>				
Rated Supply Voltages		+5, $\pm 12$ or $\pm 15$		V
Supply Ranges: $\pm V_{CC}$	$\pm 11.4$		+16.5	V
$V_{DD}$	+4.5		+5.5	V
Supply Drain: $+I_{CC}$ ( $+V_{CC} = 15\text{V}$ )		8.5	11	mA
$-I_{CC}$ ( $-V_{CC} = 15\text{V}$ )		21	24	mA
$I_{DD}$ ( $V_{CC} = 5\text{V}$ )		30	36	mA
Power Dissipation ( $\pm V_{CC} = 15\text{V}$ , $V_{DD} = 5\text{V}$ )		593	705	mW
Thermal Resistance, $\theta_{JA}$		50		$^\circ\text{C}/\text{W}$
<b>TEMPERATURE RANGE</b> (Ambient)				
Specification	-25		+85	$^\circ\text{C}$
Operating (derated specs)	-55		+125	$^\circ\text{C}$
Storage	-65		+150	$^\circ\text{C}$

NOTES: (1) Accurate conversion will be obtained with any convert command pulse width of greater than 100ns; however, it must be limited to 20 $\mu\text{s}$  (max) to assure the specified conversion time. (2) Gain and offset errors are adjustable to zero. See "Optional External Gain and Offset Adjustment" section. (3) FSR means Full-Scale Range and is 20V for  $\pm 10\text{V}$  range, 10V for  $\pm 5\text{V}$  and 0 to +10V ranges, etc. (4) Includes drift due to linearity, gain, and offset drifts. (5) Conversion time is specified using internal clock. For operation with an external clock see "Clock Options" section. This converter may also be short-cycled to less than 12-bit resolution for shorter conversion time; see "Short Cycle Feature" section. (6) CSB means Complementary Straight Binary, COB means Complementary Offset Binary, and CTC means Complementary Two's Complement coding. See Table I for additional information. (7) NRZ means Non-Return-to-Zero coding. (8) External loading must be constant during conversion, and must not exceed 200 $\mu\text{A}$  for guaranteed specification.

## ABSOLUTE MAXIMUM RATINGS PCM1760

$+V_{CC}$ to Analog Common .....	0 to +16.5V
$-V_{CC}$ to Analog Common .....	0 to -16.5V
$V_{DD}$ to Digital Common .....	0 to +7V
Analog Common to Digital Common .....	$\pm 0.5\text{V}$
Logic Inputs (Convert Command, Clock In) to Digital Common .....	-0.3V to $+V_{CC}$
Analog Inputs (Analog In, Bipolar Offset) to Analog Common .....	$\pm 16.5\text{V}$
Reference Output .....	Indefinite Short to Common, Momentary Short to $V_{CC}$
Lead Temperature, (soldering, 10s) .....	+300 $^\circ\text{C}$
Maximum Junction Temperature .....	+160 $^\circ\text{C}$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION

MODEL	RESOLUTION (Bits)
ADC80MAH-12	12
BURN-IN SCREENING OPTION	
MODEL	BURN-IN TEMPERATURE (160h) <sup>(1)</sup>
ADC80MAH-12-BI	12

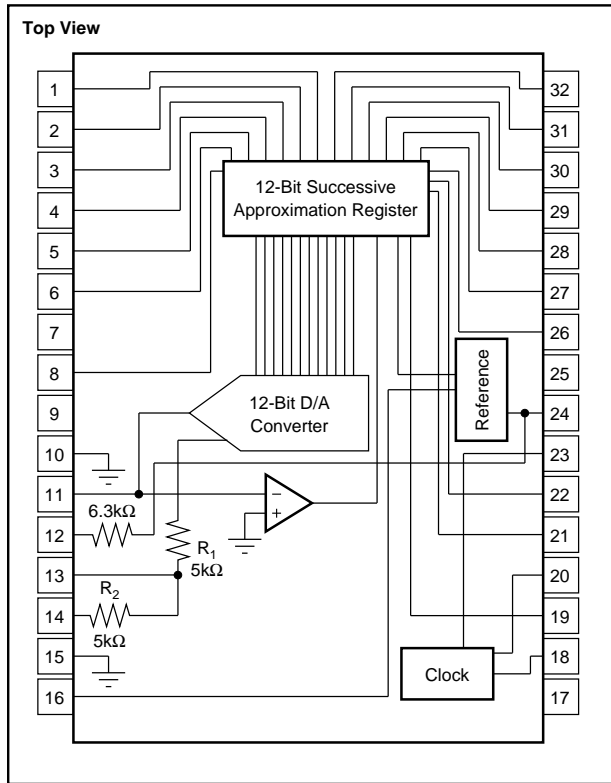
NOTE: (1) Or equivalent.

## PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER <sup>(1)</sup>
ADC80MAH-12	32-Pin Hermetic	212

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

## CONNECTION DIAGRAM



## PIN ASSIGNMENTS

PIN	DESCRIPTION	PIN	DESCRIPTION
1	Bit 6	32	Bit 7
2	Bit 5	31	Bit 8
3	Bit 4	30	Bit 9
4	Bit 3	29	Bit 10 (LSB-10 Bits)
5	Bit 2	28	Bit 11
6	Bit 1 (MSB)	27	Bit 12 (LSB-12 Bits)
7	NC <sup>(1)</sup>	26	Serial Out
8	Bit 1 (MSB)	25	-V <sub>CC</sub>
9	+5V Digital Supply	24	Reference Out (+6.3V)
10	Digital Common	23	Clock Out
11	Comparator In	22	Status
12	Bipolar Offset	21	Short Cycle
13	R <sub>1</sub> 10V Range	20	Clock Inhibit
14	R <sub>2</sub> 20V Range	19	External Clock
15	Analog Common	18	Convert Command
16	Gain Adjust	17	+V <sub>CC</sub>

NOTE: (1) +5V applied to pin 7 has no effect on circuit.

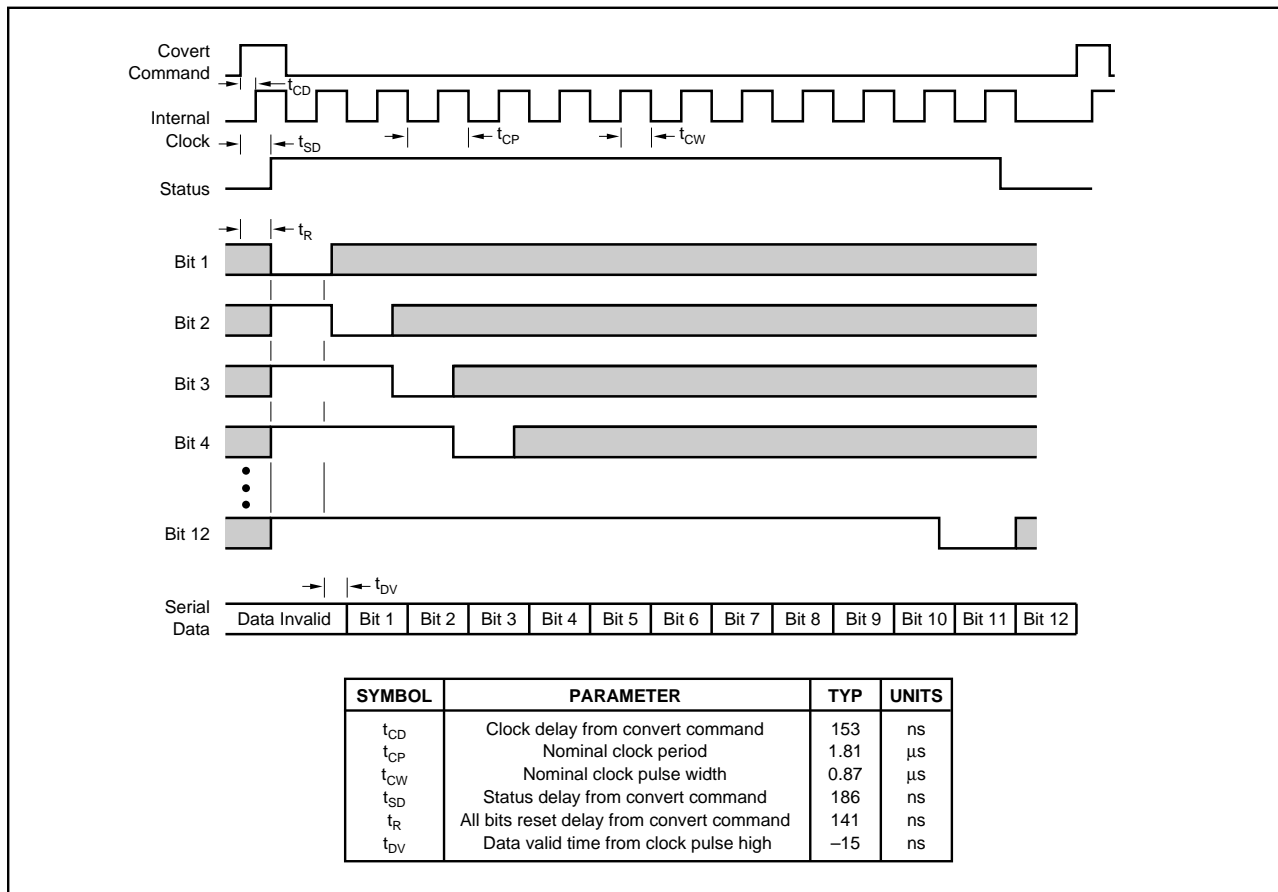


FIGURE 1. Timing Diagram (nominal values at +25°C with internal clock).