Low Capacitance, Triple/Quad SPDT ±15 V/+12 V *i*CMOS™ Switches

ADG1233/ADG1234

FEATURES

- 1.5 pF off capacitance
- 0.5 pC charge injection
- 33 V supply range
- 120 Ω on resistance
- Fully specified at ±15 V/+12 V
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 16-lead TSSOP, 20-lead TSSOP, and 4 mm × 4 mm LFCSP
- Typical power consumption (<0.03 µW)

APPLICATIONS

- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Communication systems

GENERAL DESCRIPTION

The ADG1233 and ADG1234 are monolithic *i*CMOS analog switches comprising three independently selectable single-pole, double throw SPDT switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. An $\overline{EN}$ input on the ADG1233 and ADG1234 is used to enable or disable the device. When disabled, all channels are switched off.

The *i*CMOS (industrial-CMOS) modular manufacturing process combines a high voltage complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lowered power consumption, and reduced package size.

The ultralow capacitance and charge injection of these multiplexers make them ideal solutions for data acquisition and sample-and-hold applications, where low glitch and fast settling are required.

FUNCTIONAL BLOCK DIAGRAMS

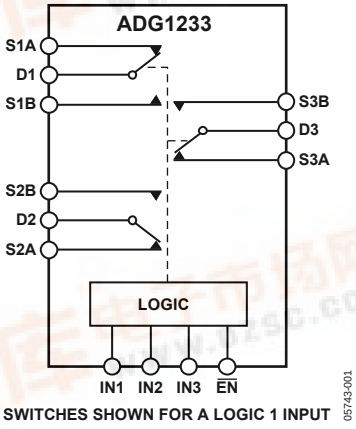

Figure 1.

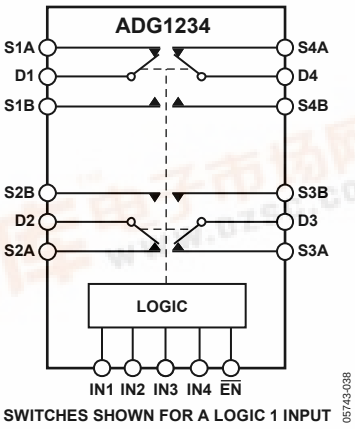

Figure 2.

Fast switching speed coupled with high signal bandwidth make the parts suitable for video signal switching. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 1.5 pF off capacitance (±15 V supply).
2. 0.5 pC charge injection.
3. 3 V logic-compatible digital input, V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. 16-lead TSSOP, 20-lead TSSOP, and 4 mm × 4 mm LFCSP.

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REVISION HISTORY

8/06—Rev. 0 to Rev. A

Updated Format……Universal
Changes to Table 1……3
Changes to Table 2……4
Changes to Figure 11……10
Changes to Figure 12……11

1/06—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	Y Version[1] +25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	120			Ω typ	V_S = ±10 V, I_S = −1 mA; see Figure 24
	190	230	260	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels (ΔR_{ON})	3.5			Ω typ	V_S = ±10 V, I_S = −1 mA
	6	10	12	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	20			Ω typ	V_S = −5 V, 0 V, +5 V; I_S = −1 mA
	60	72	79	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage I_S (Off)	±0.02			nA typ	V_D = ±10 V, V_S = −10 V; see Figure 25
	±0.1	±0.6	±1	nA max	
Drain Off Leakage I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 25
	±0.1	±0.6	±1	nA max	
Channel On Leakage I_D, I_S (On)	±0.02			nA typ	V_S = V_D = ±10 V; see Figure 26
	±0.2	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current					
I_{INL} or I_{INH}	±0.005			μA typ	V_{IN} = V_{INL} or V_{INH}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[2]					
$t_{TRANSITION}$	110			ns typ	R_L = 300 Ω, C_L = 35 pF
	130	150	170	ns max	V_S = 10 V; see Figure 27
t_{BBM}	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = +10 V; see Figure 28
t_{ON} ($\overline{EN}$)	120			ns typ	R_L = 300 Ω, C_L = 35 pF
	140	170	195	ns max	V_S = 10 V; see Figure 29
t_{OFF} ($\overline{EN}$)	40			ns typ	R_L = 300 Ω, C_L = 35 pF
	45	55	60	ns max	V_S = 10 V; see Figure 29
Charge Injection	0.5			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 30
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33
Total Harmonic Distortion, THD + N	0.14			% typ	R_L = 10 kΩ, 5 V rms, f = 20 Hz to 20 kHz; see Figure 34
−3 dB Bandwidth	900			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 32
C_S (Off)	1.5			pF typ	f = 1 MHz; V_S = 0 V
	1.7			pF max	f = 1 MHz; V_S = 0 V
C_D (Off)	1.6			pF typ	f = 1 MHz; V_S = 0 V
	1.8			pF max	f = 1 MHz; V_S = 0 V
C_D, C_S (On)	3.5			pF typ	f = 1 MHz; V_S = 0 V
	4			pF max	f = 1 MHz; V_S = 0 V

Parameter	Y Version[1] +25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	260			µA typ	Digital inputs = 5 V
			420	µA max	
I_{SS}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{SS}	0.002			µA typ	Digital inputs = 5 V
			1.0	µA max	
V_{DD}/V_{SS}			±5/±16.5	V min/max	GND = 0 V

[1] Temperature range for the Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	Y Version[1] +25°C	Y Version[1] −40°C to +85°C	Y Version[1] −40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance (R_{ON})	300			Ω typ	V_S = 0 V to10 V, I_S = −1 mA; see Figure 24
	475	567	625	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	5			Ω typ	V_S = 0 V to10 V, I_S = −1 mA
	16	26	27	Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	60			Ω typ	V_S = 3 V, 6 V, 9 V, I_S = −1 mA
LEAKAGE CURRENTS					V_{DD} = 13.2 V
Source Off Leakage I_S (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 25
	±0.1	±0.6	±1	nA max	
Drain Off Leakage I_D (Off)	±0.02			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 25
	±0.1	±0.6	±1	nA max	
Channel On Leakage I_D, I_S (On)	±0.02			nA typ	V_S = V_D = 1 V or 10 V, see Figure 26
	±0.2	±0.6	±1	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.001			μA typ	
			±0.1	μA max	V_{IN} = V_{INL} or V_{INH}
Digital Input Capacitance, C_{IN}	2			pF typ	
DYNAMIC CHARACTERISTICS[2]					
$t_{TRANSITION}$	135			ns typ	R_L = 300 Ω, C_L = 35 pF
	170	200	230		V_S = 8 V; see Figure 27
t_{BBM}	45			ns typ	R_L = 300 Ω, C_L = 35 pF
			10	ns min	V_{S1} = V_{S2} = 8 V; see Figure 28
t_{ON} ($\overline{EN}$)	150			ns typ	R_L = 300 Ω, C_L = 35 pF
	195	230	265		V_S = 8 V; see Figure 29
t_{OFF} ($\overline{EN}$)	45			ns typ	R_L = 300 Ω, C_L = 35 pF
	60	70	75		V_S = 8 V; see Figure 29
Charge Injection	−0.3			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 30
Off Isolation	−80			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 31
Channel-to-Channel Crosstalk	−85			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 33
−3 dB Bandwidth	600			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 32
C_S (Off)	1.5			pF typ	f = 1 MHz; V_S = 6 V
	1.7			pF max	f = 1 MHz; V_S = 6 V
C_D (Off)	2			pF typ	f = 1 MHz; V_S = 6 V
	2.2			pF max	f = 1 MHz; V_S = 6 V
C_D, C_S (On)	4			pF typ	f = 1 MHz; V_S = 6 V
	4.5			pF max	f = 1 MHz; V_S = 6 V

Parameter	Y Version[1] +25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.002			µA typ	Digital inputs = 0 V or V_{DD}
			1.0	µA max	
I_{DD}	260			µA typ	Digital inputs = 5 V
			440	µA max	
V_{DD}			5/16.5	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range for the Y version: −40°C to +125°C
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	24 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Mximum)	100 mA
Operating Temperature Range	
Automotive Temperature Range (Y Version)	–40°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
TSSOP, θ_{JA}, Thermal Impedance	112°C/W
LFCSP, θ_{JA}, Thermal Impedance	30.4°C/W
Reflow Soldering Peak Temperature, Pb-Fee	260°C

[1] Overvoltages at A, $\overline{EN}$, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating is applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

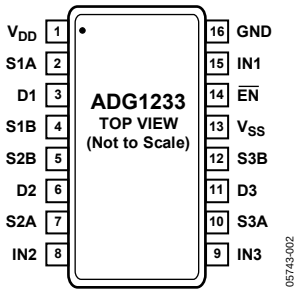


Figure 3. 16-Lead TSSOP Pin Configuration

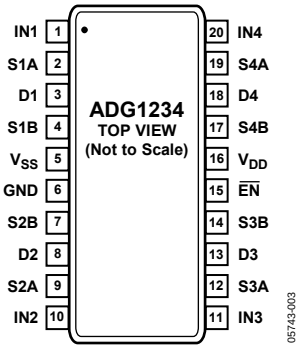


Figure 4. 20-Lead TSSOP Pin Configuration

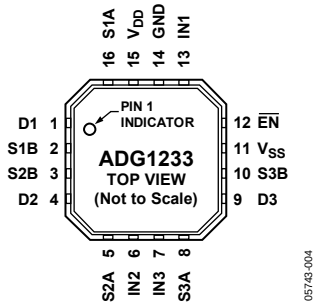


Figure 5. 16-Lead, 4 mm × 4 mm LFCSP Pin Configuration, Exposed Pad Tied to Substrate, V_{SS}

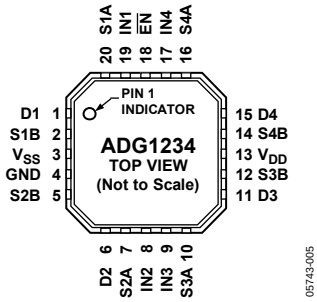


Figure 6. 20-Lead, 4 mm × 4 mm LFCSP Pin Configuration Exposed Pad Tied to Substrate, V_{SS}

Table 4. 16-Lead TSSOP/20-Lead TSSOP Pin Configurations

Pin No. ADG1233 16-Lead TSSOP	Pin No. ADG1234 20-Lead TSSOP	Mnemonic
1	16	V_{DD}
2	2	S1A
3	3	D1
4	4	S1B
5	7	S2B
6	8	D2
7	9	S2A
8	10	IN2
9	11	IN3
10	12	S3A
11	13	D3
12	14	S3B
13	5	V_{SS}
14	15	$\overline{EN}$
15	1	IN1
16	6	GND
N/A	17	S4B
N/A	18	D4
N/A	19	S4A
N/A	20	IN4

Table 5. 16-Lead LFCSP/20-Lead LFCSP Pin Configurations

Pin No. ADG1233 16-Lead LFCSP	Pin No. ADG1234 20-Lead LFCSP	Mnemonic
1	1	D1
2	2	S1B
3	5	S2B
4	6	D2
5	7	S2A
6	8	IN2
7	9	IN3
8	10	S3A
9	11	D3
10	12	S3B
11	3	V_{SS}
12	18	$\overline{EN}$
13	19	IN1
14	4	GND
15	13	V_{DD}
16	20	S1A
N/A	14	S4B
N/A	15	D4
N/A	16	S4A
N/A	17	IN4

Table 6. ADG1233/ADG1234 Truth Table

$\overline{EN}$	INx	Switch xA	Switch xB
1	X	Off	Off
0	0	Off	On
0	1	On	Off

TERMINOLOGY

V_{DD}
Most positive supply potential.

V_{SS}
Most negative power supply potential in dual supplies. In single-supply applications, it can be connected to ground.

GND
Ground (0 V) reference.

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
Difference between the R_{ON} of any two channels.

I_S (Off)
Source leakage current when switch is off.

I_D (Off)
Drain leakage current when switch is off.

I_D, I_S (On)
Channel leakage current when switch is on.

V_D, V_S
Analog voltage on Terminal D, Terminal S.

C_S (Off)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON} ($\overline{EN}$)
Delay time between the 50% and 90% points of the digital input and switch on condition.

t_{OFF} ($\overline{EN}$)
Delay time between the 50% and 90% points of the digital input and switch off condition.

$t_{TRANSITION}$
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

t_{BBM}

Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL}, I_{INH}
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of an unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
Frequency at which the output is attenuated by 3 dB.

On Response
Frequency response of the on switch.

THD + N
Ratio of the harmonic amplitude plus noise of the signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

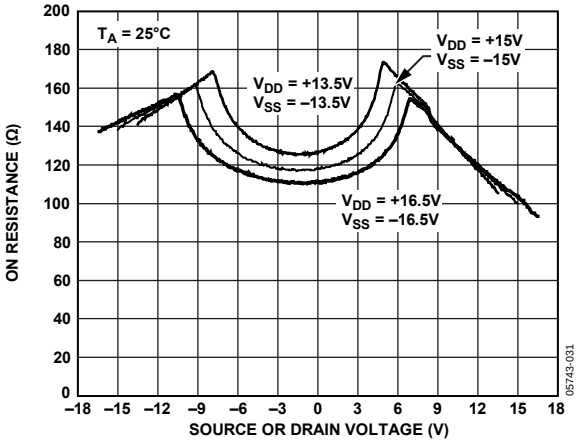


Figure 7. On Resistance as a Function of V_D (V_S) for Dual Supply

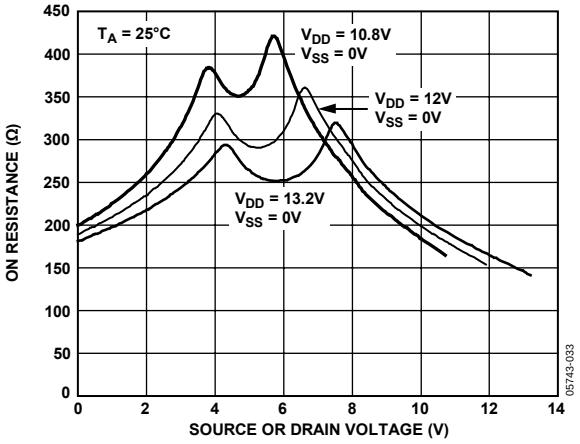


Figure 8. On Resistance as a Function of V_D (V_S) for Dual Supply

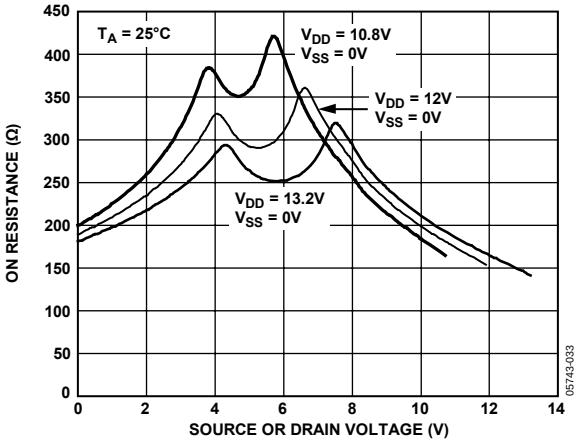


Figure 9. On Resistance as a Function of V_D (V_S) for Single Supply

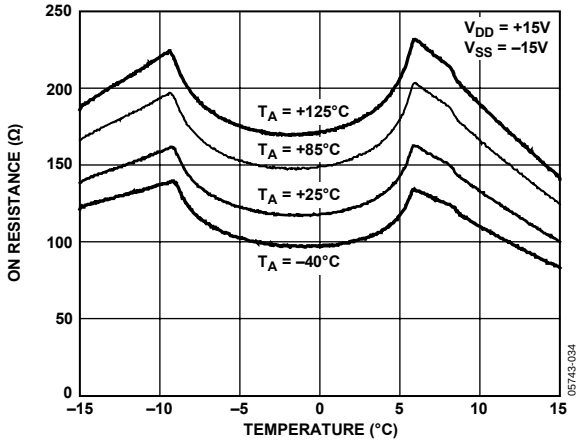


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

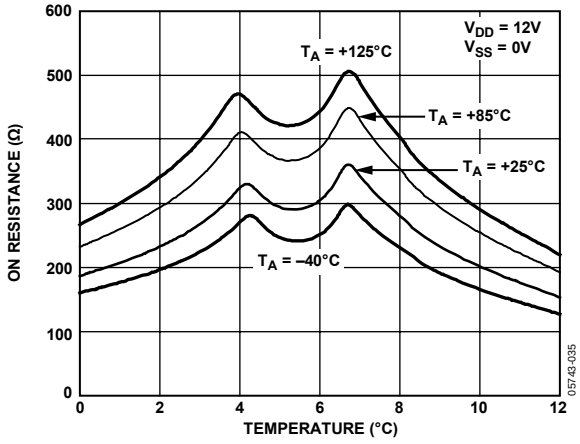


Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

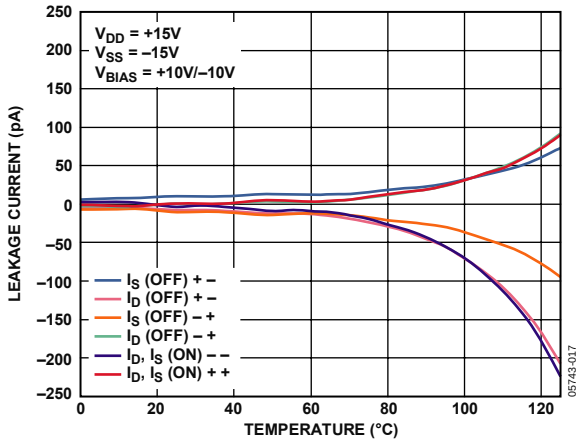


Figure 12. Leakage Currents as a Function of Temperature, Dual Supply

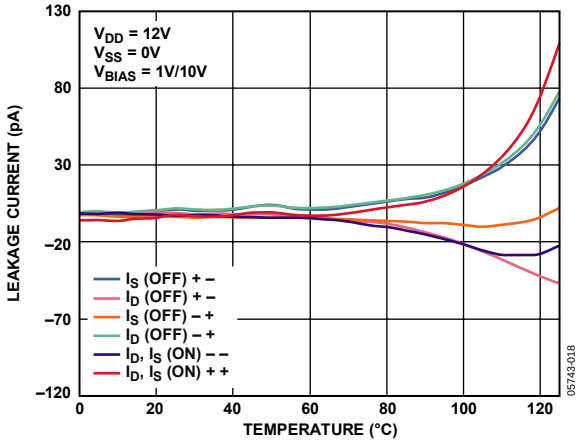


Figure 13. Leakage Currents as a Function of Temperature, Single Supply

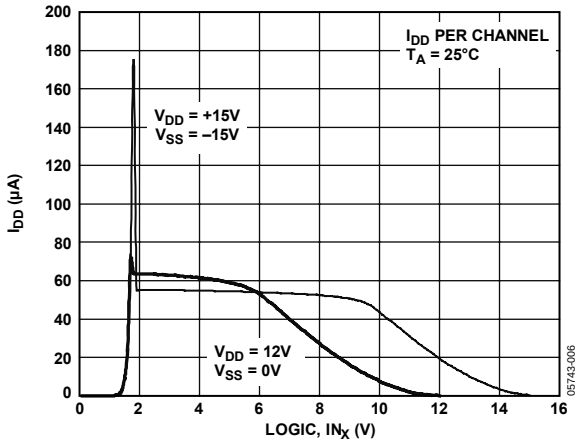


Figure 14. I_{DD} vs. Logic Level

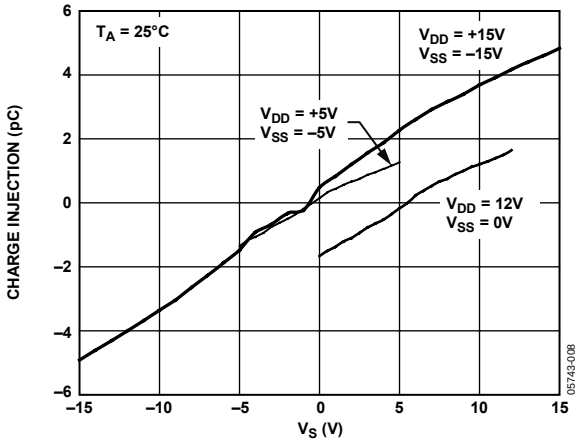


Figure 15. Charge Injection vs. Source Voltage

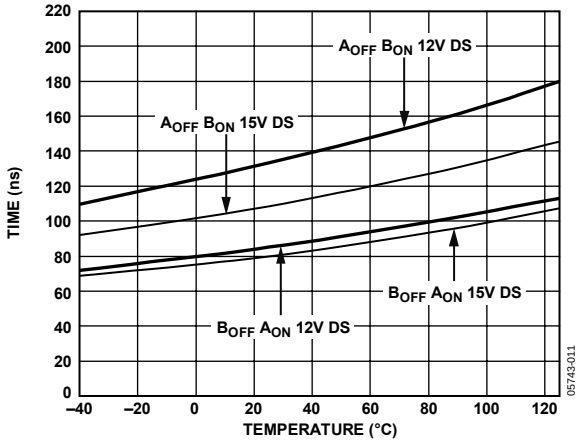


Figure 16. $t_{TRANSITION}$ vs. Temperature

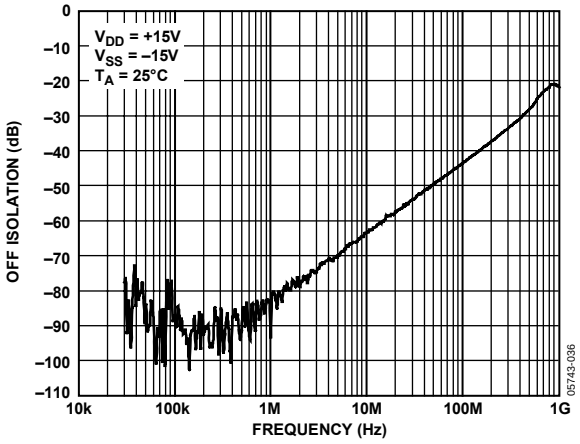


Figure 17. Off Isolation vs. Frequency

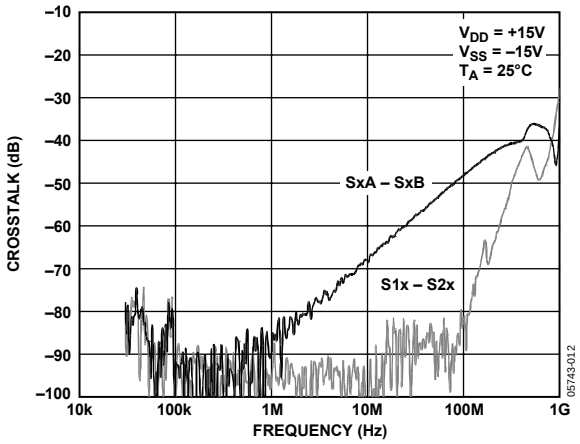


Figure 18. Crosstalk vs. Frequency

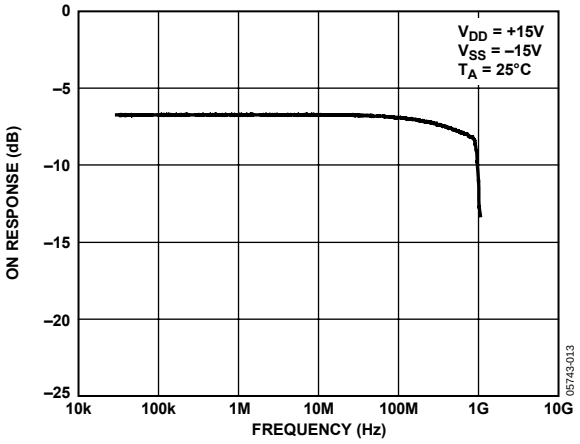


Figure 19. On Response vs. Frequency

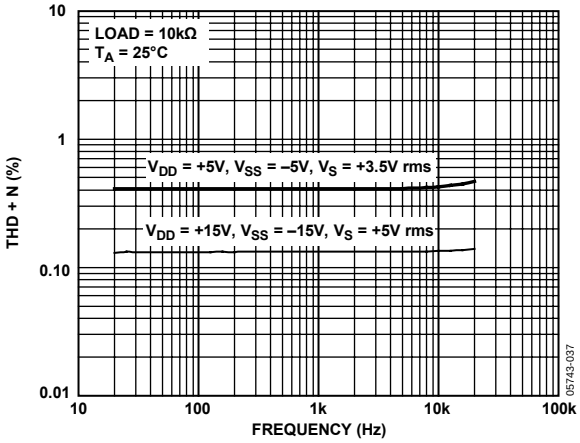


Figure 20. THD + N vs. Frequency

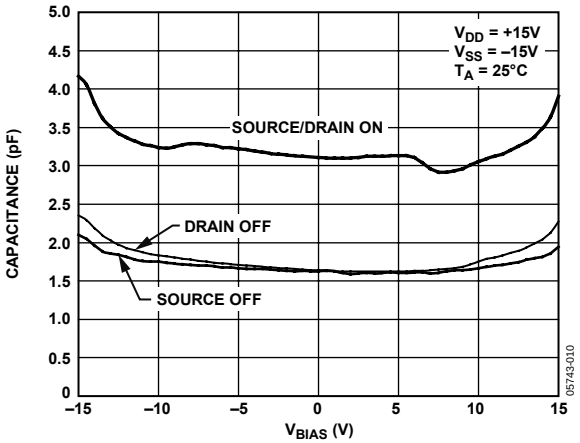


Figure 21. Capacitance vs. Source Voltage for Dual Supply

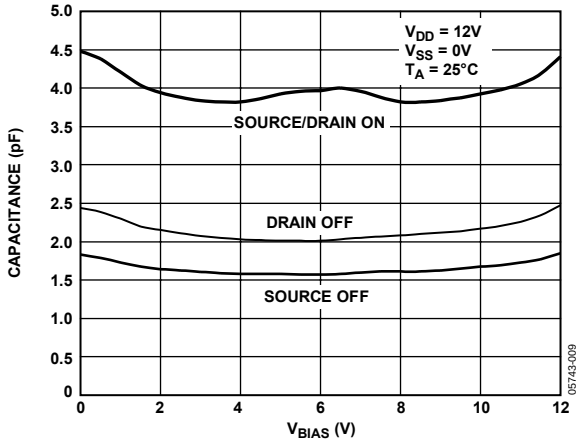


Figure 22. Capacitance vs. Source Voltage for Single Supply

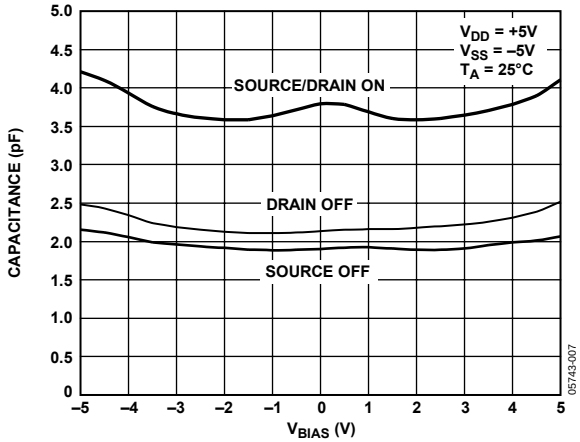


Figure 23. Capacitance vs. Source Voltage for Dual Supply

TEST CIRCUITS

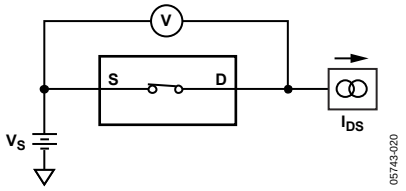


Figure 24. On Resistance

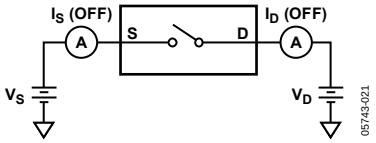


Figure 25. Off Leakage

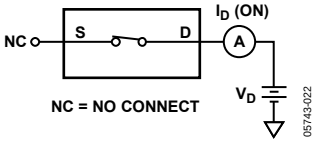


Figure 26. On Leakage

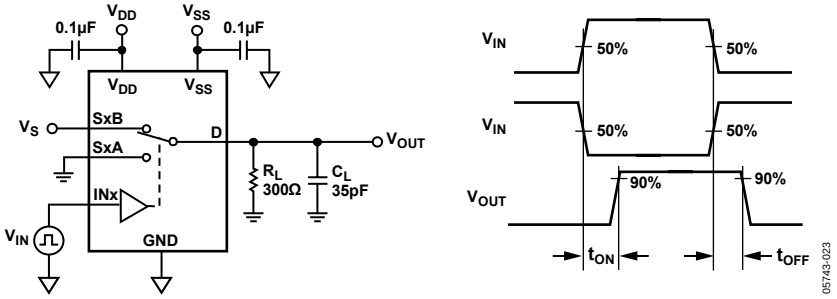


Figure 27. Switching Timing

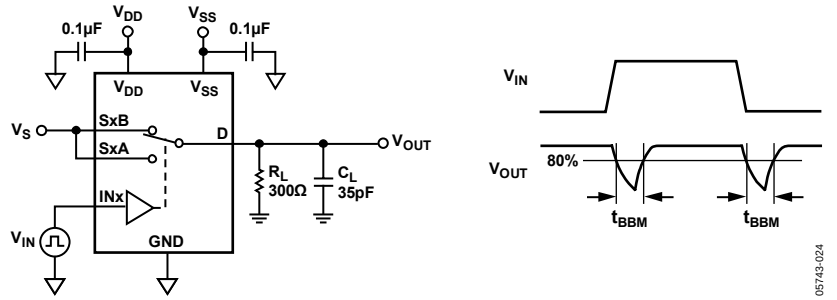


Figure 28. Break-Before-Make Delay

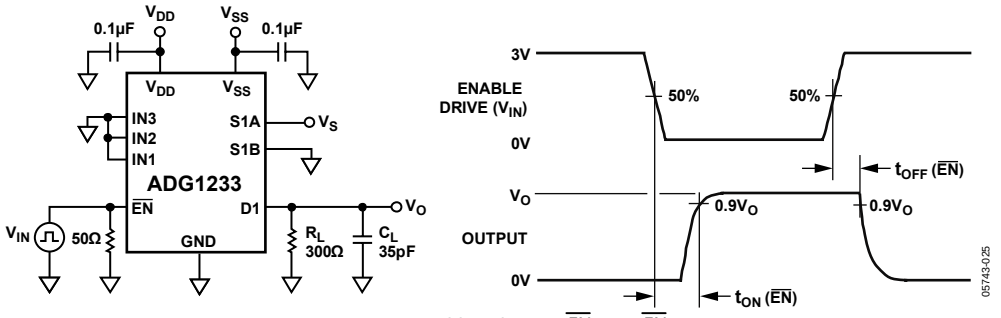


Figure 29. Enable Delay, t_{ON} ($\overline{EN}$), t_{OFF} ($\overline{EN}$)

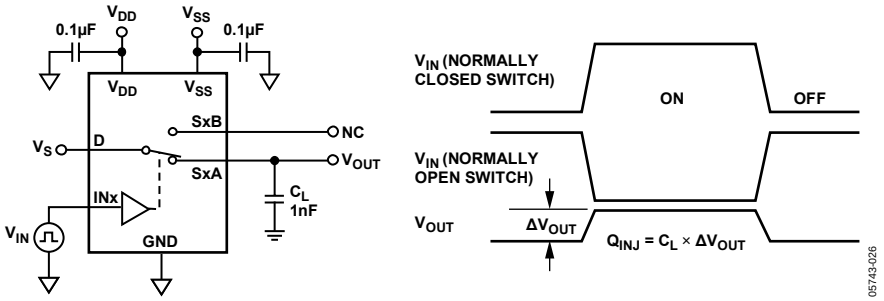


Figure 30. Charge Injection

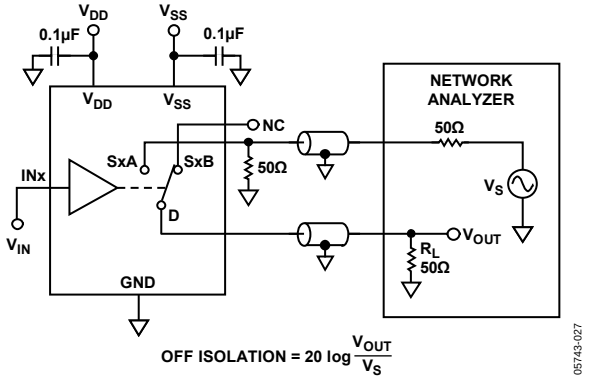


Figure 31. Off Isolation

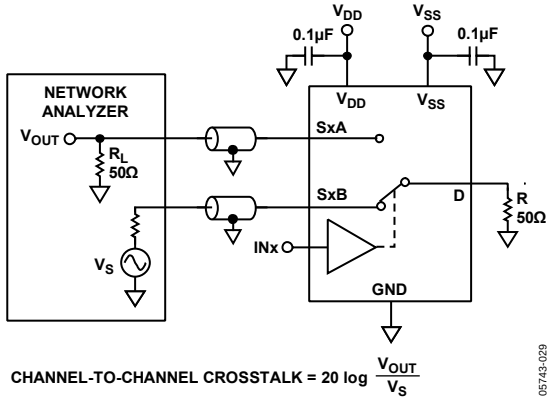


Figure 33. Channel-to-Channel Crosstalk

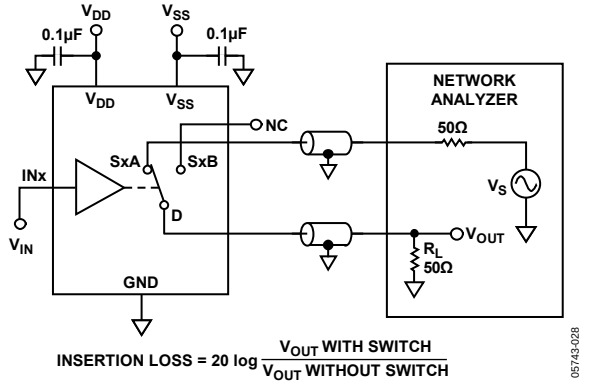


Figure 32. Bandwidth

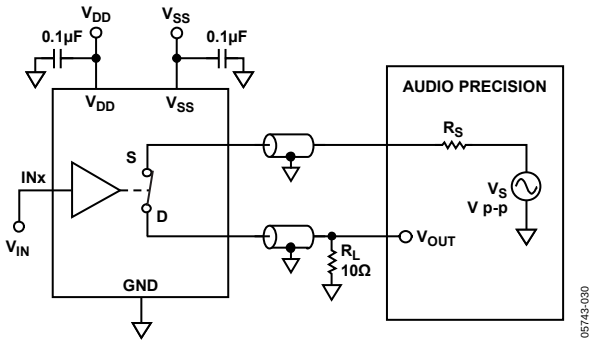
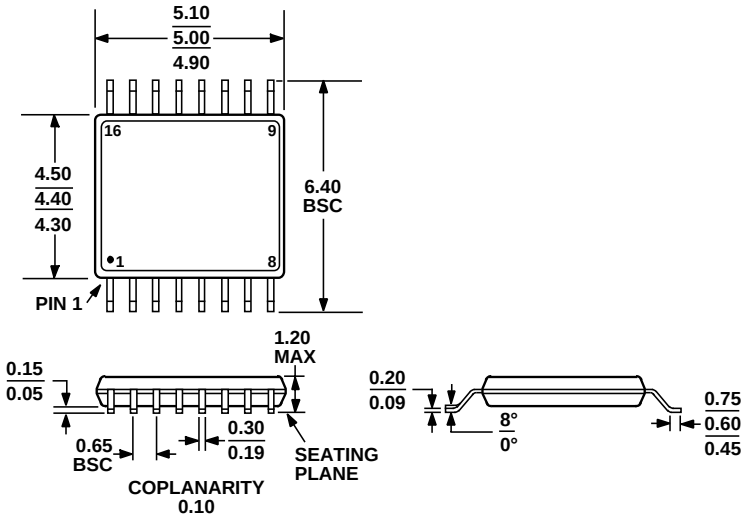


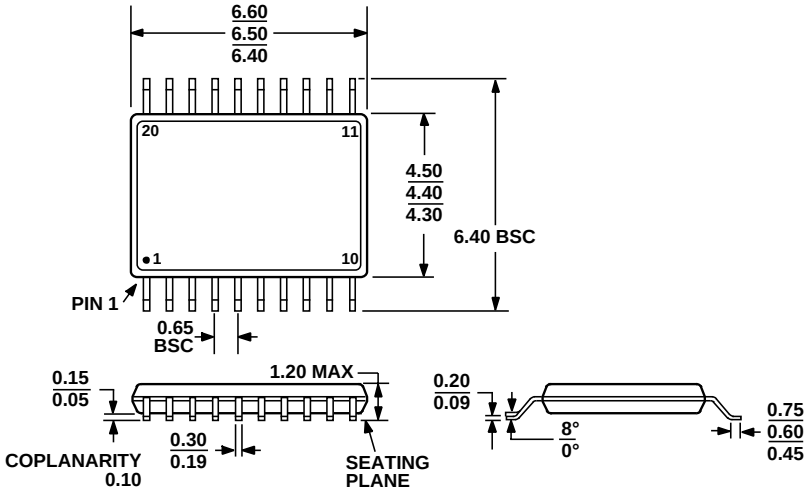
Figure 34. THD + Noise

OUTLINE DIMENSIONS



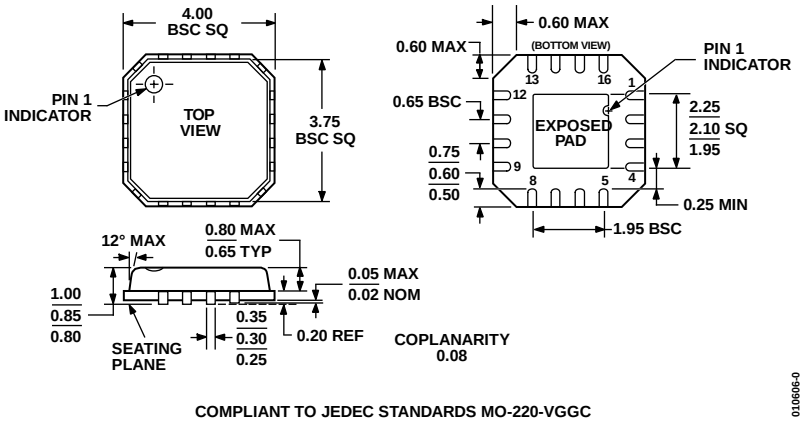
COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 35. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



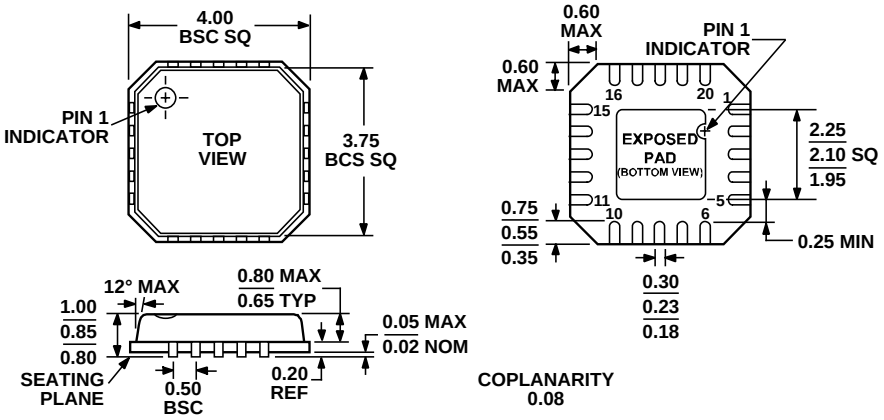
COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 36. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGC

Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 38. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG1233YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1233YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package (TSSOP)	RU-16
ADG1233YCPZ-REEL[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-4
ADG1233YCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-16-4
ADG1234YRUZ[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20
ADG1234YRUZ-REEL7[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package (TSSOP)	RU-20
ADG1234YCPZ-REEL[1]	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20-1
ADG1234YCPZ-REEL7[1]	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package (LFCSP_VQ)	CP-20-1

[1] Z = Pb-free part.

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