Quad SPDT ±15 V/+12 V Switches

ADG1334

FEATURES

- 33 V supply range
- 130 Ω on resistance
- Fully specified at ±15 V/+12 V
- 3 V logic compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 20-lead SSOP

APPLICATIONS

- Audio and video routing
- Battery-powered systems
- Signal routing

FUNCTIONAL BLOCK DIAGRAM

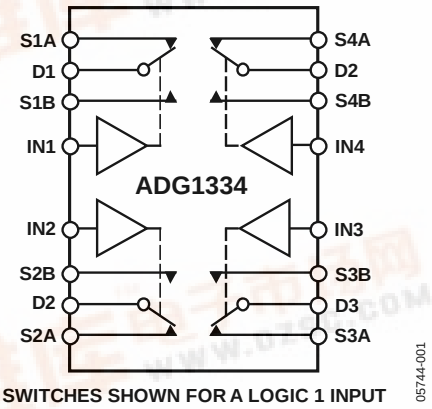

Figure 1.

GENERAL DESCRIPTION

The ADG1334 is a monolithic CMOS device comprising four independently selectable SPDT switches designed on a CMOS process.

When the switches are on, each switch conducts equally well in both directions and has an input signal range that extends to the power supplies. In the off condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is the low charge injection for minimum transients when switching the digital inputs.

Fast switching speed coupled with high signal bandwidth makes the part suitable for video signal switching. CMOS construction ensures ultra ow power dissipation, making the part ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 3 V logic compatible digital input V_{IH} = 2.0 V, V_{IL} = 0.8 V.
2. No V_L logic power supply required.
3. Low power consumption.
4. 20-lead SSOP.

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REVISION HISTORY

1/06—Revision 0: Initial Version

SPECIFICATIONS

DUAL SUPPLY[1]

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	B Version +25°C	B Version −40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	130	230	Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 11
	200		Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between Channels (ΔR_{ON})	5		Ω typ	V_S = ±10 V, I_S = −10 mA
	10		Ω max	
On Resistance Flatness ($R_{FLAT (ON)}$)	25		Ω typ	V_S = −5 V, 0 V, +5 V; I_S = −10 mA
	65		Ω max	
LEAKAGE CURRENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage I_S (Off)	±10		nA typ	V_D = ±10 V; V_S = ±10 V; see Figure 12
Drain Off Leakage I_D (Off)	±10		nA typ	V_D = ±10 V; V_S = ±10 V; see Figure 12
Channel On Leakage I_D, I_S (On)	±10		nA typ	V_S = V_D = ±10 V; see Figure 13
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	5		pF typ	
DYNAMIC CHARACTERISTICS[2]				
T_{ON}	110		ns typ	R_L = 300 Ω, C_L = 35 pF
	130	150	ns max	V_S = 10 V; see Figure 14
T_{OFF}	65		ns typ	R_L = 300 Ω, C_L = 35 pF
	85	95	ns max	V_S = 10 V; see Figure 14
T_{BBM}	25		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = +10 V; see Figure 15
Charge Injection	2		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 16
Off Isolation	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 17
Channel-to-Channel Crosstalk	85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
−3 dB Bandwidth	700		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 18
C_S (Off)	5		pF typ	f = 1 MHz; V_S = 0 V
C_D (Off)	5		pF typ	f = 1 MHz; V_S = 0 V
C_D, C_S (On)	10		pF typ	f = 1 MHz; V_S = 0 V
POWER REQUIREMENTS				V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.002		μA typ	Digital inputs = 0 V or V_{DD}
		1	μA max	
I_{DD}	260		μA typ	Digital inputs = 5 V
		400	μA max	
I_{SS}	0.002		μA typ	Digital inputs = 0 V or V_{DD}
		1	μA max	
I_{SS}	0.002		μA typ	Digital inputs = 5 V
		1	μA max	

[1] Temperature range is B Version: −40°C to +105°C.
[2] Guaranteed by design, not subject to production test.

SINGLE SUPPLY[1]

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	B Version +25°C	B Version −40°C to +105°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to V_{DD}	V	
On Resistance (R_{ON})	325	520	Ω typ	V_S = 0 V to10 V, I_S = −10 mA; see Figure 11
	500		Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	10		Ω typ	V_S = 0 V to10 V, I_S = −10 mA
	20		Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	65		Ω typ	V_S = 3 V, 6 V, 9 V, I_S = −10 mA
LEAKAGE CURRENTS				V_{DD} = 13.2 V
Source Off Leakage I_S (Off)	±10		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 12
Drain Off Leakage I_D (Off)	±10		nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V; see Figure 12
Channel On Leakage I_D, I_S (On)	±10		nA typ	V_S = V_D = 1 V or 10 V, see Figure 13
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	3		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS[2]				
T_{ON}	135		ns typ	R_L = 300 Ω, C_L = 35 pF
	170	200	ns max	V_S = 8 V; see Figure 14
T_{OFF}	95		ns typ	R_L = 300 Ω, C_L = 35 pF
	115	140	ns max	V_S = 8 V; see Figure 14
T_{BBM}	50		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 8 V; see Figure 15
Charge Injection	2		pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 16
Off Isolation	80		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 17
Channel-to-Channel Crosstalk	85		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 19
−3 dB Bandwidth	500		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 18
C_S (Off)	5		pF typ	f = 1 MHz; V_S = 6 V
C_D (Off)	5		pF typ	f = 1 MHz; V_S = 6 V
C_D, C_S (On)	10		pF typ	f = 1 MHz; V_S = 6 V
POWER REQUIREMENTS				V_{DD} = 13.2 V
I_{DD}	0.002		μA typ	Digital inputs = 0 V or V_{DD}
		1	μA max	
I_{DD}	260		μA typ	Digital inputs = 5 V
		420	μA max	

[1] Temperature range is B Version: −40°C to +105°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	24 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle max)	100 mA
Operating Temperature Range	
Industrial Temperature Range (B Version)	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
SSOP Package	
θ_{JA}, Thermal Impedance	83.2°C/W
Reflow Soldering Peak Temperature, Pb-free	260°C

[1] Overvoltages at A, EN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

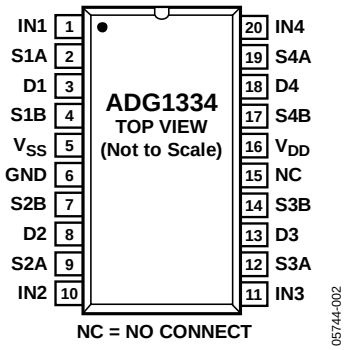


Figure 2. 20-Lead SSOP Pin Configuration

Table 4. 20-Lead SSOP Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 10, 11, 20	IN1, IN2, IN3, IN4	Logic Control Input.
2, 4, 7, 9, 12, 14, 17, 19	S1A, S1B, S2B, S2A, S3A, S3B, S4B, S4A	Source Terminal. Can be an input or output.
3, 8, 13, 18	D1, D2, D3, D4	Drain Terminal. Can be an input or output.
5	V_{SS}	Most Negative Power Supply Potential in Dual Supplies. In single-supply applications, it can be connected to ground.
6	GND	Ground (0 V) Reference.
15	NC	No Connect.
16	V_{DD}	Most Positive Power Supply Potential.

Table 5. ADG1334 Truth Table

Logic	Switch A	Switch B
0	Off	On
1	On	Off

TERMINOLOGY

R_{ON}
Ohmic resistance between D and S.

ΔR_{ON}
Difference between the R_{ON} of any two channels.

I_S (Off)
Source leakage current when switch is off.

I_D (Off)
Drain leakage current when switch is off.

I_D, I_S (On)
Channel leakage current when switch is on.

V_D (V_S)
Analog voltage on Terminal D, Terminal S.

C_S (OFF)
Channel input capacitance for off condition.

C_D (Off)
Channel output capacitance for off condition.

C_D, C_S (On)
On switch capacitance.

C_{IN}
Digital input capacitance.

t_{ON}
The delay between applying the digital control input and the output switching on (see Figure 14).

t_{OFF}
The delay between applying the digital control input and the output switching off (see Figure 14).

t_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
Frequency at which the output is attenuated by 3 dB.

On Response
Frequency response of the on switch.

TYPICAL PERFORMANCE CHARACTERISTICS

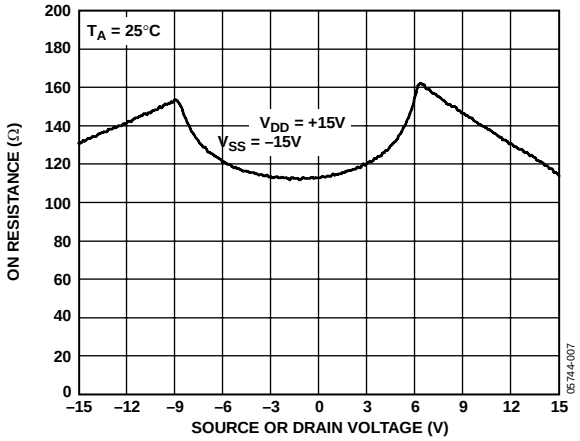


Figure 3. On Resistance as a Function of V_D (V_S) for Dual Supply

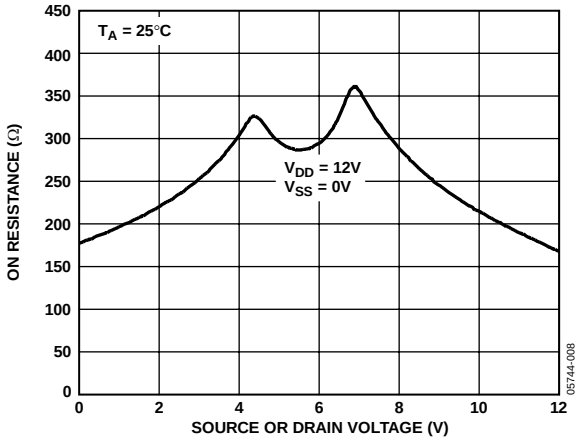


Figure 4. On Resistance as a Function of V_D (V_S) for Single Supply

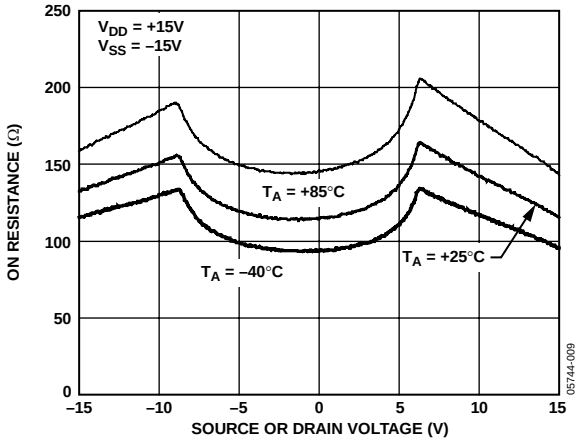


Figure 5. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

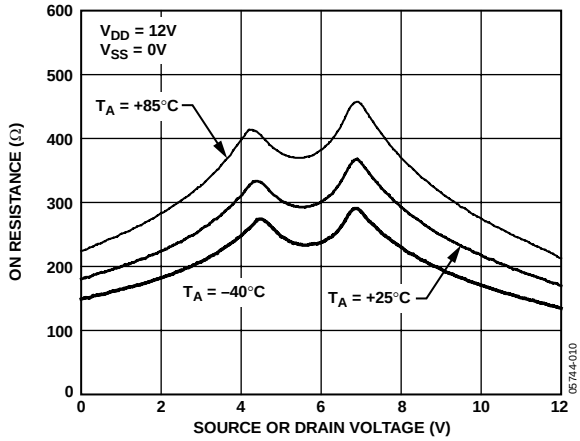


Figure 6. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

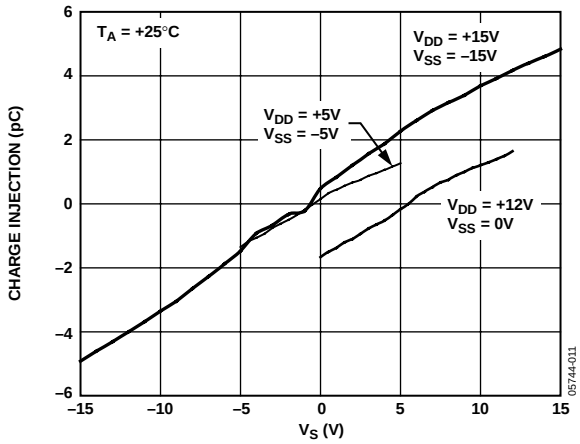


Figure 7. Charge Injection vs. Source Voltage

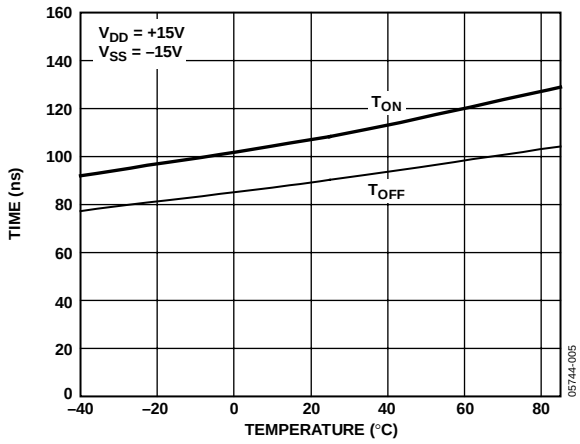


Figure 8. T_{ON}/T_{OFF} Time vs. Temperature

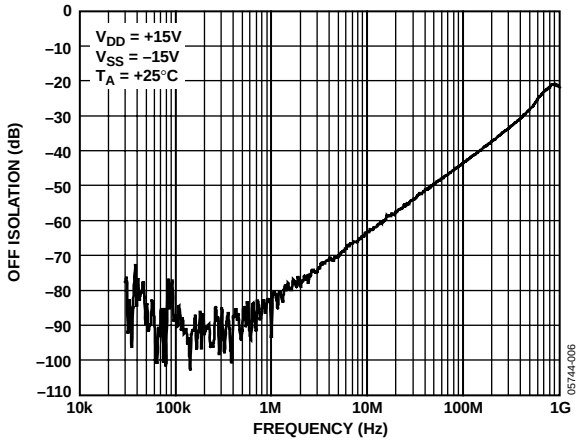


Figure 9. Off Isolation vs. Frequency

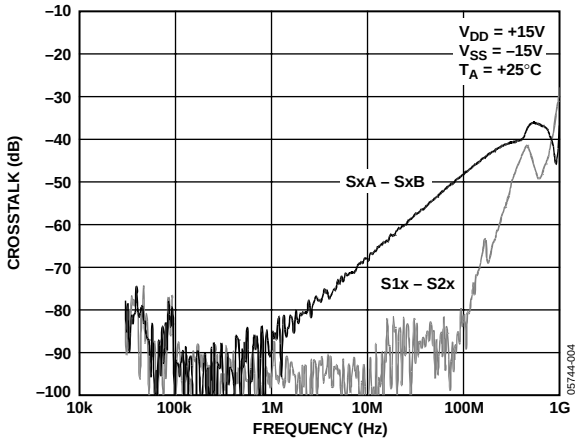


Figure 10. Crosstalk vs. Frequency

TEST CIRCUITS

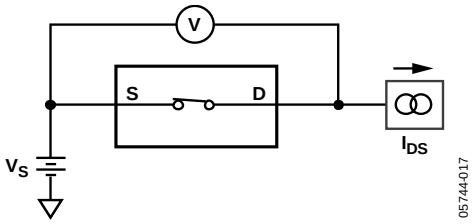


Figure 11. On Resistance

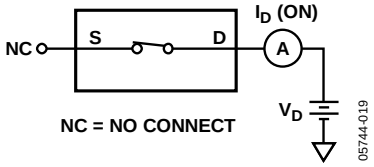


Figure 13. On Leakage

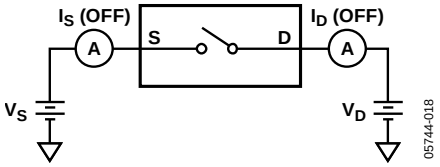


Figure 12. Off Leakage

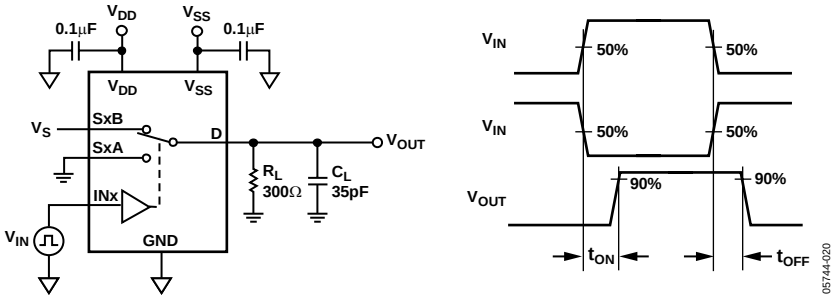


Figure 14. Switching Timing

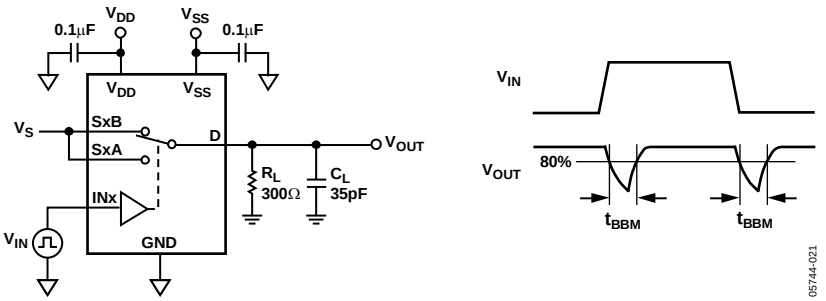


Figure 15. Break-Before-Make Delay

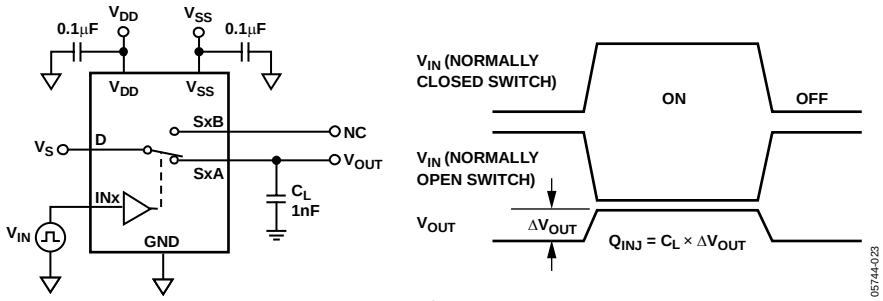


Figure 16. Charge Injection

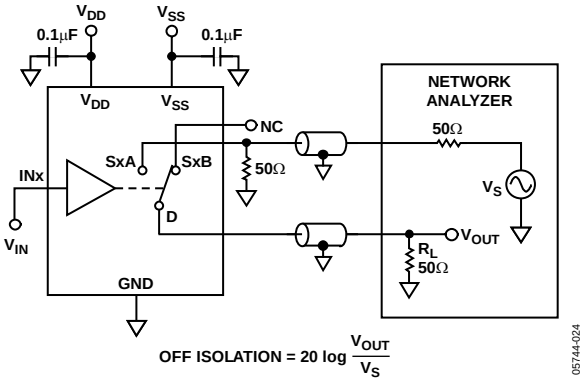


Figure 17. Off Isolation

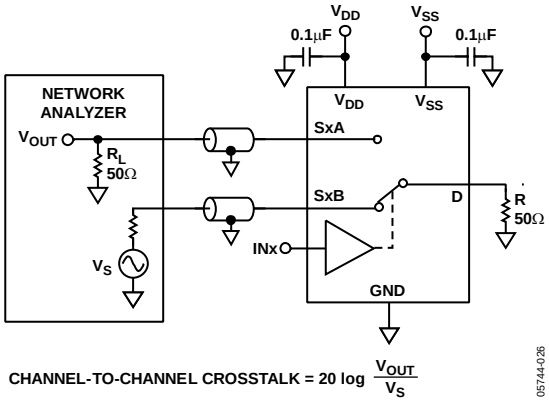


Figure 19. Channel-to-Channel Crosstalk

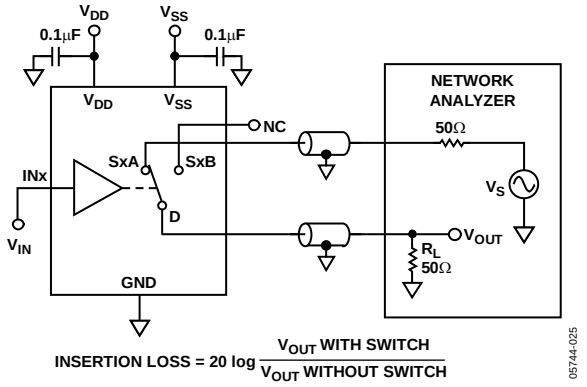
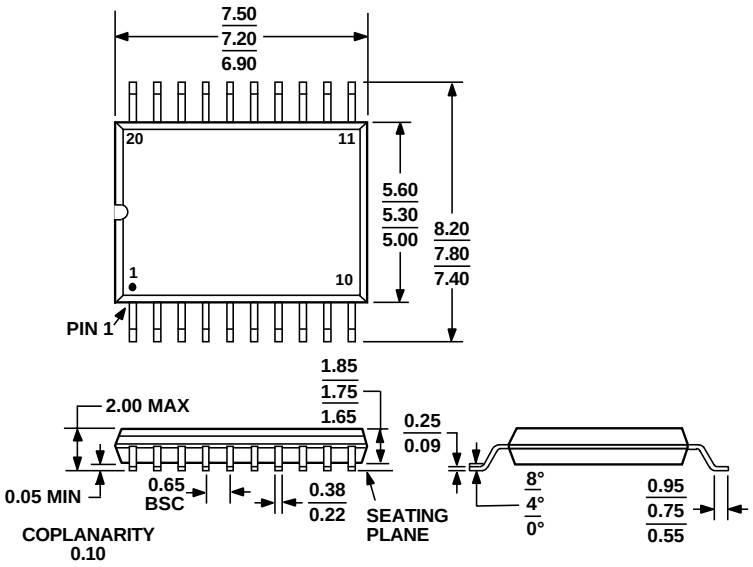


Figure 18. Bandwidth

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-150-AE

Figure 20. 20-Lead Shrink Small Outline Package [SSOP]
(RS-20)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Description	Package Option
ADG1334BRSZ[1]	−40°C to +105°C	20-Lead Shrink Small Outline Package (SSOP)	RS-20
ADG1334BRSZ-REEL[1]	−40°C to +105°C	20-Lead Shrink Small Outline Package (SSOP)	RS-20

[1] Z = Pb-free part.