# 2Ω Max On Resistance, ±15 V/12 V/±5 V *i*CMOS™ Quad SPST Switch

Preliminary Technical Data

# ADG1411/ADG1412/ADG1413

## FEATURES

**2Ω Max On Resistance**
**0.5Ω Max On Resistance Flatness**
**200mA continuous current per channel**
**33 V supply range**
**Fully specified at +12 V, ±15 V, ±5 V**
**No $V_L$ supply required**
**3 V logic-compatible inputs**
**Rail-to-rail operation**
**16-lead TSSOP and 16-lead LFCSP**
**Typical power consumption: <0.03 µW**

## APPLICATIONS

**Automatic test equipment**
**Data aquisition systems**
**Battery-powered systems**
**Sample-and-hold systems**
**Audio signal routing**
**Video signal routing**
**Communication systems**
**Relay Replacement**

## GENERAL DESCRIPTION

The ADG1411/ADG1412/ADG1413 are monolithic complementary metal-oxide semiconductor (CMOS) devices containing four independently selectable switches designed on an *i*CMOS process. *i*CMOS (industrial CMOS) is a modular manufacturing process combining high voltage CMOS and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no previous generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The on resistance profile is very flat over the full analog input range ensuring excellent linearity and low distortion when switching audio signals.

## FUNCTIONAL BLOCK DIAGRAM

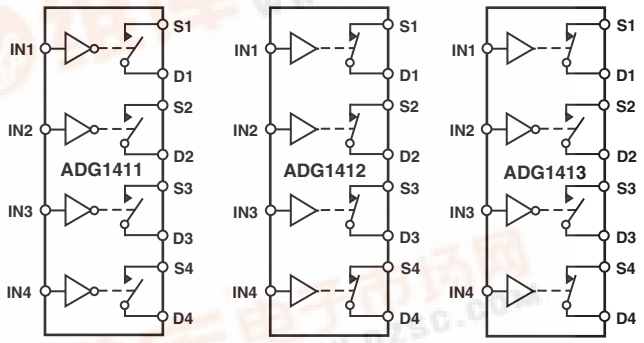


*Figure 1.*

*i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

The ADG1411/ADG1412/ADG1413 contain four independent single-pole/single-throw (SPST) switches. The ADG1411 and ADG1412 differ only in that the digital control logic is inverted. The ADG1411 switches are turned on with Logic 0 on the appropriate control input, while Logic 1 is required for the ADG1412. The ADG1413 has two switches with digital control logic similar to that of the ADG1411; the logic is inverted on the other two switches. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

The ADG1413 exhibits break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

## PRODUCT HIGHLIGHTS

1. 2Ω Max On Resistance over temperature.
2. Minimum distortion
3. 3 V logic-compatible digital inputs: $V_{IH}$ = 2.0 V, $V_{IL}$ = 0.8 V.
4. No $V_L$ logic power supply required.
5. Ultralow power dissipation: <0.03 µW.
6. 16-lead TSSOP and 4 mm × 4 mm LFCSP packages.



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113 

# TABLE OF CONTENTS



## REVISION HISTORY

# SPECIFICATIONS

## DUAL SUPPLY

$V_{DD}$ = 15 V ± 10%, $V_{SS}$ = −15 V± 10%, GND = 0 V, unless otherwise noted.

**Table 1.**

| | 25°C | −40°C to +85°C | −40°C to +125°C | | |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | $V_{DD}$ to $V_{SS}$ | V | |
| On Resistance ($R_{ON}$) | 1.5 | | | Ω typ | $V_S$ = ±10 V, $I_S$ = −10 mA; Figure 20 |
| | | 2 | | Ω max | $V_{DD}$ = +13.5 V, $V_{SS}$ = −13.5 V |
| On Resistance Match Between Channels ($\Delta R_{ON}$) | 0.1 | | | Ω typ | $V_S$ = ±10 V , $I_S$ = −10 mA |
| | | 0.5 | | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.1 | | | Ω typ | $V_S$ = −5 V/0 V/+5 V; $I_S$ = −10 mA |
| | | 0.5 | | Ω max | |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = +16.5 V, $V_{SS}$ = −16.5 V |
| Source Off Leakage, $I_S$ (Off) | ±0.01 | | | nA typ | $V_S$ = ±10 V, $V_D$ = ∓10 V; Figure 21 |
| | ±0.5 | ±2.5 | ±5 | nA max | |
| Drain Off Leakage, $I_D$ (Off) | ±0.01 | | | nA typ | $V_S$ = ±10V, $V_D$ = ∓10 V; Figure 21 |
| | ±0.5 | ±2.5 | ±5 | nA max | |
| Channel On Leakage, $I_D$, $I_S$ (On) | ±0.04 | | | nA typ | $V_S$ = $V_D$ = ±10 V; Figure 22 |
| | ±1 | ±5 | ±5 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V max | |
| Input Current, $I_{INL}$ or $I_{INH}$ | 0.005 | | ±2.5 | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | | ±0.5 | μA max | |
| Digital Input Capacitance, $C_{IN}$ | 2.5 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[1] | | | | | |
| $t_{ON}$ | 105 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 125 | | 185 | ns max | $V_S$ = +10 V; Figure 23 |
| $t_{OFF}$ | 40 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 50 | | 60 | ns max | $V_S$ = +10 V; Figure 23 |
| Break-Before-Make Time Delay, $t_D$ | 25 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| (ADG1413 only) | | | 10 | ns min | $V_{S1}$ = $V_{S2}$ = 10 V; Figure 24 |
| Charge Injection | 50 | | | pC typ | $V_S$ = 0 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Figure 25 |
| Off Isolation | 50 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 26 |
| Channel-to-Channel Crosstalk | 60 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 27 |
| Total Harmonic Distortion + Noise | 0.015 | | | % typ | $R_L$ = 110 Ω, 5 V rms, f = 20 Hz to 20 kHz |
| −3 dB Bandwidth | 200 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 28 |
| $C_S$ (Off) | 35 | | | pF typ | Vs = 0 V, f = 1 MHz |
| $C_D$ (Off) | 35 | | | pF typ | Vs = 0 V, f = 1 MHz |
| $C_D$, $C_S$ (On) | 150 | | | pF typ | Vs = 0 V, f = 1 MHz |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = +16.5 V, $V_{SS}$ = −16.5 V |
| $I_{DD}$ | 0.001 | | | μA typ | Digital inputs = 0 V or $V_{DD}$ |
| | | | 1 | μA max | |
| $I_{DD}$ | 220 | | | μA typ | Digital inputs = 5 V |

| | 25°C | −40°C to +85°C | −40°C to +125°C | | |
|---|---|---|---|---|---|
| | | | 320 | µA max | |
| $I_{SS}$ | 0.001 | | | µA typ | Digital inputs = 0 V, 5V or $V_{DD}$ |
| | | | 1. | µA max | |
| $V_{DD}/V_{SS}$ | | | ±4.5/±16.5 | V min/max | Gnd = 0V |

[1] Guaranteed by design, not subject to production test.

## SINGLE SUPPLY

$V_{DD}$ = 12 V ± 10%, $V_{SS}$ = 0 V, GND = 0 V, unless otherwise noted.

**Table 2.**

| | Y Version | | | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| | **25°C** | **−40°C to +85°C** | **−40°C to +125°C** | | |
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 2 | | | Ω typ | $V_S$ = +10 V, $I_S$ = −10 mA; Figure 20 |
| | 3 | 4 | | Ω max | $V_{DD}$ = +10.8 V, $V_{SS}$ = 0 V |
| On Resistance Match Between Channels ($\Delta R_{ON}$) | 0.1 | | | Ω typ | $V_S$ = +10 V, $I_S$ = −10 mA |
| | | | | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.1 | | | Ω typ | $V_S$ = −5 V/0 V/+5 V, $I_S$ = −10 mA |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = 13.2 V, $V_{SS}$ = 0 V |
| Source Off Leakage, $I_S$ (Off) | ±0.01 | | | nA typ | $V_S$ = 1 V/10 V, $V_D$ = 10 V/0 V; Figure 21 |
| | ±0.5 | ±2.5 | ±5 | nA max | |
| Drain Off Leakage, $I_D$ (Off) | ±0.01 | | | nA typ | $V_S$ = 1 V/10 V, $V_D$ = 10 V/0 V; Figure 21 |
| | ±0.5 | ±2.5 | ±5 | nA max | |
| Channel On Leakage, $I_D$, $I_S$ (On) | ±0.04 | | | nA typ | $V_S$ = $V_D$ = 1 V or 10 V; Figure 22 |
| | ±1 | ±5 | ±5 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V max | |
| Input Current, $I_{INL}$or $I_{INH}$ | 0.001 | | | μA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | | ±0.5 | μA max | |
| Digital Input Capacitance, $C_{IN}$ | 3 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[1] | | | | | |
| $t_{ON}$ | 120 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 155 | | 225 | ns max | $V_S$ = 8 V; Figure 23 |
| $t_{OFF}$ | 45 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 65 | | 85 | ns max | $V_S$ = 8 V; Figure 23 |
| Break-Before-Make Time Delay, $t_D$ | 50 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| (ADG1413 only) | | | 10 | ns min | $V_{S1}$ = $V_{S2}$ = 8 V; Figure 24 |
| Charge Injection | 50 | | | pC typ | $V_S$ = 6 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Figure 25 |
| Off Isolation | 50 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 26 |
| Channel-to-Channel Crosstalk | 60 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 27 |
| Total Harmonic Distortion + Noise | 0.015 | | | % typ | $R_L$ = 110 Ω, 5 V rms, f = 20 Hz to 20 kHz |
| −3 dB Bandwidth | 200 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 28 |
| $C_S$ (Off) | 35 | | | pF typ | Vs = 6V, f = 1 MHz |
| $C_D$ (Off) | 35 | | | pF typ | Vs = 6V, f = 1 MHz |
| $C_D$, $C_S$ (On) | 150 | | | pF typ | Vs = 6V, f = 1 MHz |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 13.2 V |
| $I_{DD}$ | 0.001 | | | μA typ | Digital inputs = 0 V or $V_{DD}$ |
| | | | 1 | μA max | |
| $I_{DD}$ | 220 | | | μA typ | Digital inputs = 5 V |
| | | | 320 | μA max | |
| $V_{DD}$ | | | 5/16.5 | V min/max | Gnd = 0V, Vss = 0V |

[1] Guaranteed by design, not subject to production test.

## DUAL SUPPLY

$V_{DD}$ = 5 V ± 10%, $V_{SS}$ = -5 V ± 10%, GND = 0 V, unless otherwise noted.

**Table 3.**

| | 25°C | −40°C to +85°C | −40°C to +125°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| ANALOG SWITCH | | | | | |
| Analog Signal Range | | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 3 | | | Ω typ | $V_S$ = ±3.3V, $I_S$ = −10 mA; Figure 20 |
| | 4 | | | Ω max | $V_{DD}$ = +4.5 V, $V_{SS}$ = −4.5 V |
| On Resistance Match Between Channels ($\Delta R_{ON}$) | 0.1 | | | Ω typ | $V_S$ = ±3.3 V , $I_S$ = −10 mA |
| | | | | Ω max | |
| On Resistance Flatness ($R_{FLAT(ON)}$) | 0.1 | | | Ω typ | $V_S$ = −3 V/0 V/+3 V; $I_S$ = −10 mA |
| LEAKAGE CURRENTS | | | | | $V_{DD}$ = +5.5 V, $V_{SS}$ = −5.5 V |
| Source Off Leakage, $I_S$ (Off) | ±0.01 | | | nA typ | $V_S$ = ±4.5 V, $V_D$ = ∓4.5 V; Figure 21 |
| | ±0.5 | ±2.5 | ±5 | nA max | |
| Drain Off Leakage, $I_D$ (Off) | ±0.01 | | | nA typ | $V_S$ = ±4.5V, $V_D$ = ∓4.5 V; Figure 21 |
| | ±0.5 | ±2.5 | ±5 | nA max | |
| Channel On Leakage, $I_D$, $I_S$ (On) | ±0.04 | | | nA typ | $V_S$ = $V_D$ = ±4.5V; Figure 22 |
| | ±1 | ±5 | ±5 | nA max | |
| DIGITAL INPUTS | | | | | |
| Input High Voltage, $V_{INH}$ | | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | | 0.8 | V max | |
| Input Current, $I_{INL}$or $I_{INH}$ | 0.001 | | | µA typ | $V_{IN}$ = $V_{INL}$ or $V_{INH}$ |
| | | | ±0.5 | µA max | |
| Digital Input Capacitance, $C_{IN}$ | 3 | | | pF typ | |
| DYNAMIC CHARACTERISTICS[1] | | | | | |
| $t_{ON}$ | 120 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 155 | | 225 | ns max | $V_S$ = 3 V; Figure 23 |
| $t_{OFF}$ | 45 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| | 65 | | 85 | ns max | $V_S$ = 3 V; Figure 23 |
| Break-Before-Make Time Delay, $t_D$ | 50 | | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF |
| (ADG1413 only) | | | 10 | ns min | $V_{S1}$ = $V_{S2}$ = 8 V; Figure 24 |
| Charge Injection | 10 | | | pC typ | $V_S$ = 0V, $R_S$ = 0 Ω, $C_L$ = 1 nF; Figure 25 |
| Off Isolation | 50 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 26 |
| Channel-to-Channel Crosstalk | 60 | | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; Figure 27 |
| Total Harmonic Distortion + Noise | 0.015 | | | % typ | $R_L$ = 110 Ω, 5 V rms, f = 20 Hz to 20 kHz |
| −3 dB Bandwidth | 200 | | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF; Figure 28 |
| $C_S$ (Off) | 35 | | | pF typ | Vs = 0V, f = 1 MHz |
| $C_D$ (Off) | 35 | | | pF typ | Vs = 0V, f = 1 MHz |
| $C_D$, $C_S$ (On) | 150 | | | pF typ | Vs = 0V, f = 1 MHz |
| POWER REQUIREMENTS | | | | | $V_{DD}$ = 5.5 V , Vss = -5.5V |
| $I_{DD}$ | 0.001 | | | µA typ | Digital inputs = 0 V or $V_{DD}$ |
| | | | 1.0 | µA max | |
| $I_{SS}$ | 0.001 | | | µA typ | Digital inputs = 5 V |
| | | | 1.0 | µA max | |
| $V_{DD}$/$V_{SS}$ | | | ±4.5/±16.5 | V min/max | Gnd = 0V |

[1] Guaranteed by design, not subject to production test.

# ABSOLUTE MAXIMUM RATINGS

$T_A$ = 25°C, unless otherwise noted.

**Table 4.**

| Parameter | Rating |
|---|---|
| $V_{DD}$ to $V_{SS}$ | 35 V |
| $V_{DD}$ to GND | −0.3 V to +25 V |
| $V_{SS}$ to GND | +0.3 V to −25 V |
| Analog Inputs[1] | $V_{SS}$ – 0.3 V to $V_{DD}$ + 0.3 V |
| Digital Inputs[1] | GND – 0.3 V to $V_{DD}$ + 0.3 V or 30 mA, whichever occurs first |
| Peak Current, S or D | 300 mA (pulsed at 1 ms, 10% duty cycle max) |
| Continuous Current, S or D | 200 mA |
| Operating Temperature Range | |
| Automotive (Y Version) | −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| 16-Lead TSSOP, $\theta_{JA}$ Thermal Impedance | 150.4°C/W |
| 16-Lead LFCSP, $\theta_{JA}$ Thermal Impedance | 72.7°C/W |
| Reflow Soldering Peak Temperature, Pb free | 260°C |

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

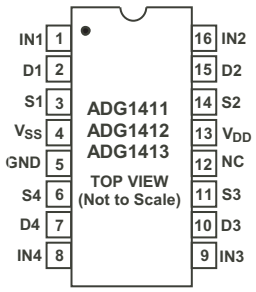


*Figure 2. TSSOP Pin Configuration*

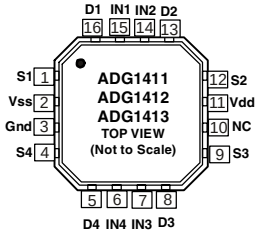


*Figure 3. LFCSP Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **TSSOP** | **LFCSP** | **Mnemonic** | **Description** |
| 1 | 15 | IN1 | Logic Control Input. |
| 2 | 16 | D1 | Drain Terminal. Can be an input or output. |
| 3 | 1 | S1 | Source Terminal. Can be an input or output. |
| 4 | 2 | $V_{SS}$ | Most Negative Power Supply Potential. |
| 5 | 3 | GND | Ground (0 V) Reference. |
| 6 | 4 | S4 | Source Terminal. Can be an input or output. |
| 7 | 5 | D4 | Drain Terminal. Can be an input or output. |
| 8 | 6 | IN4 | Logic Control Input. |
| 9 | 7 | IN3 | Logic Control Input. |
| 10 | 8 | D3 | Drain Terminal. Can be an input or output. |
| 11 | 9 | S3 | Source Terminal. Can be an input or output. |
| 12 | 10 | NC | No Connection. |
| 13 | 11 | $V_{DD}$ | Most Positive Power Supply Potential. |
| 14 | 12 | S2 | Source Terminal. Can be an input or output. |
| 15 | 13 | D2 | Drain Terminal. Can be an input or output. |
| 16 | 14 | IN2 | Logic Control Input. |

**Table 6. ADG1411/ADG1412 Truth Table**

| ADG1411 INx | ADG1412 INx | Switch Condition |
|---|---|---|
| 0 | 1 | On |
| 1 | 0 | Off |

**Table 7. ADG1413 Truth Table**

| Logic - INx | Switch 1, 4 | Switch 2, 3 |
|---|---|---|
| 0 | Off | On |
| 1 | On | Off |

# TERMINOLOGY

**$I_{DD}$**
The positive supply current.

**$I_{SS}$**
The negative supply current.

**$V_D$ ($V_S$)**
The analog voltage on Terminals D and S.

**$R_{ON}$**
The ohmic resistance between D and S.

**$R_{FLAT(ON)}$**
Flatness is defined as the difference between the maximum and minimum value of on resistance, as measured over the specified analog signal range.

**$I_S$ (Off)**
The source leakage current with the switch off.

**$I_D$ (Off)**
The drain leakage current with the switch off.

**$I_D$, $I_S$ (On)**
The channel leakage current with the switch on.

**$V_{INL}$**
The maximum input voltage for Logic 0.

**$V_{INH}$**
The minimum input voltage for Logic 1.

**$I_{INL}$ ($I_{INH}$)**
The input current of the digital input.

**$C_S$ (Off)**
The off switch source capacitance, measured with reference to ground.

**$C_D$ (Off)**
The off switch drain capacitance, measured with reference to ground.

**$C_D$, $C_S$ (On)**
The on switch capacitance, measured with reference to ground.

**$C_{IN}$**
The digital input capacitance.

**$t_{ON}$**
The delay between applying the digital control input and the output switching on. See Figure 23.

**$t_{OFF}$**
The delay between applying the digital control input and the output switching off.

**Charge Injection**
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

**Off Isolation**
A measure of unwanted signal coupling through an off switch.

**Crosstalk**
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

**Bandwidth**
The frequency at which the output is attenuated by 3 dB.

**On Response**
The frequency response of the on switch.

**Insertion Loss**
The loss due to the on resistance of the switch.

**THD + N**
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

## TYPICAL PERFORMANCE CHARACTERISTICS


*Figure 4. On Resistance as a Function of $V_D$ ($V_S$) for Dual Supply*


*Figure 5. On Resistance as a Function of $V_D$ ($V_S$) for Single Supply*


*Figure 6. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, Dual Supply*


*Figure 7. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, Single Supply*


*Figure 8. Leakage Currents as a Function of Temperature, Dual Supply*


*Figure 9. Leakage Currents as a Function of Temperature, Single Supply*


Figure 10. Logic Threshold Voltage vs. Supply Voltage


Figure 13. $T_{ON}/T_{OFF}$ Times vs. Temperature


Figure 11. $I_{DD}$ vs. Logic Level


Figure 14. Off Isolation vs. Frequency


Figure 12. Charge Injection vs. Source Voltage


Figure 15. Crosstalk vs. Frequency

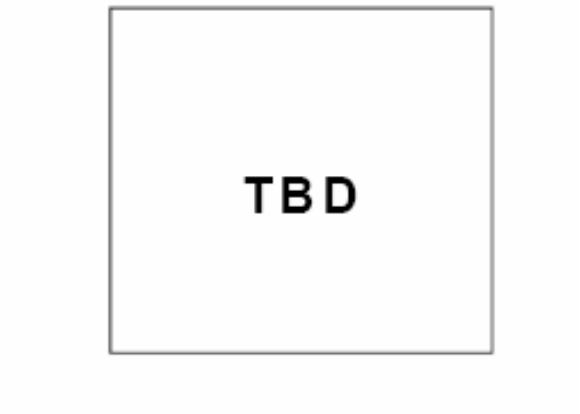


*Figure 16. On Response vs. Frequency*

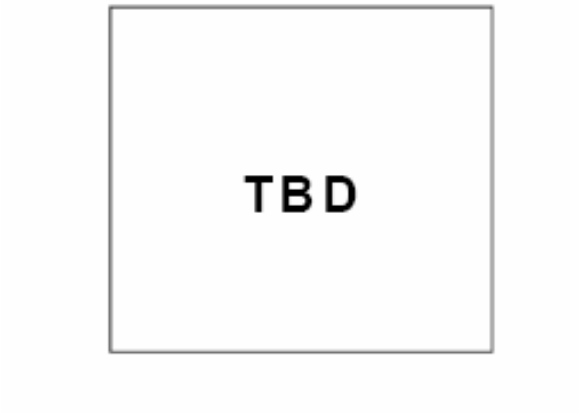


*Figure 17. Capacitance vs. Source Voltage, Dual Supply*

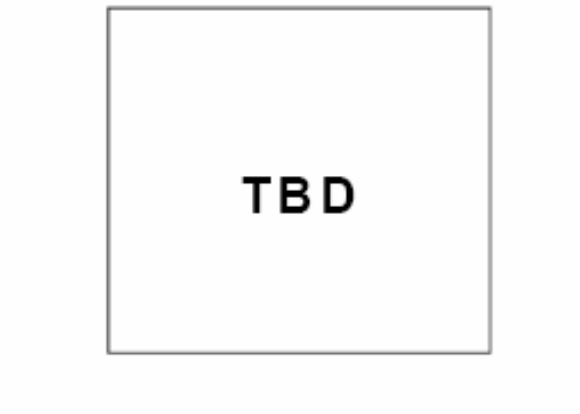


*Figure 18. Capacitance vs. Source Voltage, Single Supply*

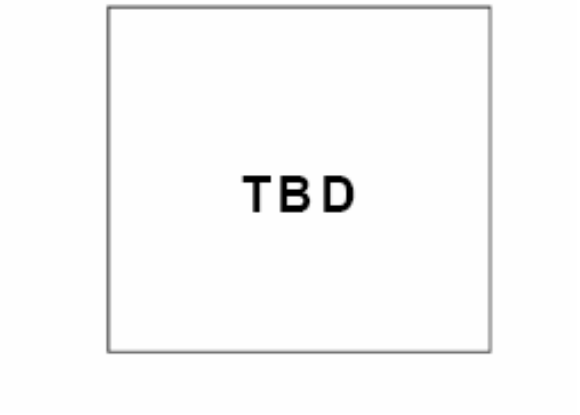


*Figure 19. THD + N vs. Frequency*

# TEST CIRCUITS

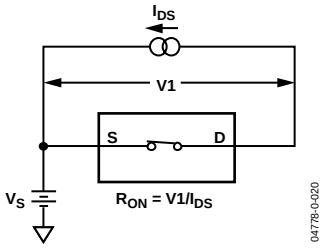


Figure 20. On Resistance

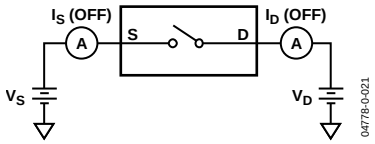


Figure 21. Off Leakage

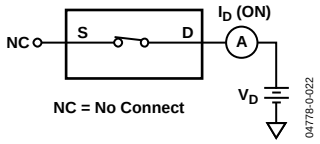


Figure 22. On Leakage

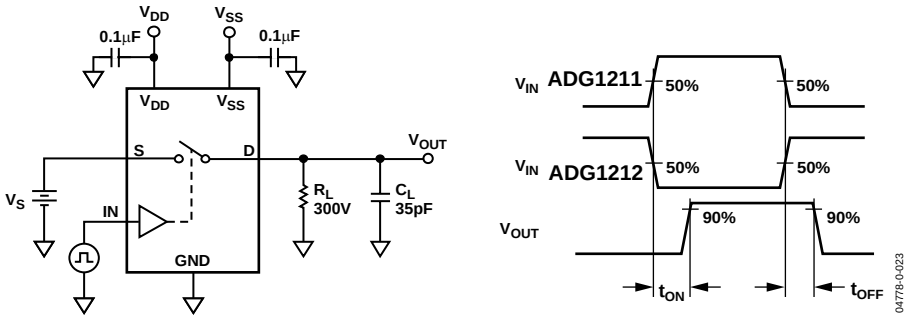


Figure 23. Switching Times

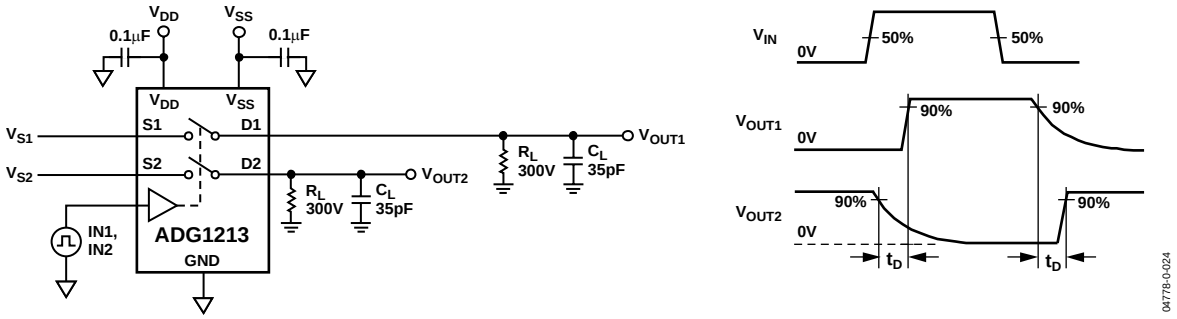


Figure 24. Break-Before-Make Time Delay

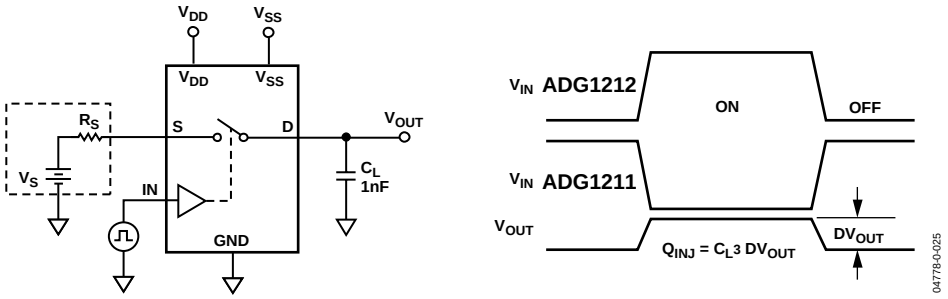


Figure 25. Charge Injection

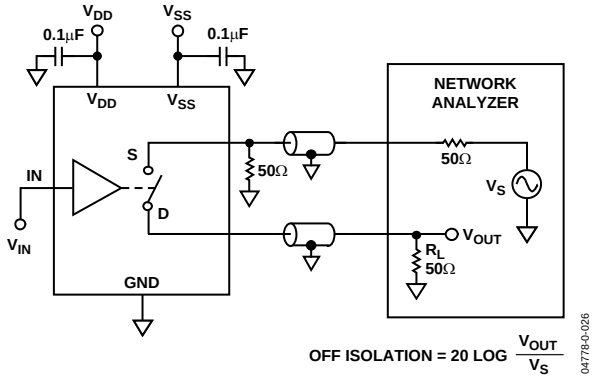


Figure 26. Off Isolation

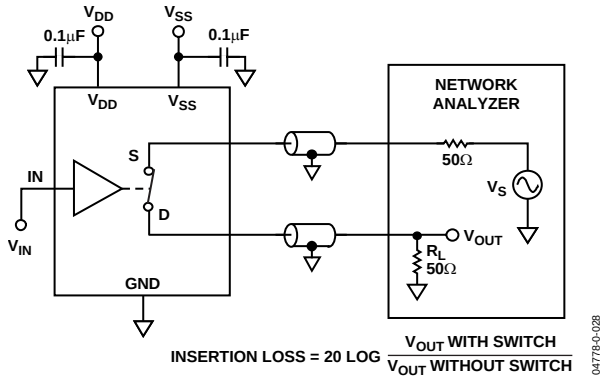


Figure 28. Bandwidth

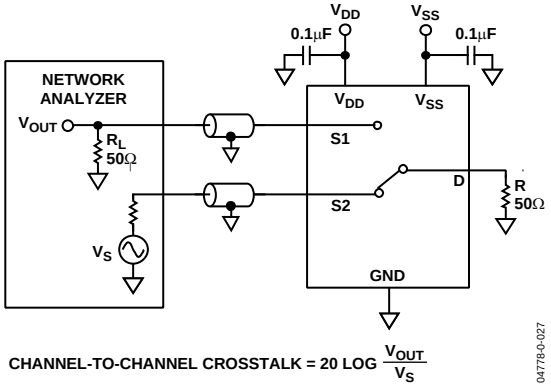


Figure 27. Channel-to-Channel Crosstalk

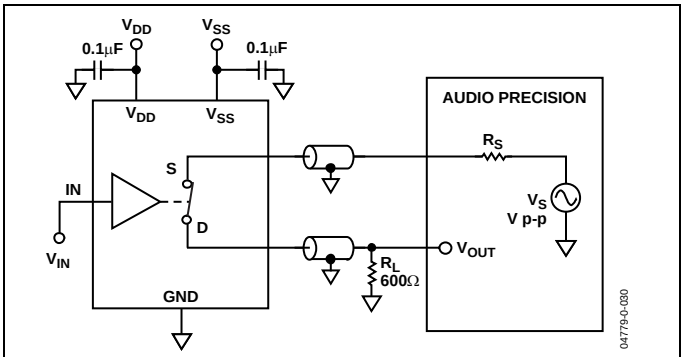


Figure 29.. THD + Noise

# OUTLINE DIMENSIONS

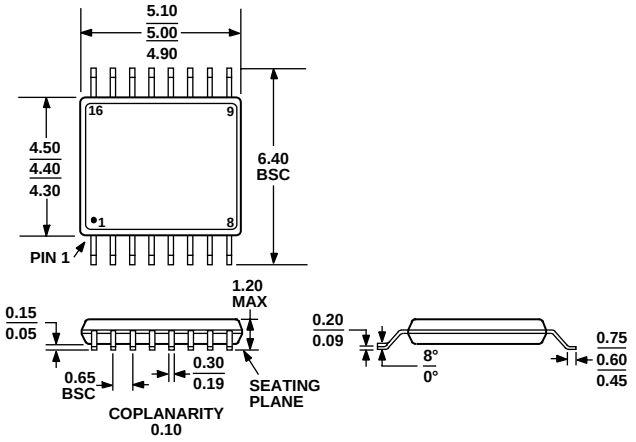


*Figure 29. 16-Lead Thin Shrink Small Outline Package [TSSOP]*
*(RU-16)*
*Dimensions shown in millimeters*

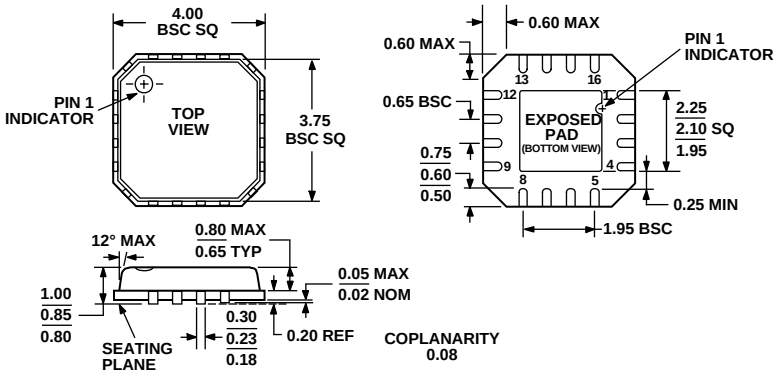


*Figure 30. 16-Lead Lead Frame Chip Scale Package [VQ_LFCSP]*
*4 mm × 4 mm Body, Very Thin Quad*
*(CP-16-4)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADG1411YRUZ[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1411YRUZ-REEL[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1411YRUZ-REEL7[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1411YCPZ-500RL7[1] | −40°C to +125°C | Lead Frame Chip Scale Package (VQ_LFCSP) | CP-16-4 |
| ADG1411YCPZ-REEL7[1] | −40°C to +125°C | Lead Frame Chip Scale Package (VQ_LFCSP) | CP-16-4 |
| ADG1412YRUZ[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1412YRUZ-REEL[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1412YRUZ-REEL7[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1412YCPZ-500RL7[1] | −40°C to +125°C | Lead Frame Chip Scale Package (VQ_LFCSP) | CP-16-4 |
| ADG1412YCPZ-REEL7[1] | −40°C to +125°C | Lead Frame Chip Scale Package (VQ_LFCSP) | CP-16-4 |
| ADG1413YRUZ[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1413YRUZ-REEL[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1413YRUZ-REEL7[1] | −40°C to +125°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG1413YCPZ-500RL7[1] | −40°C to +125°C | Lead Frame Chip Scale Package (VQ_LFCSP) | CP-16-4 |
| ADG1413YCPZ-REEL7[1] | −40°C to +125°C | Lead Frame Chip Scale Package (VQ_LFCSP) | CP-16-4 |

[1] Z = Pb-free part.

## NOTES


PR06615-0-5/07(PrE)