4 Ω R_{ON}, Triple/Quad SPDT ±15 V/+12 V/±5 V *i*CMOS® Switches

ADG1433/ADG1434

FEATURES

- 4.7 Ω maximum on resistance @ 25°C
- 0.5 Ω on resistance flatness
- 33 V supply maximum ratings
- Fully specified at ±15 V/+12 V/±5 V
- 3 V logic compatible inputs
- Rail-to-rail operation
- Break-before-make switching action
- 16-/20-lead TSSOP and 4 mm × 4 mm LFCSP_VQ packages

APPLICATIONS

- Relay replacement
- Audio and video routing
- Automatic test equipment
- Data acquisition systems
- Temperature measurement systems
- Avionics
- Battery-powered systems
- Communication systems
- Medical equipment

FUNCTIONAL BLOCK DIAGRAMS

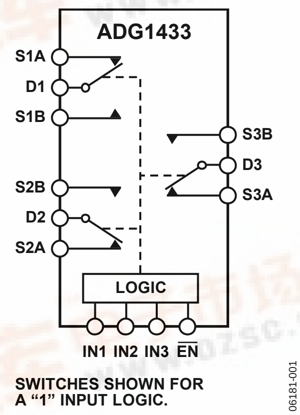

Figure 1. ADG1433 TSSOP and LFCSP_VQ

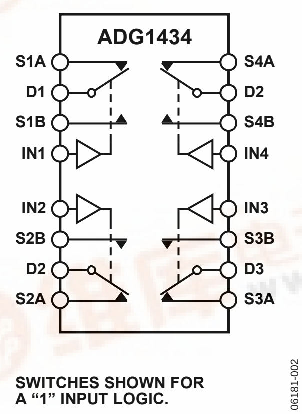

Figure 2. ADG1434 TSSOP

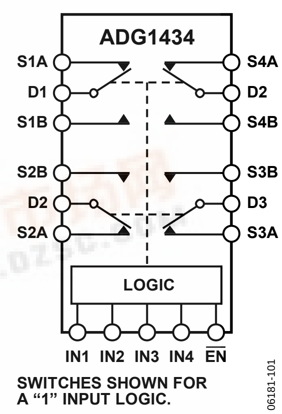

Figure 3. ADG1434 LFCSP_VQ

GENERAL DESCRIPTION

The ADG1433 and ADG1434 are monolithic industrial-CMOS (*i*CMOS) analog switches comprising three independently selectable single-pole, double-throw (SPDT) switches and four independently selectable SPDT switches, respectively.

All channels exhibit break-before-make switching action that prevents momentary shorting when switching channels. An $\overline{EN}$ input on the ADG1433 (LFCSP and TSSOP packages) and ADG1434 (LFCSP package only) is used to enable or disable the device. When disabled, all channels are switched off.

The *i*CMOS modular manufacturing process combines high voltage, complementary metal-oxide semiconductor (CMOS) and bipolar technologies. It enables the development of a wide range of high performance analog ICs capable of 33 V operation in a footprint that no other generation of high voltage parts has been able to achieve. Unlike analog ICs using conventional CMOS processes, *i*CMOS components can tolerate high supply voltages while providing increased performance, dramatically lower power consumption, and reduced package size.

The ultralow on resistance and on resistance flatness of these switches make them ideal solutions for data acquisition and gain switching applications, where low distortion is critical. *i*CMOS construction ensures ultralow power dissipation, making the parts ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 4.7 Ω maximum on resistance.
2. 0.5 Ω on resistance flatness.
3. 3 V logic compatible digital input V_{IH} = 2.0 V, V_{IL} = 0.8 V.
4. 16-/20-lead TSSOP and 4 mm × 4 mm LFCSP_VQ packages.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

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REVISION HISTORY

10/06—Revision 0: Initial Version

SPECIFICATIONS

15 V DUAL SUPPLY

V_{DD} = +15 V ± 10%, V_{SS} = −15 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance, R_{ON}	4			Ω typ	V_S = ±10 V, I_S = −10 mA; see Figure 25
	4.7	5.7	6.7	Ω max	V_{DD} = +13.5 V, V_{SS} = −13.5 V
On Resistance Match Between	0.5			Ω typ	V_S = ±10 V, I_S = −10 mA
Channels, ΔR_{ON}	0.78	0.85	1.1	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	0.5			Ω typ	V_S = ±10 V, I_S = −10 mA
	0.72	0.77	0.92	Ω max	
LEAKAGE CURRENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
Source Off Leakage, I_S (OFF)	±0.04			nA typ	V_D = ±10 V, V_S = ±10 V; see Figure 26
	±0.3	±0.6	±3	nA max	
Drain Off Leakage, I_D (OFF)	±0.04			nA typ	V_D = ±10 V, V_S = ±10 V; see Figure 26
	±0.3	±0.6	±3	nA max	
Channel On Leakage, I_D, I_S (ON)	±0.05			nA typ	V_S = V_D = ±10 V; see Figure 27
	±0.4	±0.8	±8	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005			µA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	µA max	
Digital Input Capacitance, C_{IN}	3			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS}	140			ns typ	R_L = 100 Ω, C_L = 35 pF
	170	200	230	ns max	V_S = 10 V, see Figure 28
Break-Before-Make Time Delay, t_D	40			ns typ	R_L = 100 Ω, C_L = 35 pF
			30	ns min	V_{S1} = V_{S2} = 10 V; see Figure 29
$t_{ON}(\overline{EN})$	140			ns typ	R_L = 100 Ω, C_L = 35 pF
	170	200	230	ns max	V_S = 10 V, see Figure 30
$t_{OFF}(\overline{EN})$	60			ns typ	R_L = 100 Ω, C_L = 35 pF
	75	85	90	ns max	V_S = 10 V; see Figure 30
Charge Injection	−50			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 31
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 32
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Total Harmonic Distortion, THD + N	0.025			% typ	R_L = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz, see Figure 35
−3 dB Bandwidth	200			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 33
Insertion Loss	0.24			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
C_S (OFF)	12			pF typ	f = 1 MHz
C_D (OFF)	22			pF typ	f = 1 MHz
C_D, C_S (ON)	72			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +16.5 V, V_{SS} = −16.5 V
I_{DD}	0.001			µA typ	Digital inputs = 0 V or V_{DD}
			1	µA max	
I_{DD}	260			µA typ	Digital inputs = 5 V
			440	µA max	

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
I_{SS}	0.001			μA typ	Digital inputs = 0 V, 5 V, or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	GND = 0 V

[1] Temperature range for Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 to V_{DD}	V	
On Resistance, R_{ON}	6			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA, see Figure 25
	8	9.5	11.2	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between	0.55			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
Channels, ΔR_{ON}	0.82	0.85	1.1	Ω max	
On Resistance Flatness, $R_{FLAT(ON)}$	1.5			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	2.5	2.5	2.8	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V
Source Off Leakage, I_S (OFF)	±0.04			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 26
	±0.3	±0.6	±3	nA max	
Drain Off Leakage, I_D (OFF)	±0.04			nA typ	V_S = 1 V/10 V, V_D = 10 V/1 V, see Figure 26
	±0.3	±0.6	±3	nA max	
Channel On Leakage, I_D, I_S (ON)	±0.06			nA typ	V_S = V_D = 1 V or 10 V, see Figure 27
	±0.4	±0.8	±8	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS}	200			ns typ	R_L = 100 Ω, C_L = 35 pF
	255	310	350	ns max	V_S = 8 V, see Figure 28
Break-Before-Make Time Delay, t_D	80			ns typ	R_L = 100 Ω, C_L = 35 pF
			55	ns min	V_{S1} = V_{S2} = 8 V, see Figure 29
$t_{ON}(\overline{EN})$	210			ns typ	R_L = 100 Ω, C_L = 35 pF
	270	320	360	ns max	V_S = 8 V, see Figure 30
$t_{OFF}(\overline{EN})$	70			ns typ	R_L = 100 Ω, C_L = 35 pF
	86	95	105	ns max	V_S = 8 V, see Figure 30
Charge Injection	−10			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF, see Figure 31
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 32
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
−3 dB Bandwidth	135			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 33
Insertion Loss	0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
C_S (OFF)	25			pF typ	f = 1 MHz
C_D (OFF)	45			pF typ	f = 1 MHz
C_D, C_S (ON)	80			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 13.2 V
I_{DD}	0.002			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
I_{DD}	260			μA typ	Digital inputs = 5 V
			440	μA max	
V_{DD}			5/16.5	V min/max	V_{SS} = 0 V, GND = 0 V

[1] Temperature range for Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C[1]	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{SS} to V_{DD}	V	
On Resistance (R_{ON})	7			Ω typ	V_S = ±4.5 V, I_S = −10 mA, see Figure 25
	9	10.5	12	Ω max	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance Match Between	0.55			Ω typ	V_S = ±4.5 V, I_S = −10 mA
Channels (ΔR_{ON})	0.78	0.91	1.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	1.5			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	2.5	2.5	3	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (OFF)	±0.02			nA typ	V_D = ±4.5 V, V_S = ±4.5 V, see Figure 26
	±0.3	±0.6	±3	nA max	
Drain Off Leakage, I_D (OFF)	±0.02			nA typ	V_D = ±4.5 V, V_S = ±4.5 V, see Figure 26
	±0.3	±0.6	±3	nA max	
Channel On Leakage, I_D, I_S (ON)	±0.04			nA typ	V_S = V_D = ±4.5 V, see Figure 27
	±0.4	±0.8	±8	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	±0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	4			pF typ	
DYNAMIC CHARACTERISTICS[2]					
Transition Time, t_{TRANS}	315			ns typ	R_L = 100 Ω, C_L = 35 pF
	430	480	550	ns max	V_S = 5 V, see Figure 28
Break-Before-Make Time Delay, t_D	90			ns typ	R_L = 100 Ω, C_L = 35 pF
			55	ns min	V_{S1} = V_{S2} = 5 V, see Figure 29
$t_{ON}(\overline{EN})$	325			ns typ	R_L = 100 Ω, C_L = 35 pF
	425	490	545	ns max	V_S = 5 V, see Figure 30
$t_{OFF}(\overline{EN})$	150			ns typ	R_L = 100 Ω, C_L = 35 pF
	200	225	240	ns max	V_S = 5 V, see Figure 30
Charge Injection	−10			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF, see Figure 31
Off Isolation	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 32
Channel-to-Channel Crosstalk	−70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 34
Total Harmonic Distortion, THD + N	0.06			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz, see Figure 35
−3 dB Bandwidth	145			MHz typ	R_L = 50 Ω, C_L = 5 pF, see Figure 33
Insertion Loss	0.5			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz, see Figure 33
C_S (OFF)	18			pF typ	f = 1 MHz
C_D (OFF)	32			pF typ	f = 1 MHz
C_D, C_S (ON)	80			pF typ	f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.002			μA typ	Digital inputs = 0 V, 5 V, or V_{DD}
			1	μA max	
I_{SS}	0.001			μA typ	Digital inputs = 0 V, 5 V, or V_{DD}
			1	μA max	
V_{DD}/V_{SS}			±4.5/±16.5	V min/max	GND = 0 V

[1] Temperature range for Y version: −40°C to +125°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	35 V
V_{DD} to GND	−0.3 V to +25 V
V_{SS} to GND	+0.3 V to −25 V
Analog Inputs, Digital Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% Duty Cycle Maximum)	100 mA
Operating Temperature Range	
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature (Pb-Free)	260 (+ 0 to −5)°C

[1] Overvoltages at A, $\overline{EN}$, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Only one absolute maximum rating may be applied at any one time.

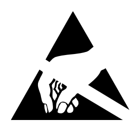
THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
TSSOP	150.4	50	°C/W
LFCSP_VQ	30.4	–	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

ADG1433

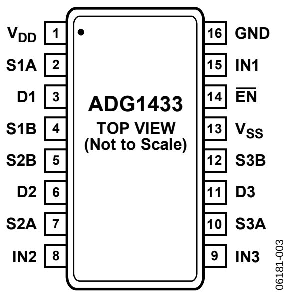


Figure 4. TSSOP Pin Configuration

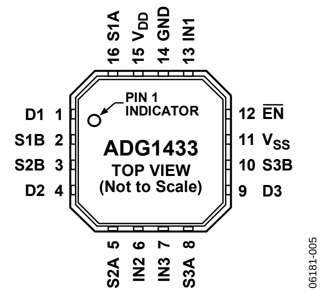


Figure 5. LFCSP_VQ Pin Configuration

Table 6. ADG1433 Pin Function Descriptions

Pin Number			
TSSOP	**LFCSP_VQ**	**Mnemonic**	**Description**
1	15	V_{DD}	Most Positive Power Supply Potential.
2	16	S1A	Source Terminal 1A. Can be an input or an output.
3	1	D1	Drain Terminal 1. Can be an input or an output.
4	2	S1B	Source Terminal 1B. Can be an input or an output.
5	3	S2B	Source Terminal 2B. Can be an input or an output.
6	4	D2	Drain Terminal 2. Can be an input or an output.
7	5	S2A	Source Terminal 2A. Can be an input or an output.
8	6	IN2	Logic Control Input.
9	7	IN3	Logic Control Input.
10	8	S3A	Source Terminal 3A. Can be an input or an output.
11	9	D3	Drain Terminal 3. Can be an input or an output.
12	10	S3B	Source Terminal 3B. Can be an input or an output.
13	11	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
14	12	$\overline{EN}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches.
15	13	IN1	Logic Control Input.
16	14	GND	Ground (0 V) Reference.

Table 7. ADG1433 Truth Table

$\overline{EN}$	INx	SxA	SxB
1	X	Off	Off
0	0	Off	On
0	1	On	Off

ADG1434

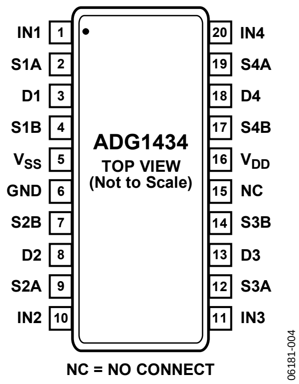


Figure 6. TSSOP Pin Configuration

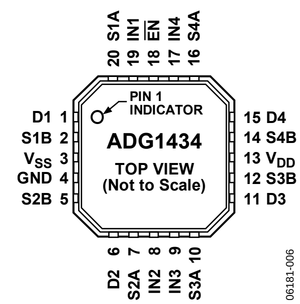


Figure 7. LFCSP_VQ Pin Configuration

Table 8. ADG1434 Pin Function Descriptions

Pin Number			
TSSOP	LFCSP_VQ	Mnemonic	Description
1	19	IN1	Logic Control Input.
2	20	S1A	Source Terminal 1A. Can be an input or an output.
3	1	D1	Drain Terminal 1. Can be an input or an output.
4	2	S1B	Source Terminal 1B. Can be an input or an output.
5	3	V_{SS}	Most Negative Power Supply Potential. In single supply applications, it can be connected to ground.
6	4	GND	Ground (0 V) Reference.
7	5	S2B	Source Terminal 2B. Can be an input or an output.
8	6	D2	Drain Terminal 2. Can be an input or an output.
9	7	S2A	Source Terminal 2A. Can be an input or an output.
10	8	IN2	Logic Control Input.
11	9	IN3	Logic Control Input.
12	10	S3A	Source Terminal 3A. Can be an input or an output.
13	11	D3	Drain Terminal 3. Can be an input or an output.
14	12	S3B	Source Terminal 3B. Can be an input or an output.
15	–	NC	No Connect.
16	13	V_{DD}	Most Positive Power Supply Potential.
17	14	S4B	Source Terminal 4B. Can be an input or an output.
18	15	D4	Drain Terminal 4. Can be an input or an output.
19	16	S4A	Source Terminal 4A. Can be an input or an output.
20	17	IN4	Logic Control Input.
–	18	$\overline{EN}$	Active Low Digital Input. When high, the device is disabled and all switches are off. When low, INx logic inputs determine the on switches.

Table 9. ADG1434 TSSOP Truth Table

INx	SxA	SxB
0	Off	On
1	On	Off

Table 10. ADG1434 LFCSP_VQ Truth Table

$\overline{EN}$	INx	SxA	SxB
1	X	Off	Off
0	0	Off	On
0	1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

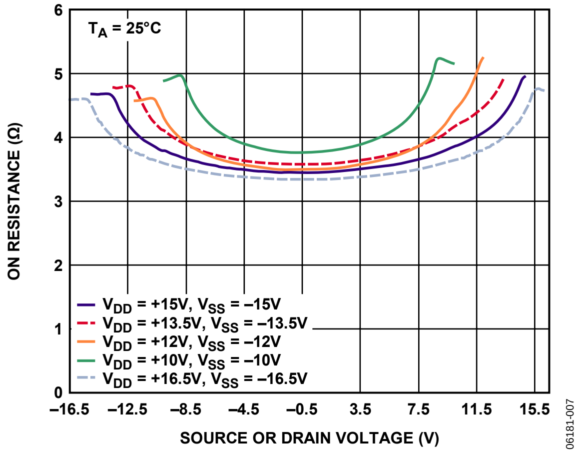


Figure 8. On Resistance as a Function of V_D (V_S), Dual Supply

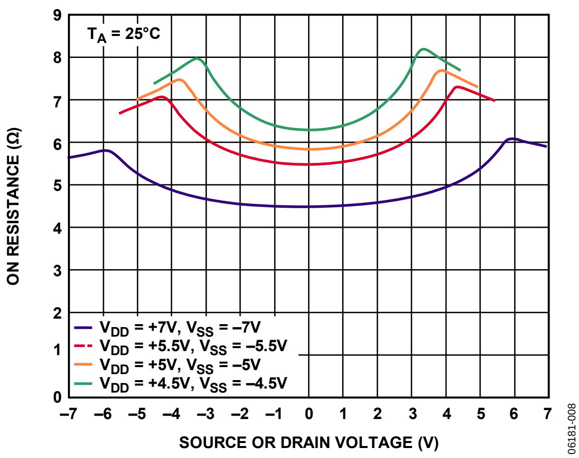


Figure 9. On Resistance as a Function of V_D (V_S), Dual Supply

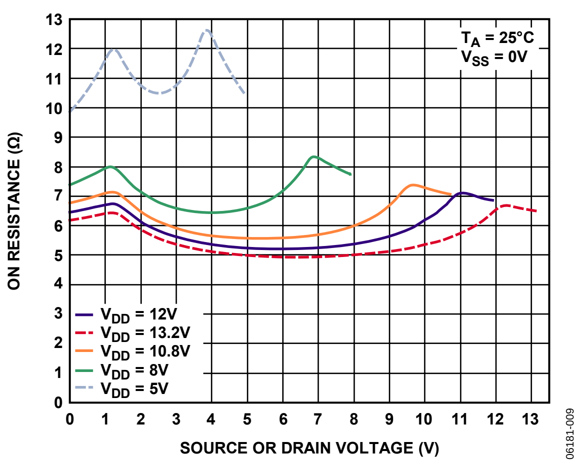


Figure 10. On Resistance as a Function of V_D (V_S), Single Supply

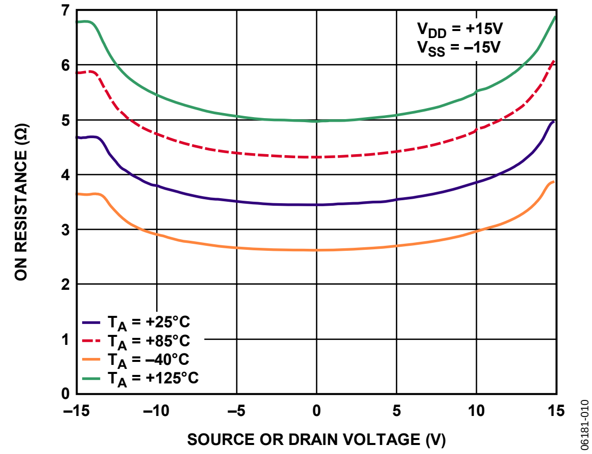


Figure 11. On Resistance as a Function of V_D (V_S) for Different Temperatures, 15 V Dual Supply

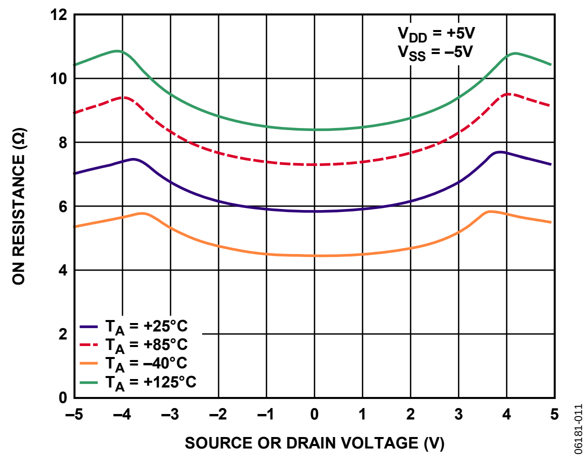


Figure 12. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Dual Supply

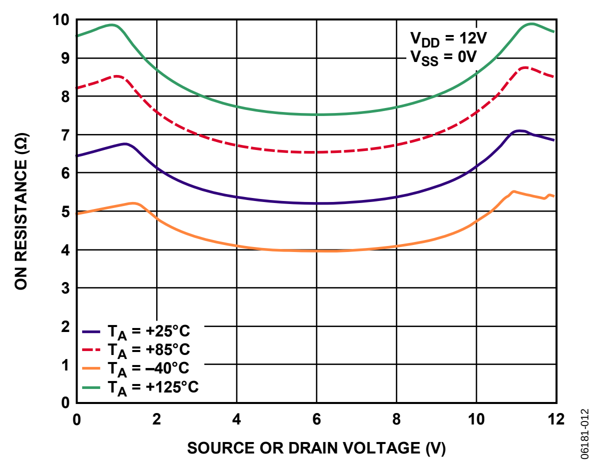


Figure 13. On Resistance as a Function of V_D (V_S) for Different Temperatures, 12 V Single Supply

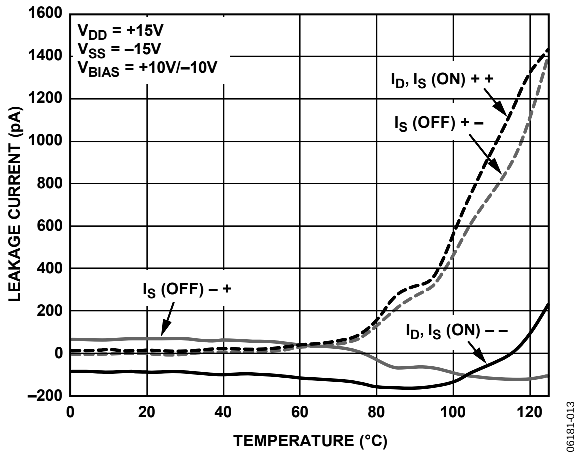


Figure 14. Leakage Currents as a Function of V_D (V_S), 15 V Dual Supply

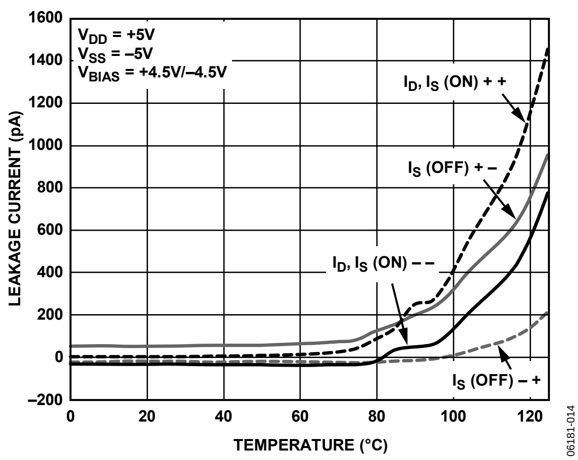


Figure 15. Leakage Currents as a Function of Temperature, 5 V Dual Supply

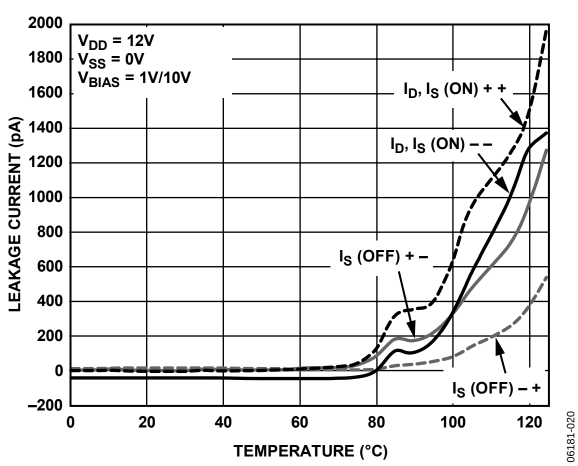


Figure 16. Leakage Currents as a Function of Temperature, 12 V Single Supply

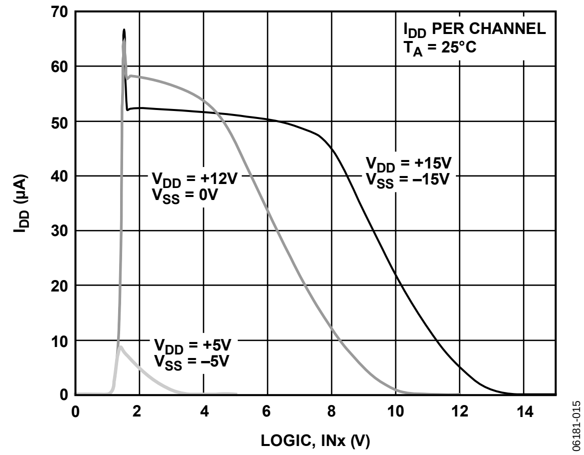


Figure 17. I_{DD} vs. Logic Level

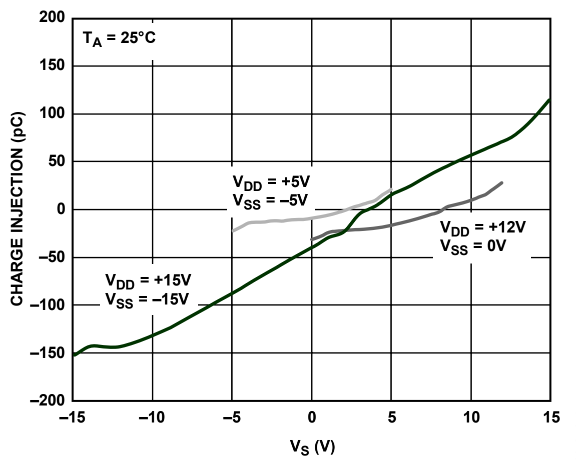


Figure 18. Charge Injection vs. Source Voltage

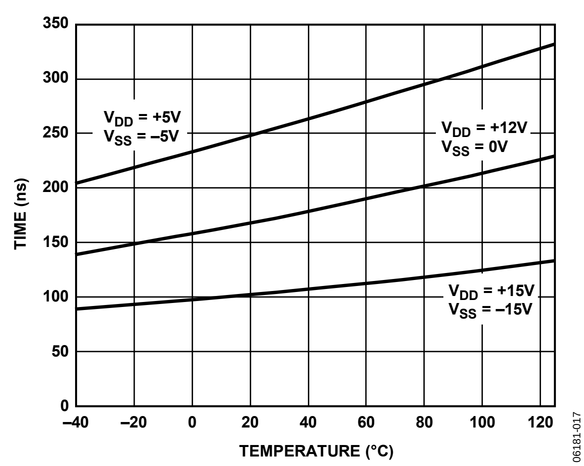


Figure 19. Transition Time vs. Temperature

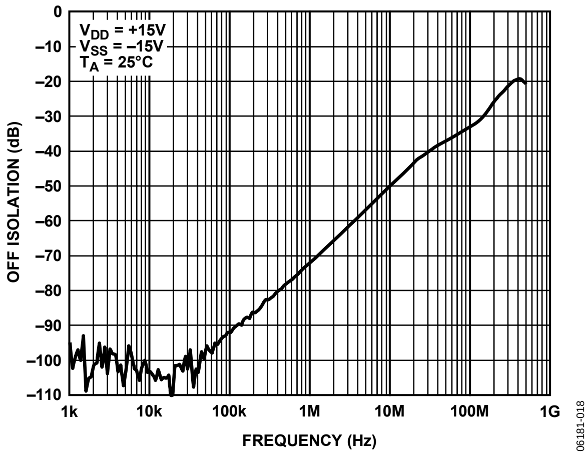


Figure 20. Off Isolation vs. Frequency

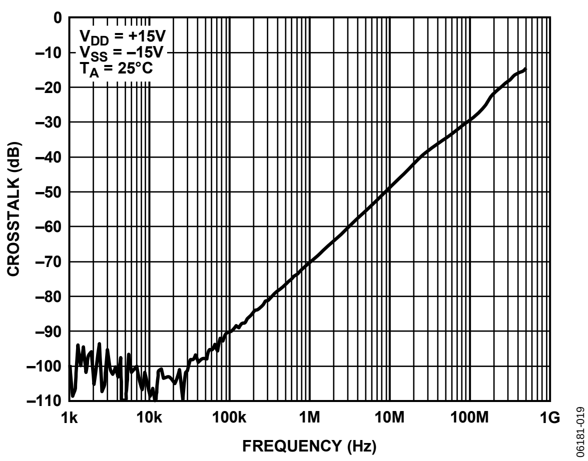


Figure 21. Crosstalk vs. Frequency

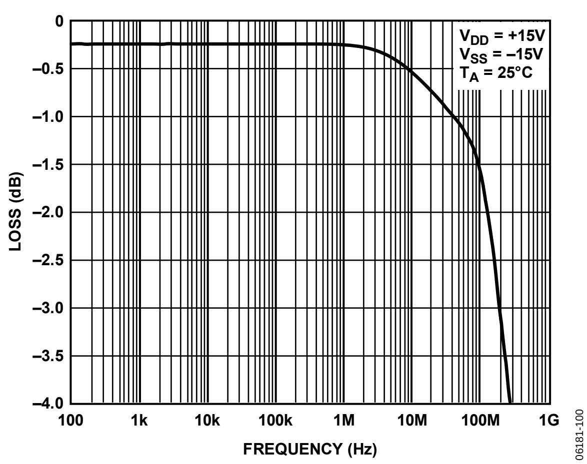


Figure 22. On Response vs. Frequency

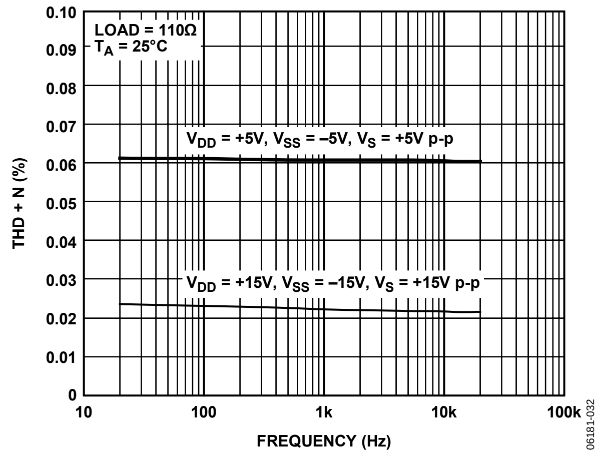


Figure 23. THD + N vs. Frequency

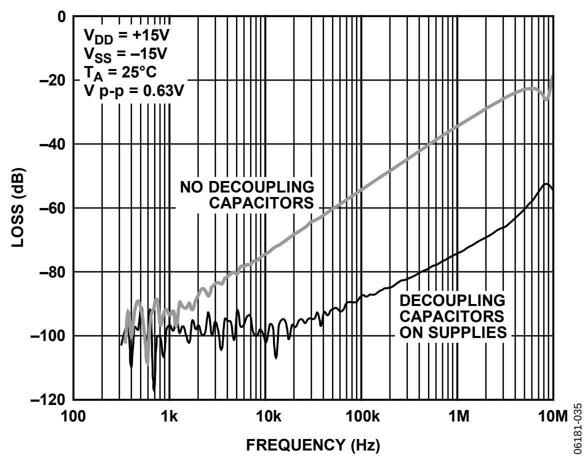


Figure 24. ACPSRR vs. Frequency

TEST CIRCUITS

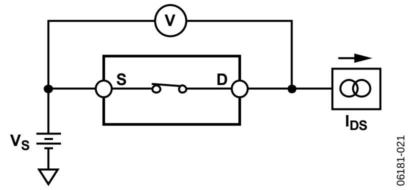


Figure 25. On Resistance

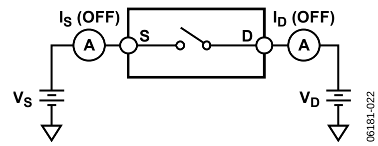


Figure 26. Off Leakage

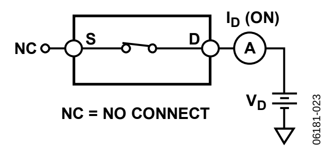


Figure 27. On Leakage

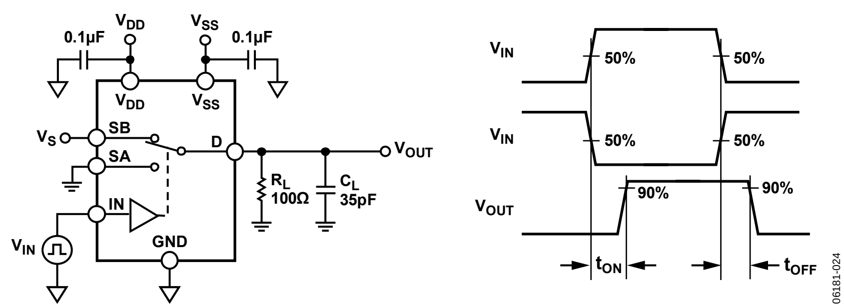


Figure 28. Switching Timing

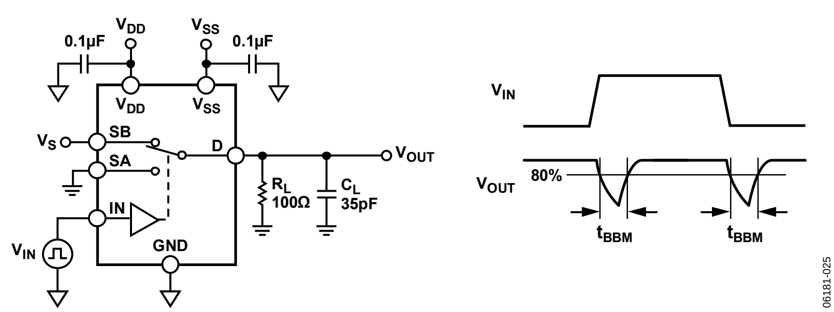


Figure 29. Break-Before-Make Delay

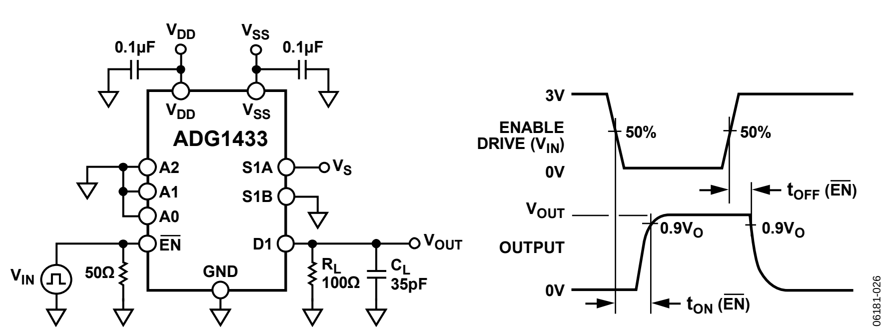


Figure 30. Enable Delay, $t_{ON}(\overline{EN})$, $t_{OFF}(\overline{EN})$

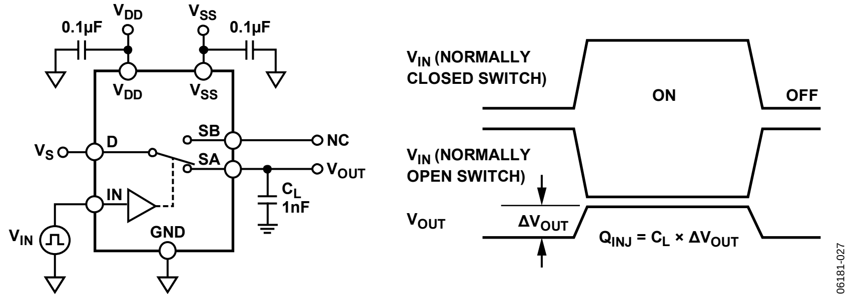


Figure 31. Charge Injection

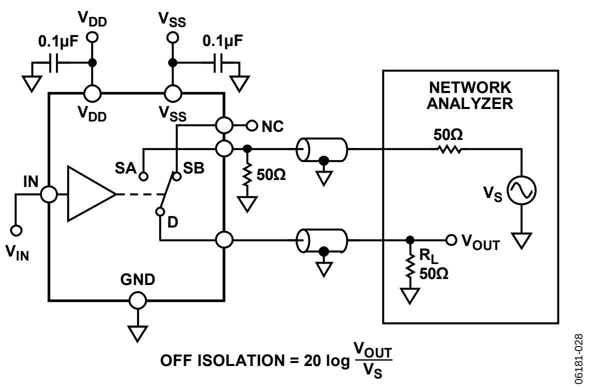


Figure 32. Off Isolation

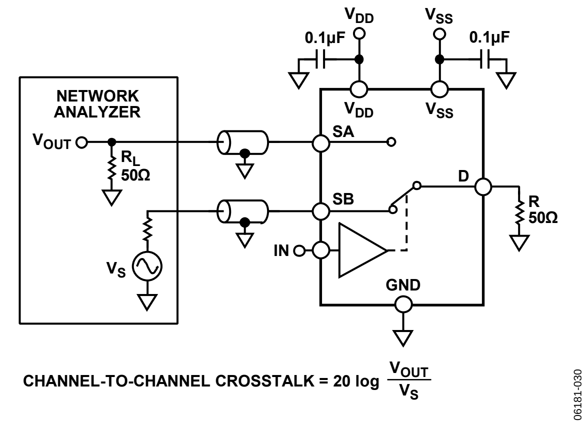


Figure 34. Channel-to-Channel Crosstalk

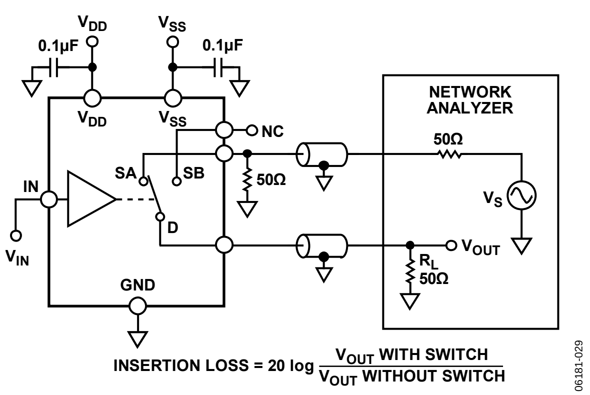


Figure 33. Bandwidth

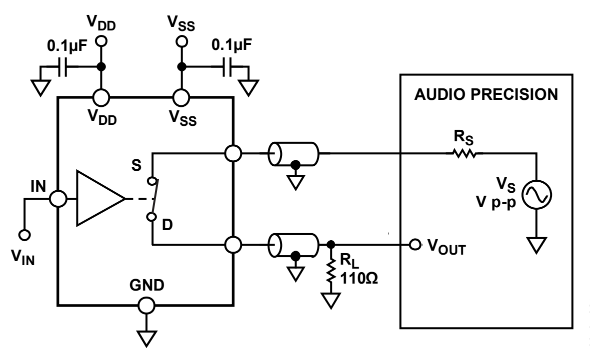


Figure 35. THD + Noise

TERMINOLOGY

R_{ON}
Ohmic resistance between Terminal D and Terminal S.

ΔR_{ON}
The difference between the R_{ON} of any two channels.

$R_{FLAT(ON)}$
The difference between the maximum and minimum value of on resistance as measured.

I_S (OFF)
Source leakage current when the switch is off.

I_D (OFF)
Drain leakage current when the switch is off.

I_D, I_S (ON)
Channel leakage current when the switch is on.

V_D (V_S)
Analog voltage on Terminal D and Terminal S.

C_S (OFF)
Channel input capacitance for off condition.

C_D (OFF)
Channel output capacitance for off condition.

C_D, C_S (ON)
On switch capacitance.

C_{IN}
Digital input capacitance.

$t_{ON}(\overline{EN})$

Delay time between the 50% and 90% points of the digital input and switch on condition.

$t_{OFF}(\overline{EN})$
Delay time between the 50% and 90% points of the digital input and switch off condition.

t_{TRANS}
Delay time between the 50% and 90% points of the digital inputs and the switch on condition when switching from one address state to another.

T_{BBM}
Off time measured between the 80% point of both switches when switching from one address state to another.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

I_{DD}
Positive supply current.

I_{SS}
Negative supply current.

Off Isolation
A measure of unwanted signal coupling through an off channel.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

THD + N
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

AC Power Supply Rejection Ratio (ACPSRR)
A measure of the ability of a part to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p. The ratio of the amplitude of signal on the output to the amplitude of the modulation is the ACPSRR.

OUTLINE DIMENSIONS

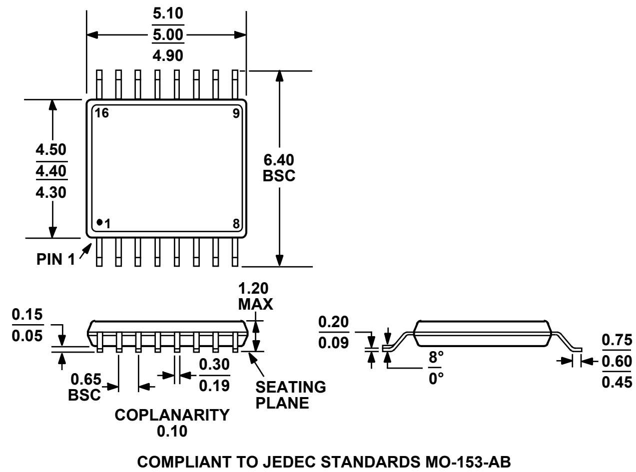


Figure 36. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

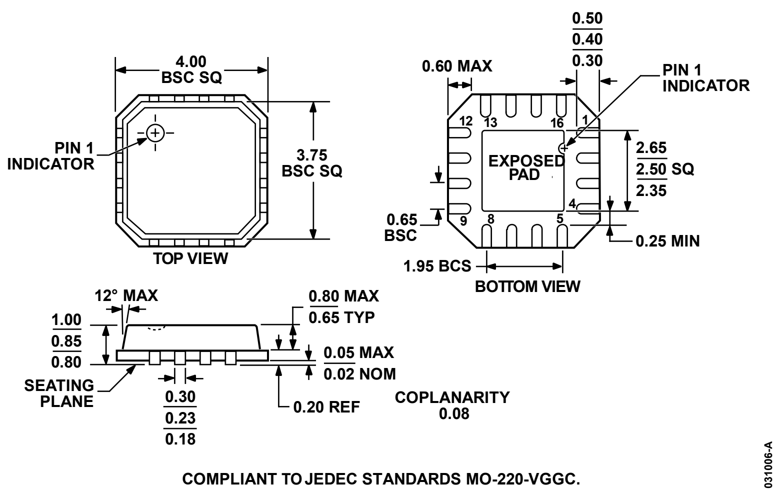
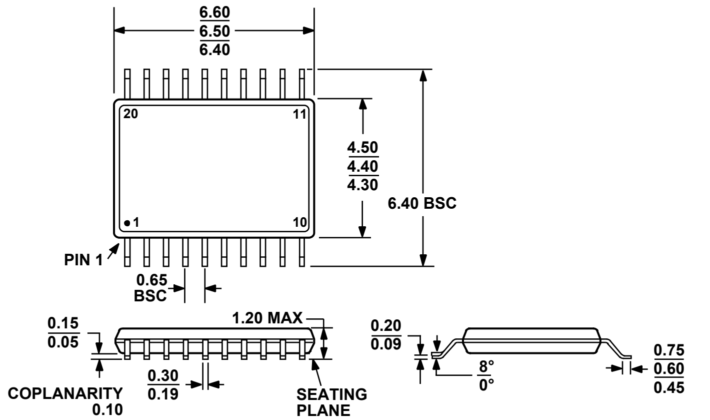
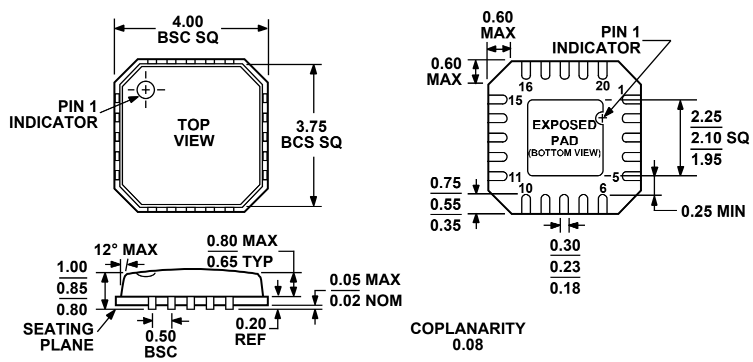


Figure 37. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm, Very Thin Quad (CP-16-13)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AC

Figure 38. 20-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-20)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

Figure 39. 20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad (CP-20-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Description	$\overline{\text{EN}}$ Pin	Package Option
ADG1433YRUZ[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG1433YRUZ-REEL[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG1433YRUZ-REEL7[1]	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	Yes	RU-16
ADG1433YCPZ-REEL[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	Yes	CP-16-13
ADG1433YCPZ-REEL7[1]	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	Yes	CP-16-13
ADG1434YRUZ[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG1434YRUZ-REEL[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG1434YRUZ-REEL7[1]	−40°C to +125°C	20-Lead Thin Shrink Small Outline Package [TSSOP]	No	RU-20
ADG1434YCPZ-REEL[1]	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	Yes	CP-20-1
ADG1434YCPZ-REEL7[1]	−40°C to +125°C	20-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	Yes	CP-20-1

[1] Z = Pb-free part.

NOTES

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