±80°/sec Yaw Rate Gyro with SPI® Interface

ADIS16080

FEATURES

Complete angular rate gyroscope
Z-axis (yaw rate) response
SPI digital output interface
High vibration rejection over wide frequency
2000 *g* powered shock survivability
Externally controlled self test
Internal temperature sensor output
Dual auxiliary 12-bit ADC inputs
Absolute rate output for precision applications
5 V single-supply operation
8.2 mm × 8.2 mm × 5.2 mm package
RoHS-compliant

APPLICATIONS

Platform stabilization
Image stabilization
Guidance and control
Inertial measurement units
Robotics

GENERAL DESCRIPTION

The ADIS16080 is a complete angular rate sensor (gyroscope) that uses the Analog Devices, Inc. surface-micromachining process to make a functionally complete angular rate sensor with an integrated serial peripheral interface (SPI).

The digital data available at the SPI port is proportional to the angular rate about the axis normal to the top surface of the package (see Figure 19). A single external resistor can be used to increase the measurement range. An external capacitor can be used to lower the bandwidth.

Access to an internal temperature sensor measurement is provided, through the SPI, for compensation techniques. Two pins are available for the user to input analog signals for digitization. An additional output pin provides a precision voltage reference. Two digital self-test inputs electro-mechanically excite the sensor to test operation of the sensor and the signal conditioning circuits.

The ADIS16080 is available in an 8.2 mm × 8.2 mm × 5.2 mm 16-terminal, peripheral land grid array (LGA) package.

FUNCTIONAL BLOCK DIAGRAM

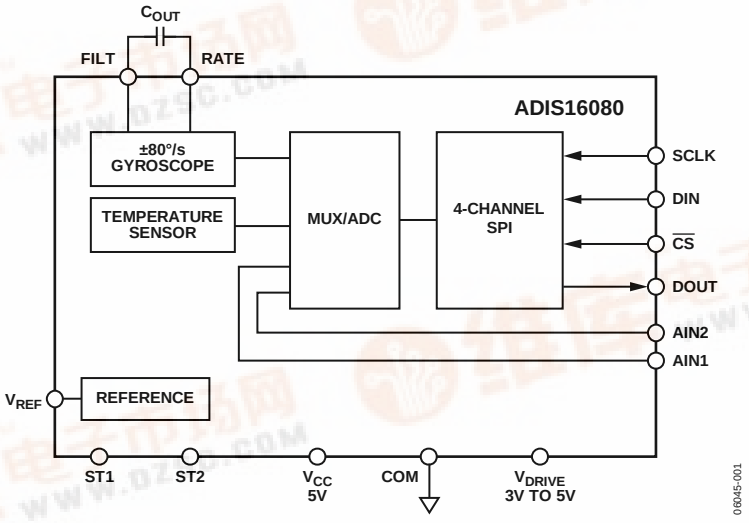

Figure 1.

Rev. 0

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REVISION HISTORY

7/06—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_{CC} = V_{DRIVE} = 5 V, angular rate = 0°/sec, C_{OUT} = 0 µF, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
SENSITIVITY					
Dynamic Range[2]	Full-scale range over specifications range	±80			°/sec
Initial	Clockwise rotation is positive output, T_A = −40°C to +85°C	9.21	10.24	11.26	LSB/°/sec
Change over Temperature[3]	V_{CC} = V_{DRIVE} = 4.75 V to 5.25 V		±5		%
Nonlinearity	Best fit straight line		0.15		% of FS
Voltage Sensitivity	V_{CC} = V_{DRIVE} = 4.75 V to 5.25 V		0.7		% of FS
NULL					
Initial		1629	2048	2466	LSB
Change Over Temperature[3]	V_{CC} = V_{DRIVE} = 4.75 V to 5.25 V		±85		LSB
Turn-On Time	Power on to ±½°/sec of final		35		ms
Linear Acceleration Effect	Any axis		2.05		LSB/*g*
Voltage Sensitivity	V_{CC} = V_{DRIVE} = 4.75 V to 5.25 V		±10.24		LSB/V
NOISE PERFORMANCE					
Total Noise	0.1 Hz to 40 Hz; no averaging		0.42		°/sec rms
			43		LSB rms
Rate Noise Density	@ 25°C		0.05		°/sec /√Hz
			0.51		LSB rms/√Hz
FREQUENCY RESPONSE					
3 dB Bandwidth (User-Selectable)[4]	C_{OUT} = 0 µF		40		Hz
Sensor Resonant Frequency			14		kHz
SELF-TEST INPUTS					
ST1 RATEOUT Response[5]	ST1 pin from Logic 0 to Logic 1	−328	−540	−819	LSB
ST2 RATEOUT Response[5]	ST2 pin from Logic 0 to Logic 1	+328	+540	+819	LSB
Logic 1 Input Voltage	Standard high logic level definition	3.3			V
Logic 0 Input Voltage	Standard low logic level definition			1.7	V
Input Impedance	To common		50		kΩ
TEMPERATURE SENSOR					
Reading at 298 K			2048		LSB
Scale Factor	Proportional to absolute temperature		6.88		LSB/K
2.5 V REFERENCE					
Voltage Value		2.45	2.5	2.55	V
Load Drive to Ground	Source		100		µA
Load Regulation	0 µA < I_{OUT} < 100 µA		5.0		mV/mA
Power Supply Rejection	V_{CC} = V_{DRIVE} = 4.75 V to 5.25 V		1.0		mV/V
Temperature Drift	Delta from 25°C		5.0		mV
LOGIC INPUTS					
Input High Voltage, V_{INH}		0.7 × V_{DRIVE}			V
Input Low Voltage, V_{INL}				0.3 × V_{DRIVE}	V
Input Current, I_{IN}	Typically 10 nA	−1		+1	µA
Input Capacitance, C_{IN}			10		pF
ANALOG INPUTS[6]					
Resolution			12		Bits
Integral Nonlinearity[6]		−2		+2	LSB
Differential Nonlinearity		−2		+2	LSB
Offset Error		−8		+8	LSB
Gain Error		−2		+2	LSB
Input Voltage Range		0		V_{REF} × 2	V

Parameter	Conditions	Min[1]	Typ	Max[1]	Unit
Leakage Current		−1		+1	µA
Input Capacitance			20		pF
Full Power Bandwidth			8		MHz
DIGITAL OUTPUTS					
Output High Voltage (V_{OH})	I_{SOURCE} = 200 µA	V_{DRIVE} − 0.2			V
Output Low Voltage (V_{OL})	I_{SINK} = 200 µA			0.4	V
CONVERSION RATE					
Conversion Time	16 SCLK cycles with SCLK at 20 MHz			800	ns
Throughput Rate				1	MSPS
POWER SUPPLY[7]					
V_{CC}		4.75	5	5.25	V
V_{DRIVE}		2.7		5.25	V
V_{CC} Quiescent Supply Current	V_{CC} @ 5 V, f_{SCLK} = 50 kSPS		7.0	9.0	mA
V_{DRIVE} Quiescent Supply Current	V_{DRIVE} @ 5 V, f_{SCLK} = 50 kSPS		70	500	µA
Power Dissipation	V_{CC} and V_{DRIVE} @ 5 V, f_{SCLK} = 50 kSPS		40		mW
TEMPERATURE RANGE					
Specified Performance	Tested to max and min specifications	−40		+85	°C

[1] All minimum and maximum specifications are guaranteed. Typical specifications are neither tested nor guaranteed.
[2] Dynamic range is the maximum full-scale measurement range possible, including output swing range, initial offset, sensitivity, offset drift, and sensitivity drift at 5 V supplies.
[3] Defined as the output change from ambient to maximum temperature or ambient to minimum temperature.
[4] Frequency at which the response is 3 dB down from dc response. Bandwidth = $1/(2 \times \pi \times 180\ k\Omega \times (22\ nF + C_{OUT}))$. For C_{OUT} = 0, bandwidth = 40 Hz. For C_{OUT} = 1 µF, bandwidth = 0.87 Hz.
[5] Self-test response varies with temperature.
[6] For $V_{IN} < V_{CC}$.
[7] All at T_A = −40°C to +85°C.

TIMING SPECIFICATIONS

T_A = 25°C, angular rate = 0°/sec, unless otherwise noted.[1]

Table 2.

Parameter	$V_{CC} = V_{DRIVE} = 5$	Unit	Description
f_{SCLK}[2]	10	kHz min	
	20	MHz max	
$t_{CONVERT}$	16 × t_{SCLK}		
t_{QUIET}	50	ns min	Minimum quiet time required between $\overline{CS}$ rising edge and start of next conversion
t_2	10	ns min	$\overline{CS}$ to SCLK setup time
t_3[3]	30	ns max	Delay from $\overline{CS}$ until DOUT three-state disabled
t_4[3]	40	ns max	Data access time after SCLK falling edge
t_5	0.4 × t_{SCLK}	ns min	SCLK low pulse width
t_6	0.4 × t_{SCLK}	ns min	SCLK high pulse width
t_7	10	ns min	SCLK to DOUT valid hold time
t_8[4]	15/35	ns min/max	SCLK falling edge to DOUT high impedance
t_9	10	ns min	DIN setup time prior to SCLK falling edge
t_{10}	5	ns min	DIN hold time after SCLK falling edge
t_{11}	20	ns min	16th SCLK falling edge to $\overline{CS}$ high
t_{12}	1	µs max	Power-up time from full power-down/auto shutdown modes

[1] Guaranteed by design. All input signals are specified with t_R and t_F = 5 ns (10% to 90% of V_{CC}) and timed from a voltage level of 1.6 V. The 5 V operating range spans from 4.75 V to 5.25 V.
[2] Mark/space ratio for the SCLK input is 40/60 to 60/40.
[3] Measured with the load circuit in Figure 3 and defined as the time required for the output to cross 0.4 V or 0.7 V × V_{DRIVE}.
[4] t_8 is derived from the measured time taken by the data outputs to change 0.5 V when loaded with the circuit in Figure 3. The measured number is then extrapolated back to remove the effects of charging or discharging the 50 pF capacitor. This means that the time, t_8, quoted in the timing characteristics is the true bus relinquish time of the part and is independent of the bus loading.

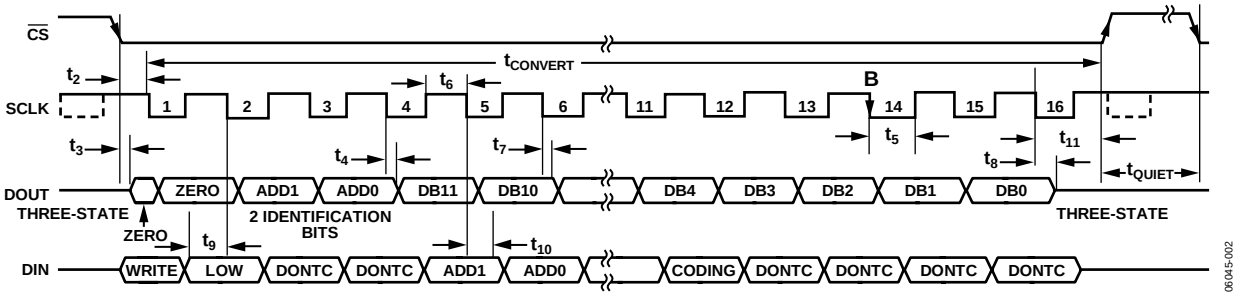

Figure 2. Gyroscope Serial Interface Timing Diagram

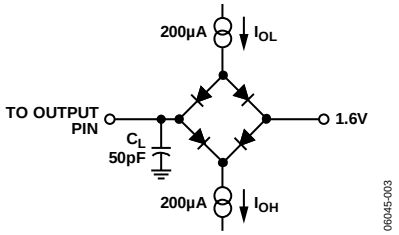

Figure 3. Load Circuit for Digital Output Timing Specifications

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration (Any Axis, Unpowered, 0.5 ms)	2000 *g*
Acceleration (Any Axis, Powered, 0.5 ms)	2000 *g*
V_{CC} to COM	−0.3 V to +6.0 V
V_{DRIVE} to COM	−0.3 V to V_{CC} + 0.3 V
Analog Input Voltage to COM	−0.3 V to V_{CC} + 0.3 V
Digital Input Voltage to COM	−0.3 V to +7.0 V
Digital Output Voltage to COM	−0.3 V to V_{CC} + 0.3 V
STx Input Voltage to COM	−0.3 V to V_{CC} + 0.3 V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under the Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Drops onto hard surfaces can cause shocks of greater than 2000 *g* and exceed the absolute maximum rating of the device. Care should be exercised in handling to avoid damage.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

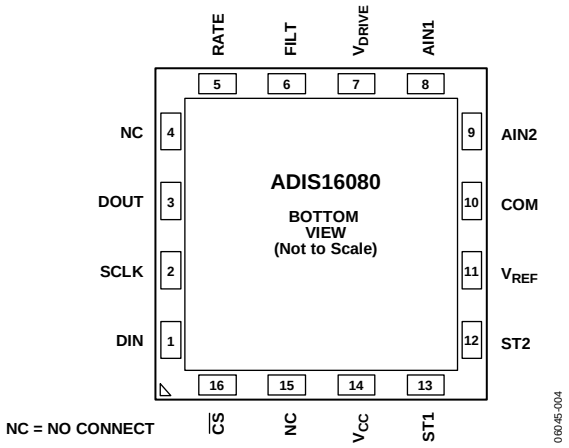

Figure 4. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	DIN	I	Data In. Data to be written to the control register is provided on this input and is clocked in on the falling edge of the SCLK.
2	SCLK	I	Serial Clock. SCLK provides the serial clock for accessing data from the part and writing serial data to the control registers. Also used as a clock source for the ADIS16080 conversion process.
3	DOUT	O	Data Out. The data on this pin represents data being read from the control registers and is clocked on the falling edge of the SCLK.
4	NC		No Connect.
5	RATE	O	Buffered Analog Output. Represents the angular rate signal.
6	FILT	I	External Capacitor Connection to Control Bandwidth.
7	V_{DRIVE}	S	Power to SPI. The voltage supplied to this pin determines the voltage at which the serial interface operates.
8	AIN1	I	External Analog Input Channel 1. Single-ended analog input multiplexed into the on-chip track-and-hold, according to the setting of the ADD0 and ADD1 address bits (see Table 5).
9	AIN2	I	External Analog Input Channel 2. Single-ended analog input multiplexed into the on-chip track-and-hold, according to the setting of the ADD0 and ADD1 address bits (see Table 5).
10	COM	S	Common. Reference point for all circuitry in the ADIS16080.
11	V_{REF}	O	Precision 2.5 V Reference.
12	ST2	I	Self-Test Input 2.
13	ST1	I	Self-Test Input 1.
14	V_{CC}	S	Analog Power.
15	NC		No Connect.
16	$\overline{CS}$	I	Chip Select. Active low. This input frames the serial data transfer and initiates the conversion process.

[1] I = input; O = output; S = power supply.

TYPICAL PERFORMANCE CHARACTERISTICS

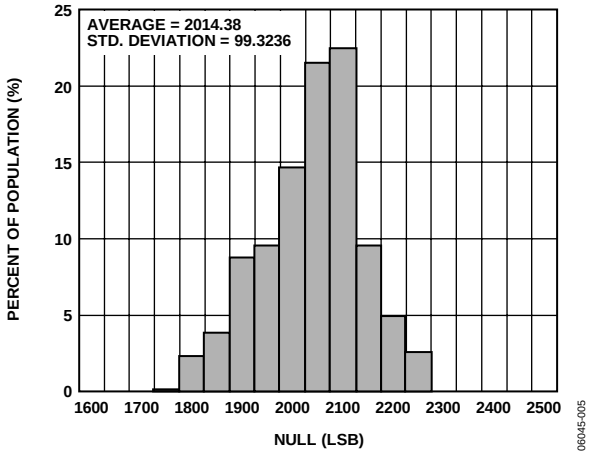

Figure 5. Initial Null Histogram

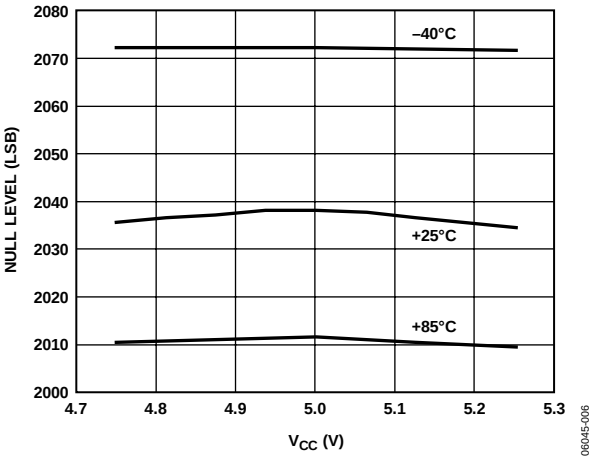

Figure 6. Null Level vs. Supply Voltage

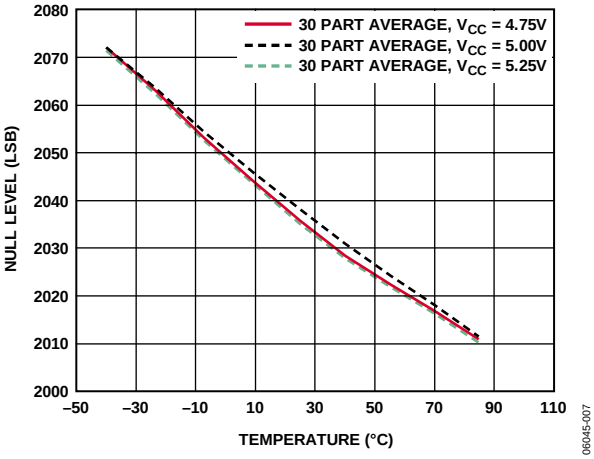

Figure 7. Null Level vs. Temperature

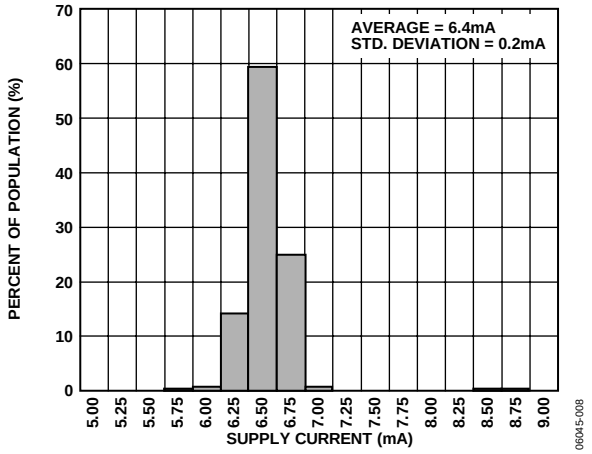

Figure 8. Supply Current Histogram

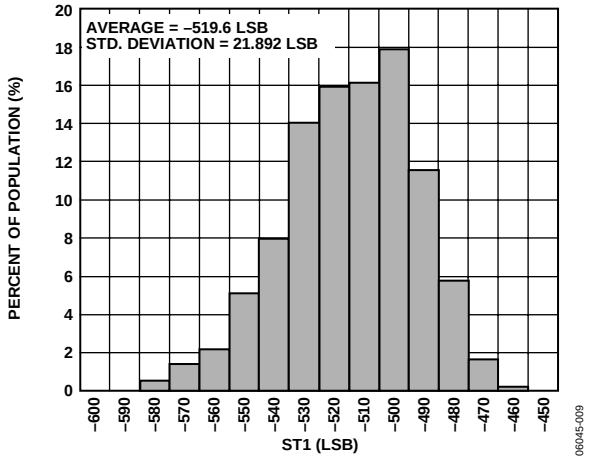

Figure 9. Self Test 1 Histogram

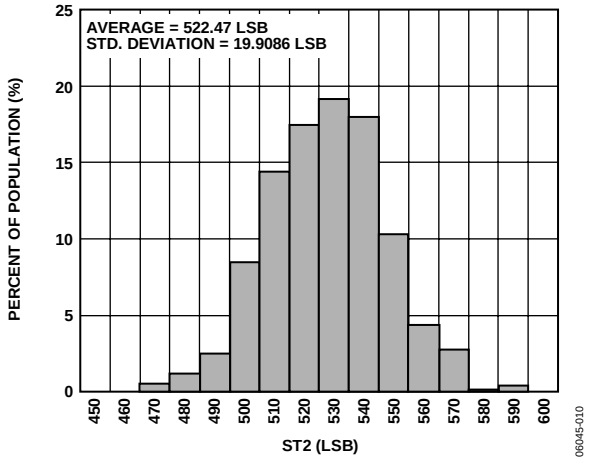

Figure 10. Self Test 2 Histogram

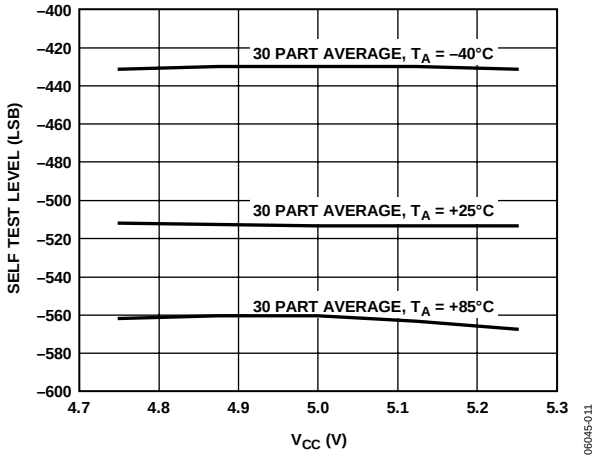

Figure 11. Self Test 1 vs. Supply Voltage

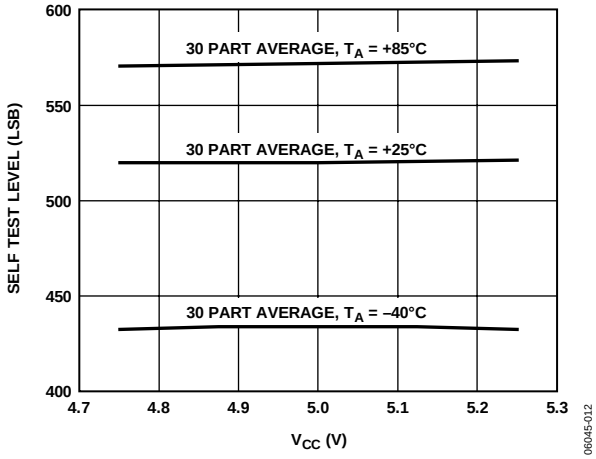

Figure 12. Self Test 2 vs. Supply Voltage

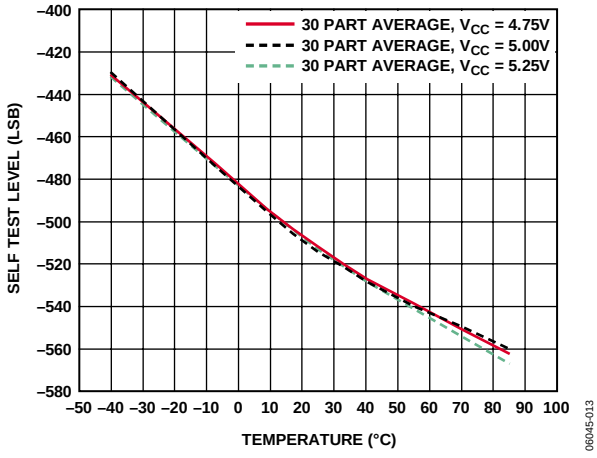

Figure 13. Self Test 1 vs. Temperature

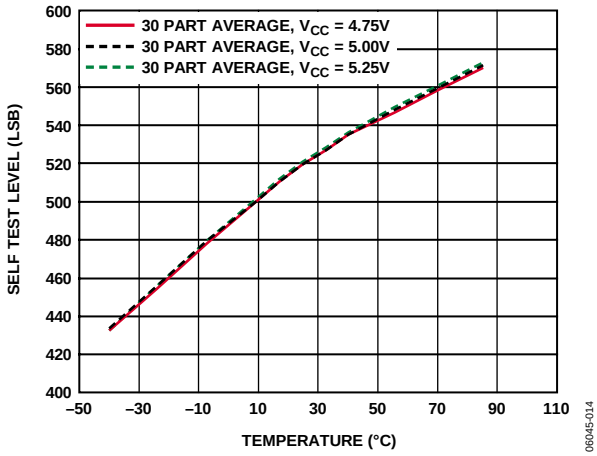

Figure 14. Self Test 2 vs. Temperature

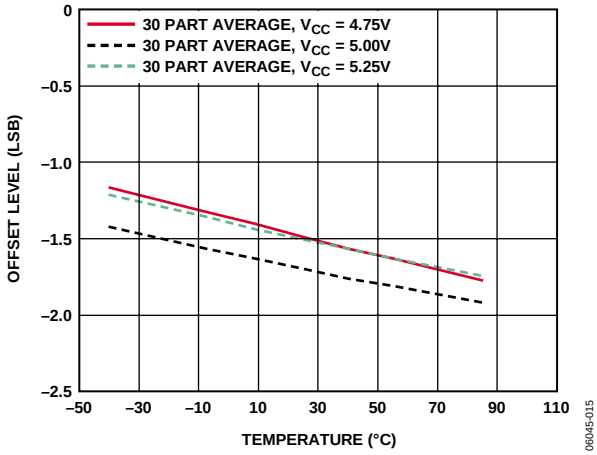

Figure 15. ADC Offset vs. Temperature and Supply Voltage

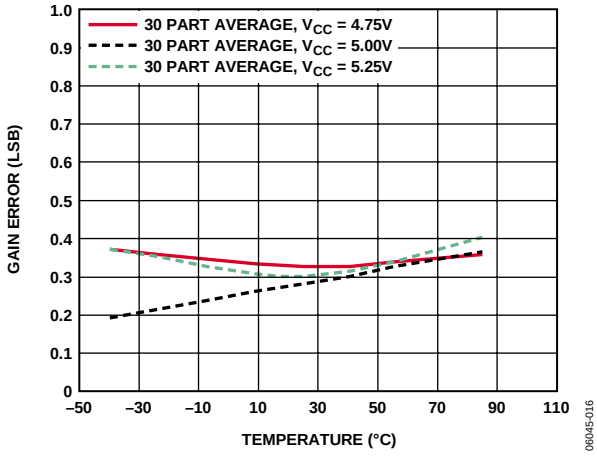

Figure 16. ADC Gain Error vs. Temperature (Excluding V_{REF})

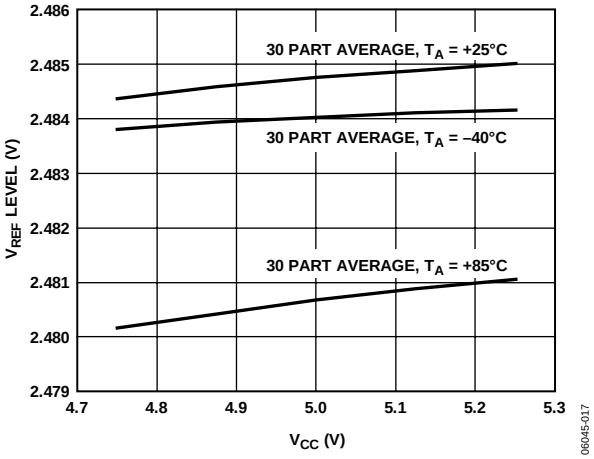

Figure 17. V_{REF} vs. Supply Voltage

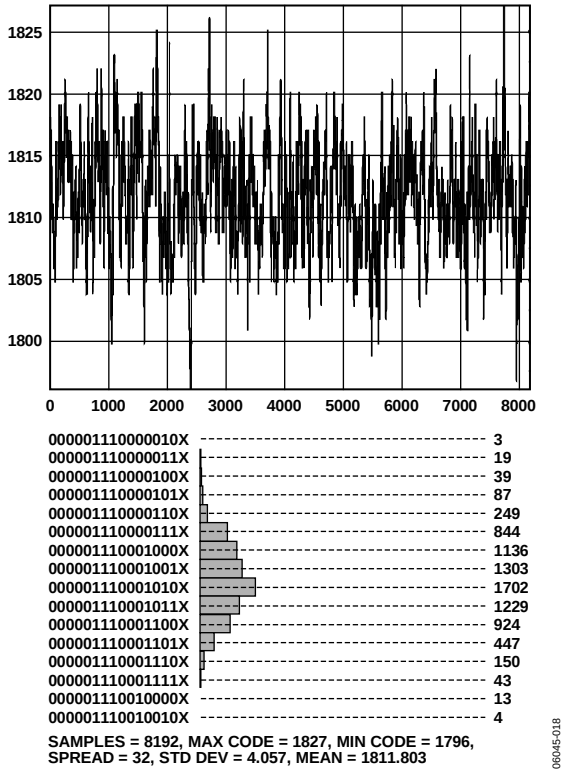

Figure 18. Noise Histogram

THEORY OF OPERATION

The ADIS16080 operates on the principle of a resonator gyro. Two polysilicon sensing structures each contain a dither frame, which is electrostatically driven to resonance. This produces the necessary velocity element to produce a Coriolis force during angular rate. At two of the outer extremes of each frame, orthogonal to the dither motion, are movable fingers that are placed between fixed pickoff fingers to form a capacitive pickoff structure that senses Coriolis motion. The resulting signal is fed to a series of gain and demodulation stages that produce the electrical rate signal output. The rate signal is then converted to a digital representation of the output on the SPI pins. The dual-sensor design rejects external *g* forces and vibration. Fabricating the sensor with the signal conditioning electronics preserves signal integrity in noisy environments.

The electrostatic resonator requires 14 V to 16 V for operation. Because only 5 V is typically available in most applications, a charge pump is included on-chip.

After the demodulation stage, there is a single-pole, low-pass filter included on-chip that is used to limit high frequency artifacts before final amplification. The frequency response is dominated by the second low-pass filter, which is set at 40 Hz. For additional bandwidth reduction options, see the Setting Bandwidth section.

SUPPLY AND COMMON CONSIDERATIONS

Power supply noise and transient behaviors can influence the accuracy and stability of any sensor-based measurement system. When considering the power supply for the ADIS16080, it is important to understand that the ADIS16080 provides 0.2 µF of decoupling capacitance on the V_{CC} pin. Depending on the level of noise present in the system power supply, the ADIS16080 may not require any additional decoupling capacitance for this supply. The analog supply, V_{CC}, and the digital drive supply, V_{DRIVE}, are segmented to allow multiple logic levels to be used in receiving the digital output data. V_{DRIVE} is intended for the down-stream logic power supply and supports standard 3.3 V and 5 V logic families. The V_{DRIVE} supply does not have internal decoupling capacitors.

INCREASING MEASUREMENT RANGE

The full-scale measurement range of the ADIS16080 is increased by placing an external resistor between the RATE pin and FILT pin, which results in a parallel connection with the internal 180 kΩ, 1% resistor. For example, a 330 kΩ external resistor gives ~50% increase in the full-scale range. This is effective for up to a 4× increase in the full-scale range (minimum value of the parallel resistor allowed is 45 kΩ). The internal circuitry headroom requirements prevent further increase in the linear full-scale output range.

The trade-offs associated with increasing the full-scale range are potential increase in output null drift (as much as 2°/sec over temperature) and introducing initial null bias errors that must be calibrated.

SETTING BANDWIDTH

An external capacitor can be used in combination with an on-chip resistor to create a low-pass filter to limit the bandwidth of the ADIS16080 rate response.

The −3 dB frequency is defined as

$$f_{OUT} = 1/\left(2 \times \pi \times R_{OUT} \times \left(C_{OUT} + 0.022\ \mu\text{F}\right)\right)$$

where R_{OUT} represents an internal impedance that was trimmed during manufacturing to 180 kΩ ± 1%.

Any external resistor applied between the RATE pin and the FILT pin results in

$$R_{OUT} = \left(180\ \text{k}\Omega \times R_{EXT}\right)/\left(180\ \text{k}\Omega + R_{EXT}\right)$$

With C_{OUT} = 0 µF, a default −3 dB frequency response of 40 Hz is obtained based upon an internal 0.022 µF capacitor implemented on-chip.

SELF-TEST FUNCTION

The ADIS16080 includes a self-test feature that actuates each of the sensing structures and associated electronics in the same manner as if subjected to angular rate. It provides a simple method for exercising the mechanical structure of the sensor, along with the entire signal processing circuit. It is activated by standard logic high levels applied to inputs ST1, ST2, or both. ST1 causes a change in the digital output equivalent to typically −540 LSB, and ST2 causes an opposite +540 LSB change. The self-test response follows the viscosity temperature dependence of the package atmosphere, approximately 0.25%/°C.

Activating both ST1 and ST2 simultaneously is not damaging. Because ST1 and ST2 are not necessarily closely matched, actuating both simultaneously can result in an apparent null bias shift.

CONTINUOUS SELF TEST

As an additional failure detection measure, power-on self test can be performed. However, some applications can warrant continuous self test while sensing rate.

RATE SENSITIVE AXIS

This is a z-axis rate-sensing device that is also called a yaw rate sensor. It produces a positive going output voltage for clockwise rotation about the axis normal to the package top, that is, clockwise when looking down at the package lid.

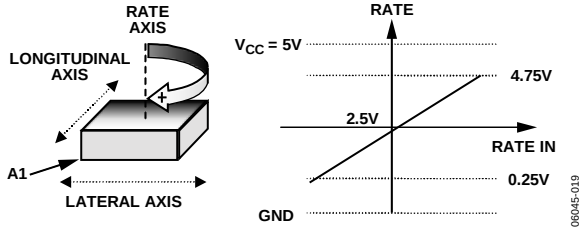

Figure 19. Rate Signal Increases with Clockwise Rotation

CONTROL REGISTER

The control register on the ADIS16080 is a 12-bit, write-only register. Data is loaded from the DIN pin on the falling edge of SCLK. The data is transferred on the DIN line at the same time that the conversion result is read from the part. The data transferred on the DIN line dictates the configuration for the next conversion.

This requires 16 serial clocks for every data transfer. Only the information provided on the first 12 falling clock edges (after $\overline{CS}$ falling edge) is loaded to the control register.

MSB denotes the first bit in the data stream. The DIN Bit Stream bit map shows the analog input channel selection options.

Table 5. Channel Selection

Analog Input Channel	ADD1	ADD0
Gyroscope	0	0
Temperature Sensor	0	1
AIN1 Input	1	0
AIN2 Input	1	1

DIN Bit Stream

MSB (11) **LSB (0)**

WRITE	LOW	DONTC	DONTC	ADD1	ADD0	HIGH	HIGH	DONTC	DONTC	LOW	CODING

Table 6. Analog Input Channel Selection Options

Bit	Mnemonic	Comments
11	WRITE	The value written to this bit of the control register determines whether the following 11 bits are loaded to the control register or not. If this bit is a 1, the following 11 bits are written to the control register. If it is a 0, the remaining 11 bits are not loaded to the control register, and it remains unchanged.
10	LOW	This bit should be low.
9, 8	DONTC	Don't care.
7, 6	ADD1, ADD0	These two address bits are loaded at the end of the present conversion sequence and select which analog input channel is to be converted in the next serial transfer. The selected input channel is decoded as shown in Table 5. The address bits corresponding to the conversion result are output on DOUT prior to the 12 bits of data. The next channel to be converted is selected by the mux on the 14th SCLK falling edge.
5, 4	HIGH	These bits should be high.
3, 2	DONTC	Don't care.
1	LOW	This bit should be low.
0	CODING	This bit selects the type of output coding used for the conversion result. If this bit is set to 0, the output coding for the part is twos complement. If this bit is set to 1, the output coding from the part is straight binary (for the next conversion).

SERIAL INTERFACE

Figure 2 shows the detailed timing diagram for the serial interface to the ADIS16080. The chip select signal, $\overline{CS}$, frames the entire data transfer, because it must be kept in a Logic 0 state to communicate with the ADIS16080. The serial clock, SCLK, provides the conversion clock and controls the transfer of information to and from the ADIS16080 during each conversion cycle. The data input, DIN, provides access to critical control parameters in the control register; and the output signal, DOUT, provides access to the ADIS16080 output data.

The ADIS16080 offers an efficient data transfer function by supporting simultaneous READ and WRITE cycles. A data transfer cycle is started when the $\overline{CS}$ transitions to a Logic 0 state. If DIN is in a Logic 1 state during the first falling edge of the SCLK, then the next 11 SCLK cycles fill the control register with the contents on the DIN pin. The appropriate bit definitions for DIN can be found in the DIN Bit Stream bit map and Table 6. If DIN is in a Logic 0 state during the first falling edge of the SCLK, then the contents of the control register remain unchanged. Because the control register is only 12 bits wide, the contents on the DIN pin during the last four SCLK cycles are ignored.

During this same cycle, the digital output data is clocked out on the DOUT pin. The 12 bits of data are preceded by two leading 0s and two channel address bits, ADD1 and ADD0, identifying to which channel the result corresponds (see the Reading DOUT Bit Stream bit map and Table 7).

$\overline{CS}$ going low clocks out the first leading zero to be read in by the system microcontroller or DSP on the first falling edge of SCLK. The first falling edge of SCLK will also clock out the second leading zero to be read in by the microcontroller or DSP on the second SCLK falling edge, and so on.

The remaining two address bits and 12 bits are then clocked out by subsequent SCLK falling edges, beginning with the first address bit, ADD1; thus, the second falling clock edge on the serial clock has the second leading 0 provided and also clocks out Address Bit ADD1. The final bit in the data transfer is valid on the 16th falling edge, having been clocked out on the previous (15th) falling edge.

After the 16th falling edge of SCLK, the DOUT line goes back into a three-state mode. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the DOUT line goes back into three-state mode and the control register is not updated. Otherwise, DOUT returns to a three-state mode on the 16th SCLK falling edge, as shown in Figure 2.

For the analog inputs, the $\overline{CS}$ signal initiates the data transfer and conversion process. The falling edge of $\overline{CS}$ put the track and hold into hold mode and takes the bus out of the three-state. The analog input is sampled at this point. The conversion is also initiated at this point and requires 16 SCLK cycles to complete.

Reading DOUT Bit Stream

SCLK1															**SCLK16**
LOW	LOW	ADD1	ADD0	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Table 7. DOUT Bit Functions

SCLK	Mnemonic	Comments
1, 2	LOW	The outputs are low for SCLK1 and SCLK2.
3, 4	ADD1, ADD0	The address bits corresponding to the conversion result are output on DOUT prior to the 12 bits of data. See Table 5 for the coding of these address bits.
5	DB11	Data Bit 11 (MSB).
6 to 15	DB10 to DB1	Data Bit 10 to Data Bit 1.
16	DB0	Data Bit 0 (LSB).

SECOND-LEVEL ASSEMBLY

The ADIS16080 can be attached to the second-level assembly board using Sn63 (or equivalent) or an RoHS-compliant solder. Figure 21 and Table 8 provide acceptable solder reflow profiles for each solder type. Note that these profiles may not be the optimum profile for the user's application. In no case shall the 260°C limit be exceeded. It is recommended that the user develop a reflow profile based upon the specific application. In general, keep in mind the lowest peak temperature and shortest dwell time above the melt temperature of the solder results in less shock and stress to the product. In addition, evaluating the cooling rate and peak temperature can result in a more reliable assembly.

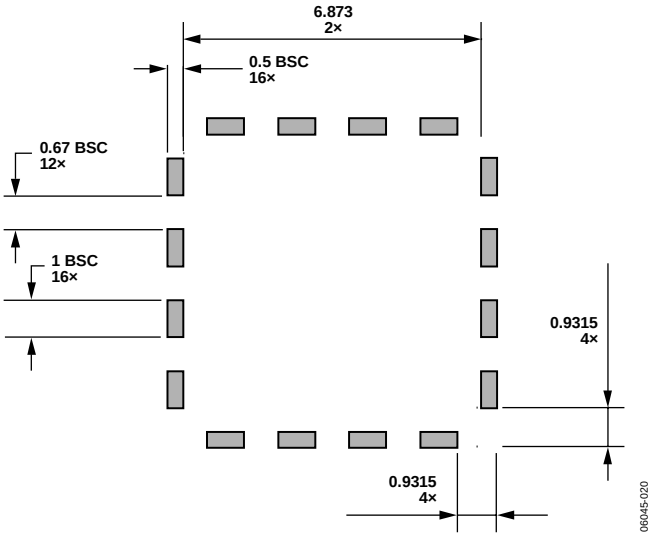

Figure 20. Second Level Assembly Pad Layout

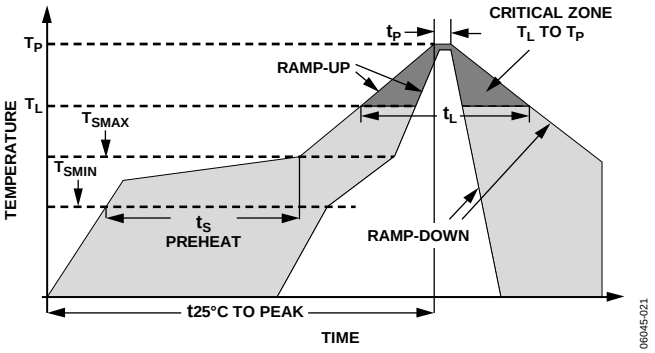

Figure 21. Recommended Solder Reflow Profiles

Table 8.

	Condition	
Profile Feature	**Sn63/Pb37**	**Pb-Free**
Average Ramp Rate (T_L to T_P)	3°C/sec max	3°C/sec max
Preheat		
Minimum Temperature (T_{SMIN})	100°C	150°C
Maximum Temperature (T_{SMAX})	150°C	200°C
Time (T_{SMIN} to T_{SMAX}) (t_S)	60 sec to 120 sec	60 sec to 150 sec
T_{SMAX} to T_L		
Ramp-Up Rate	3°C/sec	3°C/sec
Time Maintained Above Liquidous (T_L)		
Liquidous Temperature (T_L)	183°C	217°C
Time (t_L)	60 sec to 150 sec	60 sec to 150 sec
Peak Temperature (T_P)	240°C + 0°C/–5°C	260°C + 0°C/–5°C
Time Within 5°C of Actual Peak Temperature (t_P)	10 sec to 30 sec	20 sec to 40 sec
Ramp-Down Rate	6°C/sec max	6°C/sec max
Time 25°C to Peak Temperature	6 min max	8 min max

OUTLINE DIMENSIONS

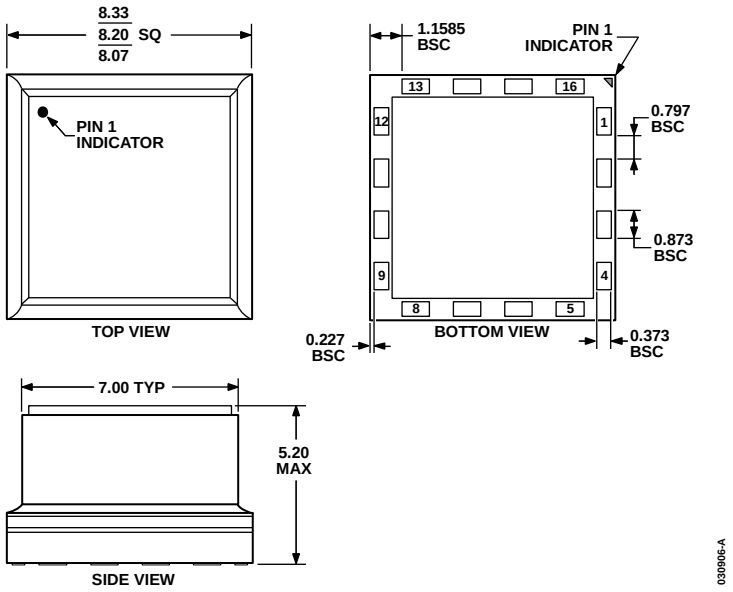

Figure 22. 16-Terminal Land Grid Array [LGA]
(CC-16-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADIS16080ACCZ[1]	−40°C to +85°C	16-Terminal Land Grid Array (LGA)	CC-16-1
ADIS16080/PCBZ[1]		Evaluation Board	

[1] Z = Pb-free part.

NOTES

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