ANALOG DEVICES

Digital Power Monitor with Clear Pin and ALERT Output

ADM1192

FEATURES

- Powered from 3.15 V to 26 V
- Precision current sense amplifier
- Precision voltage input
- 12-bit ADC for current and voltage readback
- ALERT output allows basic P-channel FET hot swap up to 26 V
- SETV input for setting overcurrent alert threshold
- Programmable overcurrent filtering via TIMER pin
- CLRB input pin
- I²C® fast mode-compliant interface (400 kHz maximum)
- 10-lead MSOP

APPLICATIONS

- Power monitoring/power budgeting
- Central office equipment
- Telecommunication and data communication equipment
- PCs/servers

GENERAL DESCRIPTION

The ADM1192 is an integrated current sense amplifier that offers digital current and voltage monitoring via an on-chip, 12-bit analog-to-digital converter (ADC), communicated through an I²C interface.

An internal current sense amplifier senses voltage across the sense resistor in the power path via the VCC pin and the SENSE pin.

A 12-bit ADC can measure the current seen in the sense resistor and in the supply voltage on the VCC pin. An industry-standard I²C interface allows a controller to read current and voltage data from the ADC. Measurements can be initiated by an I²C command. Alternatively, the ADC can run continuously, and the user can read the latest conversion data whenever it is required. Up to four unique I²C addresses can be created, depending on the way the ADR pin is connected.

A SETV pin is also included. A voltage applied to this pin is internally compared to the output voltage on the current sense amplifier. The output of the SETV comparator asserts when the current sense amplifier output exceeds the SETV voltage. This event is detected at the ALERT block. The ALERT block then charges up the external TIMER capacitor with a fixed current. When this timing cycle is complete, the ALERT output asserts.

FUNCTIONAL BLOCK DIAGRAM

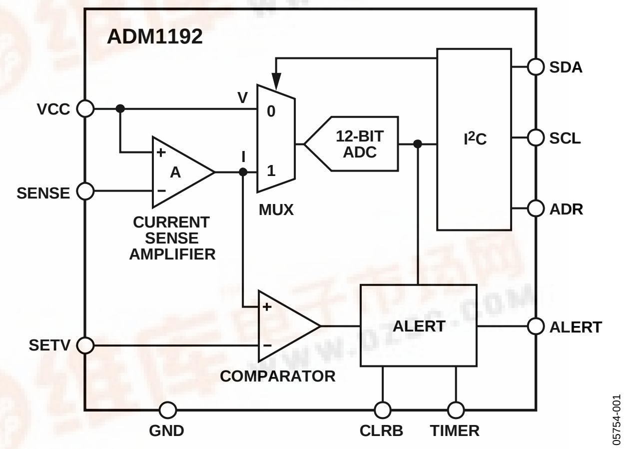

Figure 1.

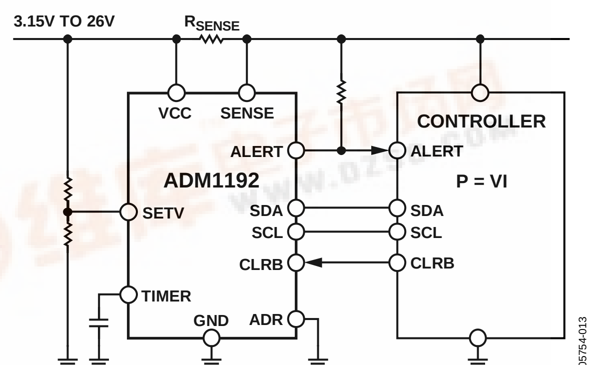

Figure 2. Applications Diagram

The ALERT output can be used as a flag to warn a microcontroller or field programmable gate array (FPGA) of an overcurrent condition. ALERT outputs of multiple ADM1192 devices can be tied together and used as a combined alert.

A basic P-channel FET hot swap circuit can be implemented with the ALERT output. The value of the TIMER capacitor should be set so that the charging time of this capacitor is much longer than the period where a higher than nominal inrush current may be flowing.

The ADM1192 is packaged in a 10-lead MSOP.

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REVISION HISTORY

9/06—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3.15 V to 26 V; T_A = −40°C to +85°C; typical values at T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Conditions	
VCC PIN						
Operating Voltage Range, V_{VCC}	3.15		26	V		
Supply Current, I_{CC}		1.7	2	mA		
Undervoltage Lockout, V_{UVLO}		2.8		V	V_{CC} rising	
Undervoltage Lockout Hysteresis, $V_{UVLOHYST}$		80		mV		
MONITORING ACCURACY[1]						
Current Sense Absolute Accuracy	−1.45		+1.45	%	V_{SENSE} = 75 mV	0°C to +70°C
	−1.8		+1.8	%	V_{SENSE} = 50 mV	0°C to +70°C
	−2.8		+2.8	%	V_{SENSE} = 25 mV	0°C to +70°C
	−5.7		+5.7	%	V_{SENSE} = 12.5 mV	0°C to +70°C
	−1.5		+1.5	%	V_{SENSE} = 75 mV	0°C to +85°C
	−1.8		+1.8	%	V_{SENSE} = 50 mV	0°C to +85°C
	−2.95		+2.95	%	V_{SENSE} = 25 mV	0°C to +85°C
	−6.1		+6.1	%	V_{SENSE} = 12.5 mV	0°C to +85°C
	−1.95		+1.95	%	V_{SENSE} = 75 mV	−40°C to +85°C
	−2.45		+2.45	%	V_{SENSE} = 50 mV	−40°C to +85°C
	−3.85		+3.85	%	V_{SENSE} = 25 mV	−40°C to +85°C
	−6.7		+6.7	%	V_{SENSE} = 12.5 mV	−40°C to +85°C
V_{SENSE} for ADC Full Scale		105.84		mV	This is an absolute value to be used when converting ADC codes to current readings; any inaccuracy in this value is factored into absolute current accuracy values (see specs for Current Sense Absolute Accuracy)	
Voltage Sense Accuracy	−0.85		+0.85	%	V_{VCC} = 3.0 V to 5.5 V (low range)	0°C to +70°C
	−0.9		+0.9	%	V_{VCC} = 10.8 V to 16.5 V (high range)	0°C to +70°C
	−0.85		+0.85	%	V_{VCC} = 3.0 V to 5.5 V (low range)	0°C to +85°C
	−0.9		+0.9	%	V_{VCC} = 10.8 V to 16.5 V (high range)	0°C to +85°C
	−0.9		+0.9	%	V_{VCC} = 3.0 V to 5.5 V (low range)	−40°C to +85°C
	−1.15		+1.15	%	V_{VCC} = 10.8 V to 16.5 V (high range)	−40°C to +85°C
V_{CC} for ADC Full Scale, Low Range (VRANGE = 1)		6.65		V	These are absolute values to be used when converting ADC codes to voltage readings; any inaccuracy in these values is factored into voltage accuracy values (see specs for Voltage Accuracy)	
V_{CC} for ADC Full Scale, High Range (VRANGE = 0)		26.52		V		
CLRB PIN						
Logic Low Threshold, V_{CLRBL}			0.8	V		
Input Current for Logic Low Input, I_{CLRBL}	−40	−22		µA	V_{CLRB} = 0 V to 0.8 V	
Logic High Threshold, V_{CLRBH}	1.6			mV		
Input Current for Logic High Input, I_{CLRBH}		3	6	µA	V_{CLRB} = 1.6 V to 5.5 V	
SENSE PIN						
Input Current, I_{SENSE}	−1		+1	µA	V_{SENSE} = V_{VCC}	

Parameter	Min	Typ	Max	Unit	Conditions
SETV PIN					
Overcurrent Trip Threshold	98	100	102	mV	V_{SETV} = 1.8 V
	49.5	50	50.5	mV	V_{SETV} = 0.9 V
Overcurrent Trip, Gain $\{V_{SETV}/(V_{VCC} - V_{SENSE})\}$		18			V_{SETV} = 0.9 V to 1.9 V
Input Current, $I_{SETVLEAK}$	−1		+1	µA	V_{SETV} = 0.9 V to 1.9 V
Glitch Filter, $t_{SETVGLITCH}$		3		µs	
TIMER PIN					
Pull-Up Current (Overcurrent Fault), $I_{TIMERUPOC}$	−46	−62	−78	µA	(18.125 × V_{SENSE}) > V_{SETV}, V_{TIMER} = 1 V
Pull-Down Current, $I_{TIMERDN}$		100		µA	Normal Operation, V_{TIMER} = 1 V
Pin Threshold High, V_{TIMERH}	1.275	1.3	1.325	V	TIMER rising
ALERT PIN					
Output Low Voltage, $V_{ALERTOL}$		0.05	0.1	V	I_{ALERT} = −100 µA
		1	1.5	mA	I_{ALERT} = −2 mA
Input Current, I_{ALERT}	−1		+1	µA	V_{ALERT} = V_{CC}; ALERT asserted
ADR PIN					
Set Address to 00, $V_{ADRLOWV}$	0		0.8	V	Low state
Set Address to 01, $R_{ADRLOWZ}$	80	120	160	kΩ	Resistor to ground state, load pin with specified resistance for 01 decode
Set Address to 10, $I_{ADRHIGHZ}$	−0.3		+0.3	µA	Open state, maximum load allowed on ADR pin for 10 decode
Set Address to 11, $V_{ADRHIGHV}$	2		5.5	V	High state
Input Current for 00 Decode, I_{ADRLOW}		3	6	µA	V_{ADR} = 2.0 V to 5.5 V
Input Current for 11 Decode, $I_{ADRHIGH}$	−40	−25		µA	V_{ADR} = 0 V to 0.8 V
I²C TIMING					
Low Level Input Voltage, V_{IL}			0.3 V_{BUS}	V	
High Level Input Voltage, V_{IH}	0.7 V_{BUS}			V	
Low Level Output Voltage on SDA, V_{OL}			0.4	V	I_{OL} = 3 mA
Output Fall Time on SDA from V_{IHMIN} to V_{ILMAX}	20 + 0.1 C_B		250	ns	C_B = bus capacitance from SDA to GND
Maximum Width of Spikes Suppressed by Input Filtering on SDA and SCL Pins	50		250	ns	
Input Current, I_I, on SDA/SCL When not Driving Out a Logic Low	−10		+10	µA	
Input Capacitance on SDA/SCL		5		pF	
SCL Clock Frequency, f_{SCL}			400	kHz	
Low Period of the SCL Clock	600			ns	
High Period of the SCL Clock	1300			ns	
Setup Time for Repeated Start Condition, $t_{SU;STA}$	600			ns	
SDA Output Data Hold Time, $t_{HD;DAT}$	100		900	ns	
Setup Time for a Stop Condition, $t_{SU;STO}$	600			ns	
Bus Free Time Between a Stop and a Start Condition, t_{BUF}	1300			ns	
Capacitive Load for Each Bus Line			400	pF	

[1] Monitoring accuracy is a measure of the error in a code that is read back for a particular voltage/current. This is a combination of amplifier error, reference error, ADC error, and error in ADC full-scale code conversion factor.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
VCC Pin	30 V
SENSE Pin	30 V
TIMER Pin	−0.3 V to +6 V
CLRB Pin	−0.3 V to +6 V
SETV Pin	30 V
ALERT Pin	30 V
SDA Pin, SCL Pin	−0.3 V to +6 V
ADR Pin	−0.3 V to +6 V
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	Unit
10-Lead MSOP	137.5	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

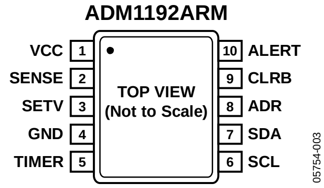


Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VCC	Positive Supply Input Pin. The operating supply voltage range is 3.15 V to 26 V. An undervoltage lockout (UVLO) circuit resets the ADM1192 when a low supply voltage is detected.
2	SENSE	Current Sense Input Pin. A sense resistor between the VCC pin and the SENSE pin generates a voltage across a sense resistor. This voltage is proportional to the load current. A current sense amplifier amplifies this voltage before it is digitized by the ADC.
3	SETV	Input Pin. The voltage driven onto this pin is compared to the output of the internal current sense amplifier. The lower the voltage on the SETV, the lower the current level that causes the ALERT output to assert.
4	GND	Chip Ground Pin.
5	TIMER	Timer Input Pin. An external capacitor, C_{TIMER}, sets the timing period for masking overcurrent conditions. This timing period should be sufficient to allow the load charge up completely with maximum current at startup without tripping an overcurrent fault.
6	SCL	I^2C Clock Pin. Open-drain input; requires an external resistive pull-up.
7	SDA	I^2C Data I/O Pin. Open-drain input/output; requires an external resistive pull-up.
8	ADR	I^2C Address Pin. This pin can be tied low, tied high, left floating, or tied low through a resistor to set four different I^2C addresses.
9	CLRB	Clear Pin. A latched overcurrent condition can be cleared by pulling this pin low.
10	ALERT	Alert Output Pin. Active high, open-drain configuration. This pin asserts high when an overcurrent condition is present. The level at which an overcurrent condition is detected depends on the voltage on the SETV pin.

TYPICAL PERFORMANCE CHARACTERISTICS

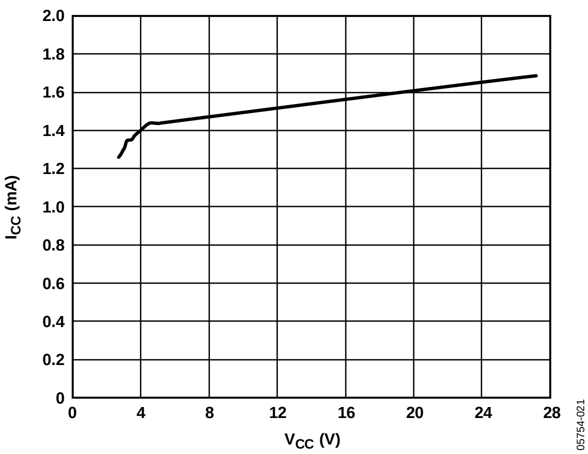


Figure 4. Supply Current vs. Supply Voltage

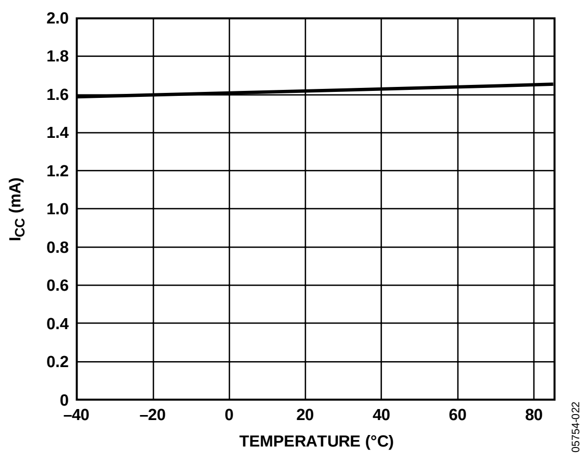


Figure 5. Supply Current vs. Temperature

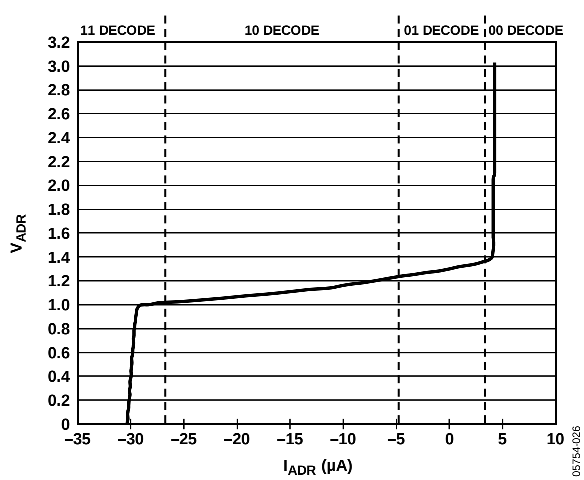


Figure 6. Address Pin Voltage vs. Address Pin Current for Four Addressing Options

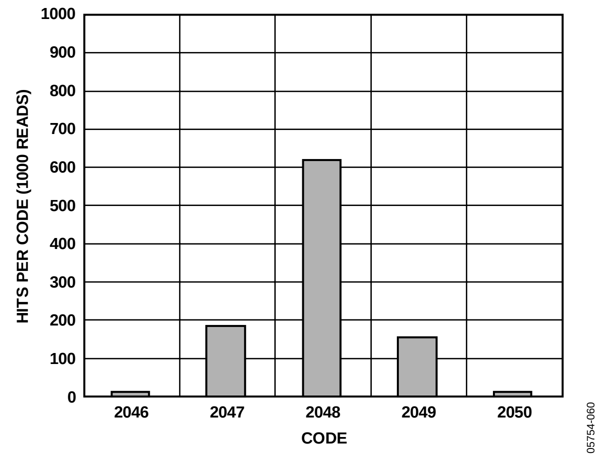


Figure 7. ADC Noise, Current Channel, Midcode Input, 1000 Reads

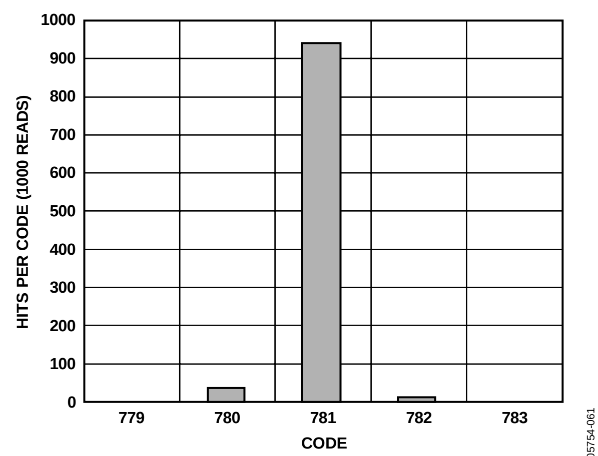


Figure 8. ADC Noise, 14:1 Voltage Channel, 5 V Input, 1000 Reads

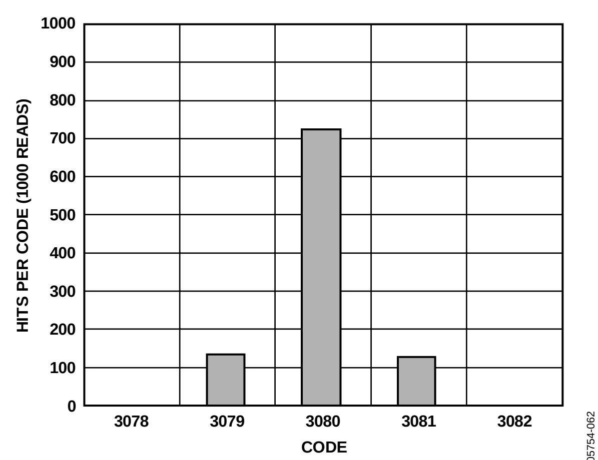


Figure 9. ADC Noise, 7:1 Voltage Channel, 5 V Input, 1000 Reads

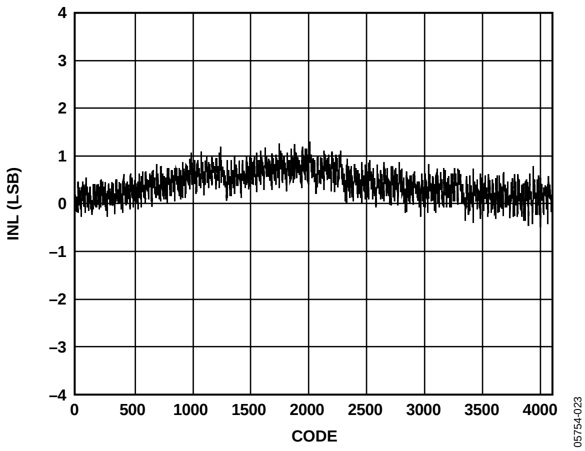


Figure 10. INL for ADC

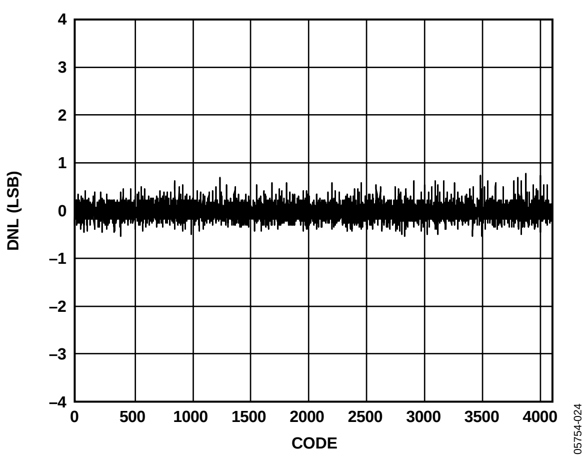


Figure 11. DNL for ADC

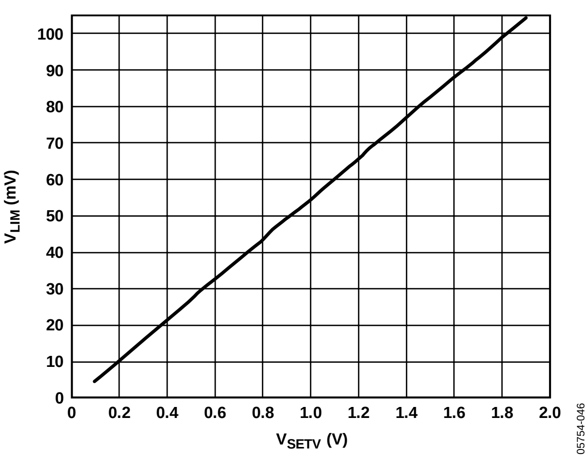


Figure 12. V_{LIM} vs. V_{SETV}

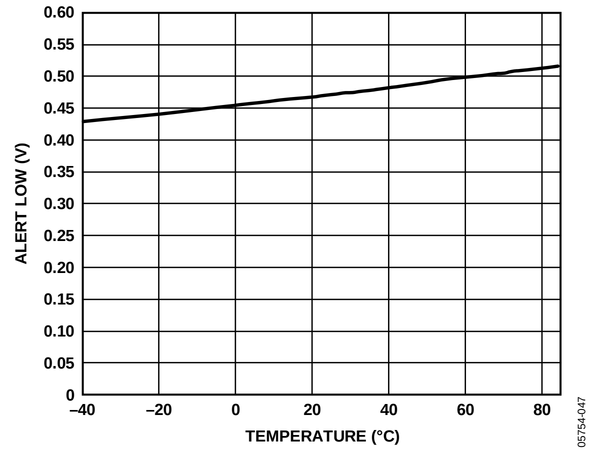


Figure 13. ALERT Output Low Voltage vs. Temperature @ 1 mA

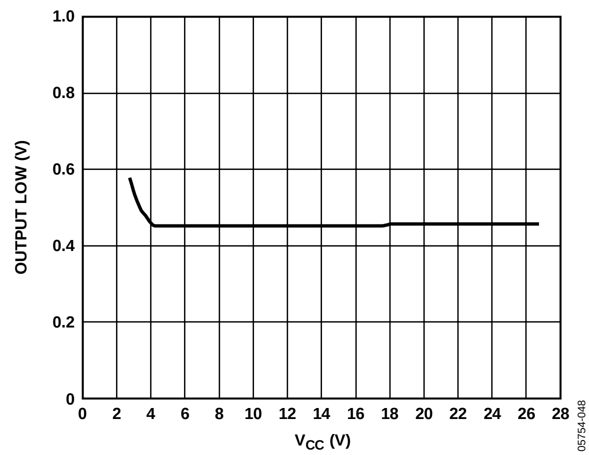


Figure 14. ALERT Output Low Voltage vs. Supply @ 1 mA

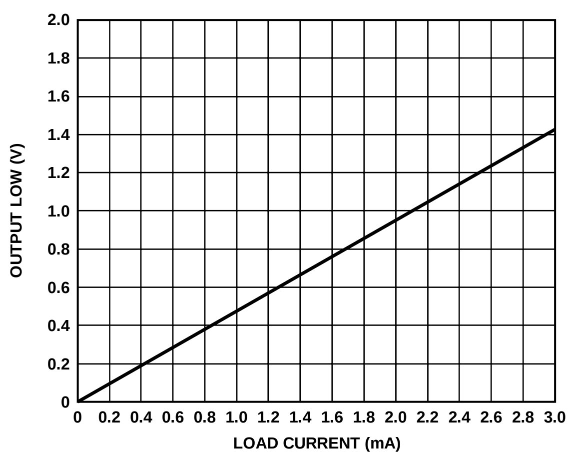


Figure 15. ALERT Output Low Voltage vs. Load Current

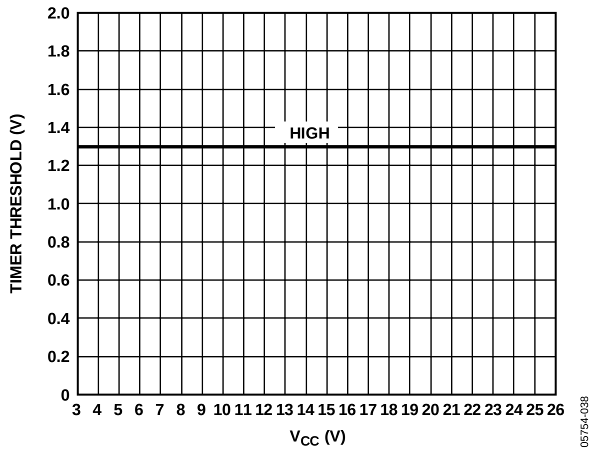


Figure 16. Timer Threshold vs. Supply Voltage

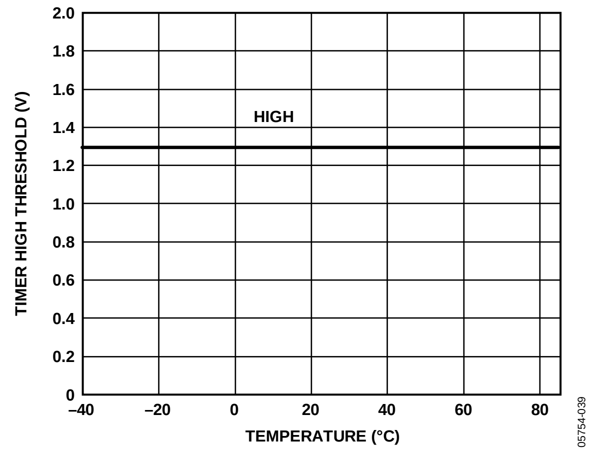


Figure 17. Timer Threshold vs. Temperature

VOLTAGE AND CURRENT READBACK

The ADM1192 contains the components to allow voltage and current readback over an Inter-IC (I^2C) bus. The voltage output of the current sense amplifier and the voltage on the VCC pin are fed into a 12-bit ADC via a multiplexer. The device can be instructed to convert voltage and/or current at any time during operation via an I^2C command. When all conversions are complete, the voltage and/or current values can be read out to 12-bit accuracy in two or three bytes.

SERIAL BUS INTERFACE

Control of the ADM1192 is carried out via the serial system management bus (I^2C). This interface is compatible with I^2C fast mode (400 kHz maximum). The ADM1192 is connected to this bus as a slave device, under the control of a master device.

IDENTIFYING THE ADM1192 ON THE I^2C BUS

The ADM1192 has a 7-bit serial bus slave address. When the device powers up, it does so with a default serial bus address. The five MSBs of the address are set to 01011; the two LSBs are determined by the state of the ADR pin. There are four different configurations available on the ADR pin that correspond to four different I^2C addresses for the two LSBs (see Table 5). This scheme allows four ADM1192 devices to operate on a single I^2C.

Table 5. Setting I^2C Addresses via the ADR Pin

ADR Configuration	Address
Low state	0x68
Resistor to GND	0x69
Floating (unconnected)	0x6A
High state	0x6B

GENERAL I^2C TIMING

Figure 18 and Figure 19 show timing diagrams for general read and write operations using the I^2C. The I^2C specification defines conditions for different types of read and write operations, which are discussed later. The general I^2C protocol operates as follows:

1. The master initiates data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit slave address (MSB first) plus an $R/\overline{W}$ bit that determines the direction of the data transfer; that is, whether data is written to or read from the slave device (0 = write, 1 = read).

   The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus now remain idle while the selected device waits for data to be read from it or written to it. If the $R/\overline{W}$ bit is 0, the master writes to the slave device. If the $R/\overline{W}$ bit is 1, the master reads from the slave device.

2. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low-to-high transition when the clock is high can be interpreted as a stop signal.

   If the operation is a write operation, the first data byte after the slave address is a command byte. This tells the slave device what to expect next. It can be an instruction, such as telling the slave device to expect a block write, or it can be a register address that tells the slave where subsequent data is to be written.

   Because data can flow in only one direction, as defined by the $R/\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before doing a read operation, it may first be necessary to do a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.

3. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, then high during the 10th clock pulse to assert a stop condition.

TIMING DIAGRAMS

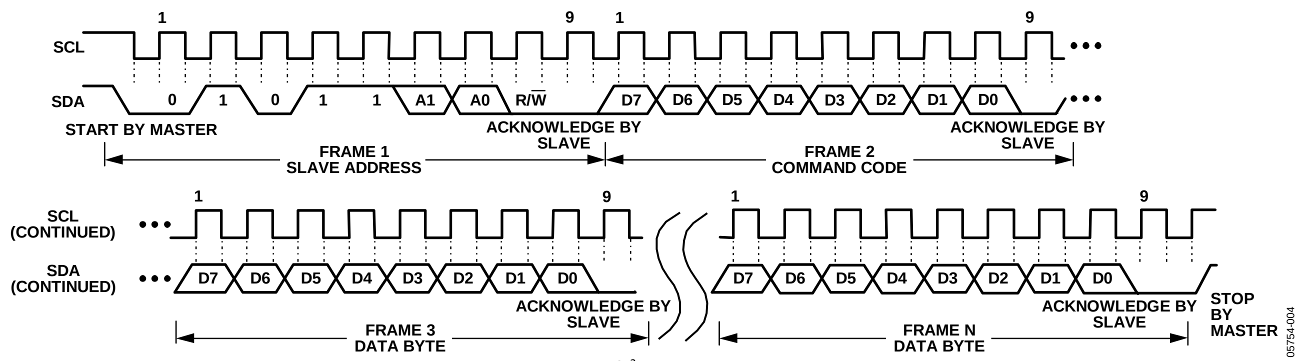


Figure 18. General I²C Write Timing Diagram

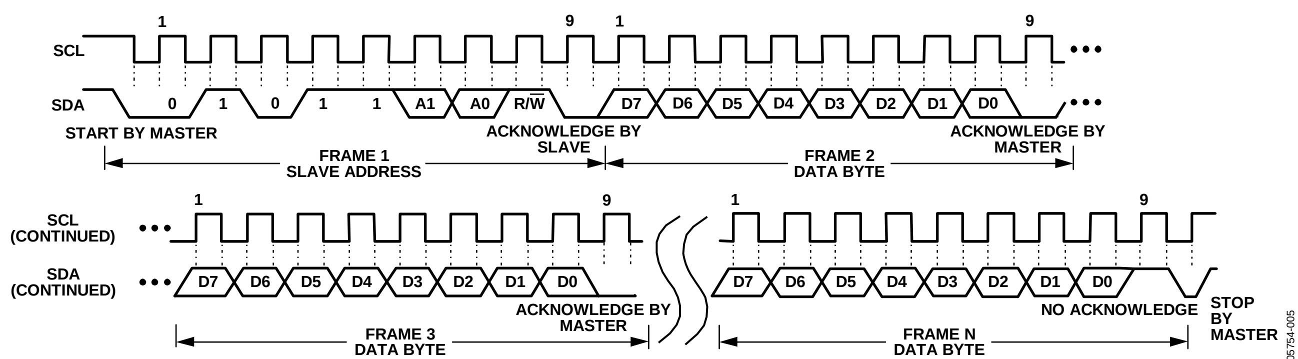


Figure 19. General I²C Read Timing Diagram

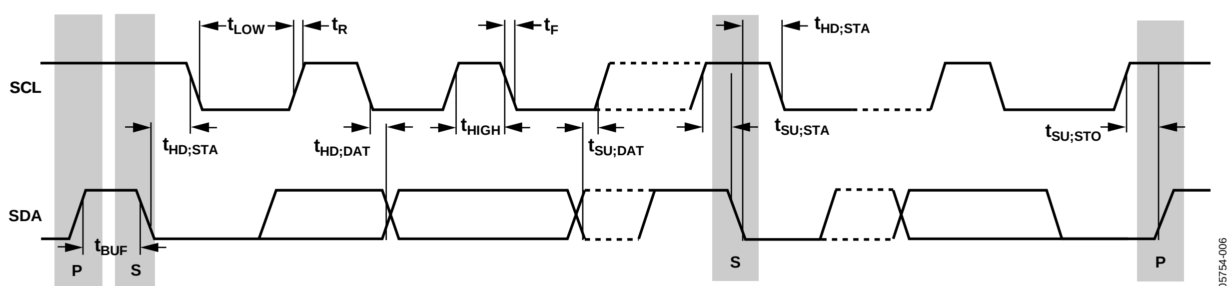


Figure 20. Serial Bus Timing Diagram

WRITE AND READ OPERATIONS

The I²C specification defines several protocols for different types of read and write operations. The operations used in the ADM1192 are discussed in the sections that follow. Table 6 shows the abbreviations used in the command diagrams.

Table 6. I²C Abbreviations

Abbreviation	Condition
S	Start
P	Stop
R	Read
W	Write
A	Acknowledge
N	No acknowledge

QUICK COMMAND

The quick command operation allows the master to check if the slave is present on the bus, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.

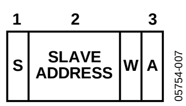


Figure 21. Quick Command

WRITE COMMAND BYTE

In the write command byte operation, the master device sends a command byte to the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends the command byte. The command byte is identified by an MSB = 0. An MSB =1 indicates an extended register write (see the Write Extended Byte section).
5. The slave asserts an acknowledge on SDA.
6. The master asserts a stop condition on SDA to end the transaction.

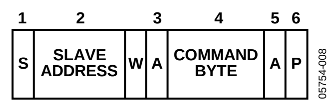


Figure 22. Write Command Byte

The seven LSBs of the command byte are used to configure and control the ADM1192. Table 7 provides details of the function of each bit.

Table 7. Command Byte Operations

Bit	Default	Name	Function
C0	0	V_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1192 asserts an acknowledge and returns all 0s in the returned data.
C1	0	V_ONCE	Set to convert voltage once. Self-clears. I²C asserts a no acknowledge on attempted reads until ADC conversion is complete.
C2	0	I_CONT	Set to convert voltage continuously. If readback is attempted before the first conversion is complete, the ADM1192 asserts an acknowledge and returns all 0s in the returned data.
C3	0	I_ONCE	Set to convert current once. Self-clears. I²C asserts a no acknowledge on attempted reads until ADC conversion is complete.
C4	0	VRANGE	Selects different internal attenuation resistor networks for voltage readback. A 0 in C4 selects a 14:1 voltage divider. A 1 in C4 selects a 7:2 voltage divider. With an ADC full scale of 1.902 V, the voltage at the VCC pin for an ADC full-scale result is 26.52 V for VRANGE = 0 and 6.65 V for VRANGE = 1.
C5	0	N/A	Unused.
C6	0	STATUS_RD	Status Read. When this bit is set, the data byte read back from the ADM1192 is the STATUS byte. This contains the status of the device alerts. See Table 15 for full details of the STATUS byte.

WRITE EXTENDED BYTE

In the write extended byte operation, the master device writes to one of the three extended registers of the slave device, as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends the register address byte. The MSB of this byte is set to 1 to indicate an extended register write. The two LSBs indicate which of the three extended registers are to be written to (see Table 8). All other bits should be set to 0.
5. The slave asserts an acknowledge on SDA.
6. The master sends the command byte. The command byte is identified by an MSB = 0. An MSB = 1 indicates an extended register write.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

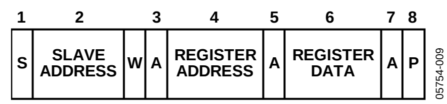


Figure 23. Write Extended Byte

Table 9, Table 10, and Table 11 give details of each extended register.

Table 8. Extended Register Addresses

A6	A5	A4	A3	A2	A1	A0	Extended Register
0	0	0	0	0	0	1	ALERT_EN
0	0	0	0	0	1	0	ALERT_TH
0	0	0	0	0	1	1	CONTROL

Table 9. ALERT_EN Register Operations

Bit	Default	Name	Function
0	0	EN_ADC_OC1	Enabled if a single ADC conversion on the I channel has exceeded the threshold set in the ALERT_TH register.
1	0	EN_ADC_OC4	Enabled if four consecutive ADC conversions on the I channel have exceeded the threshold set in the ALERT_TH register.
2	1	EN_OC_ALERT	Enables the OC_ALERT register. If an overcurrent condition is present and the TIMER pin has charged to 1.3 V, the OC_ALERT register captures and latches this condition.
3	0	EN_OFF_ALERT	Enables an alert if the HS operation is turned off by an operation that writes the SWOFF bit high. This allows software override of the ALERT output and turns on a P-channel FET controlled by ALERT.
4	0	CLEAR	Clears the OC_ALERT and ADC_ALERT status bits in the status register. These may immediately reset if the source of the alert has not been cleared or disabled with the other bits in this register. This bit self-clears to 0 after the status register bits have been cleared.

Table 10. ALERT_TH Register Operations

Bit	Default	Function
7:0	FF	The ALERT_TH register sets the current level at which an alert occurs. Defaults to ADC full scale. The ALERT_TH 8-bit number corresponds to the top eight bits of the current channel data.

Table 11. CONTROL Register Operations

Bit	Default	Name	Function
0	0	SWOFF	Forces the ALERT pin to deassert. Can be active only if the EN_OFF_ALERT bit is high (see Table 9).

READ VOLTAGE AND/OR CURRENT DATA BYTES

The ADM1192 can be set up to provide information in three different ways (see the Write Command Byte section). Depending on how the device is configured, the following data can be read out of the device after a conversion (or conversions).

Voltage and Current Readback

The ADM1192 digitizes both voltage and current. Three bytes are read out of the device in the format shown in Table 12.

Table 12. Voltage and Current Readback Format

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
3	LSBs	V3	V2	V1	V0	I3	I2	I1	I0

Voltage Readback

The ADM1192 digitizes voltage only. Two bytes are read out of the device in the format shown in Table 13.

Table 13. Voltage Only Readback Format

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Voltage MSBs	V11	V10	V9	V8	V7	V6	V5	V4
2	Voltage LSBs	V3	V2	V1	V0	0	0	0	0

Current Readback

The ADM1192 digitizes current only. Two bytes are read out of the device in the format shown in Table 14.

Table 14. Current Only Readback Format

Byte	Contents	B7	B6	B5	B4	B3	B2	B1	B0
1	Current MSBs	I11	I10	I9	I8	I7	I6	I5	I4
2	Current LSBs	I3	I2	I1	I0	0	0	0	0

The following series of events occurs when the master receives three bytes (voltage and current data) from the slave device:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives the first data byte.
5. The master asserts an acknowledge on SDA.
6. The master receives the second data byte.
7. The master asserts an acknowledge on SDA.
8. The master receives the third data byte.
9. The master asserts a no acknowledge on SDA.
10. The master asserts a stop condition on SDA, and the transaction ends.

For cases where the master is reading voltage only or current only, only two data bytes are read. Step 7 and Step 8 are not required.

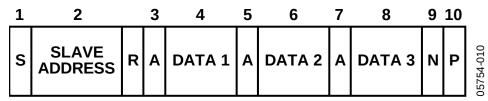


Figure 24. Three-Byte Read from ADM1192

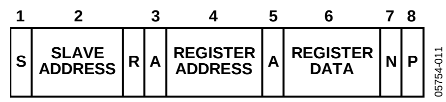


Figure 25. Two-Byte Read from ADM1192

Converting ADC Codes to Voltage and Current Readings

The following equations can be used to convert ADC codes representing voltage and current from the ADM1175 12-bit ADC into actual voltage and current values.

$$Voltage = (V_{FULLSCALE}/4096) \times Code$$

where:
$V_{FULLSCALE}$ = 6.65 (7:2 range) or 26.35 (14:1 range).
Code is the ADC voltage code read from the device (Bit V0 to Bit V11).

$$Current = ((I_{FULLSCALE}/4096) \times Code)/Sense\ Resistor$$

where:
$I_{FULLSCALE}$ = 105.84 mV.
Code is the ADC current code read from the device (Bit I0 to Bit I11).

Read Status Register

A single register of status data can also be read from the ADM1192.

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address, followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives the status byte.
5. The master asserts an acknowledge on SDA.

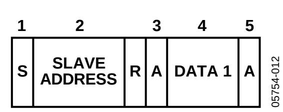


Figure 26. Status Read from ADM1192

Table 15 shows the ADM1192 status registers in detail. Note that Bit 1, Bit 3, and Bit 5 are cleared by writing to Bit 4 of the ALERT_EN register (CLEAR).

Table 15. Status Byte Operations

Bit	Name	Function
0	ADC_OC	An ADC-based overcurrent comparison has been detected on the last three conversions.
1	ADC_ALERT	An ADC-based overcurrent trip has occurred, which has caused the alert. Cleared by writing to Bit 4 of the ALERT_EN register.
2	OC	An overcurrent condition is present (that is, the output of the current sense amplifier is greater than the voltage on the SETV input).
3	OC_ALERT	An overcurrent condition has caused the ALERT block to latch a fault, and the ALERT output has asserted. Cleared by writing to Bit 4 of the ALERT_EN register.
4	OFF_STATUS	Set to 1 by writing to the SWOFF bit of the CONTROL register.
5	OFF_ALERT	An alert has been caused by the SWOFF bit. Cleared by writing to Bit 4 of the ALERT_EN register.

ALERT OUTPUT

The ALERT output is an open-drain pin with 30 V tolerance. There are two uses for this output.

Overcurrent Flag

The ALERT pin can be connected to the general-purpose logic input of a controller. Under normal operation, the ADM1192 drives this output low. When an overcurrent condition occurs, the output asserts high. An external pull-up resistor should be used.

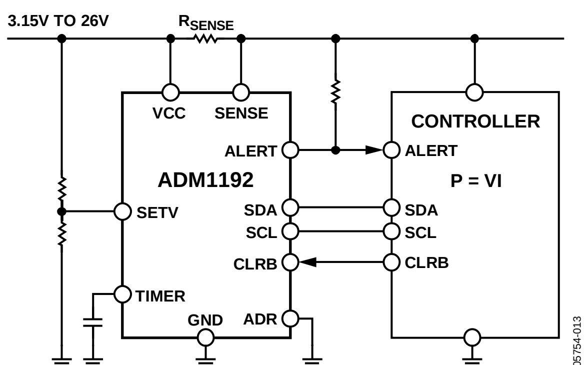


Figure 27. Using the ALERT Output as an Interrupt

Implementing a Basic Hot Swap Circuit

A basic P-channel FET hot swap circuit can be created. The ALERT output should be connected to the GATE pin of a P-channel FET connected in series with the power path. A pull-up from GATE to source ensures that the P-channel FET GATE is pulled up and the device held off as soon as power is applied. When the ADM1192 powers up, the GATE is pulled low by the ALERT output. A capacitor on the TIMER pin determines the slew rate of the GATE at turn-on. Note that if a current fault occurs at any point in operation, the ALERT output asserts high, turning off the P-channel FET.

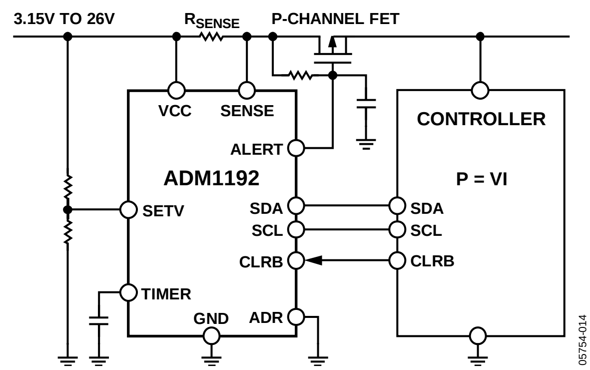


Figure 28. P-Channel FET Hot Swap Implementation

SETV PIN

The SETV pin allows the user to adjust the current level that trips the ALERT output. The output of the current sense amplifier is compared with the voltage driven onto the SETV pin. If the current sense amplifier output is higher than the SETV voltage, the output of the comparator asserts. By driving a different voltage onto the SETV pin, the ADM1192 detects an overcurrent condition at a different current level, with a gain of 18. See Figure 12 for an illustration of this relationship.

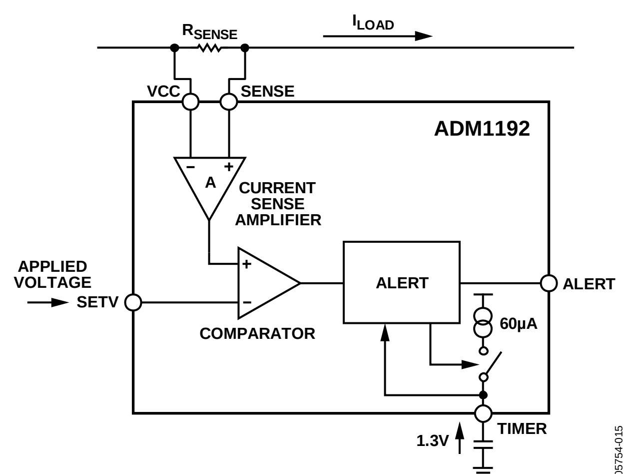


Figure 29. SETV Operation

When the output of the SETV comparator asserts, this tells the ALERT block to begin charging the external TIMER capacitor with a 60 μA charging current. When the voltage on the TIMER capacitor reaches 1 V, the charging cycle is complete. The ALERT output then asserts (goes high). Different values of TIMER capacitor generate different time delays between current faults occurring and the ALERT output asserting. When using the ALERT output to implement a hot swap circuit, the TIMER capacitor should be chosen to generate a large enough startup delay to allow the maximum inrush current to completely charge up the load without tripping an ALERT fault.

KELVIN SENSE RESISTOR CONNECTION

When using a low value sense resistor for high current measurement, the problem of parasitic series resistance can arise. The lead resistance can be a substantial fraction of the rated resistance, making the total resistance a function of lead length.

This problem can be avoided by using a Kelvin sense connection. This type of connection separates the current path through the resistor and the voltage drop across the resistor. Figure 30 shows the correct way to connect the sense resistor between the VCC pin and the SENSE pin of the ADM1192.

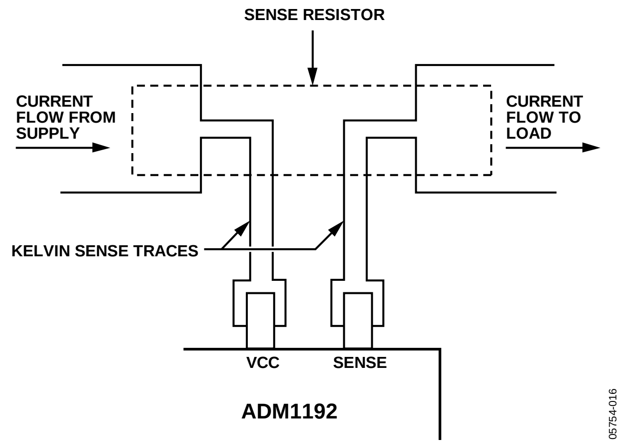
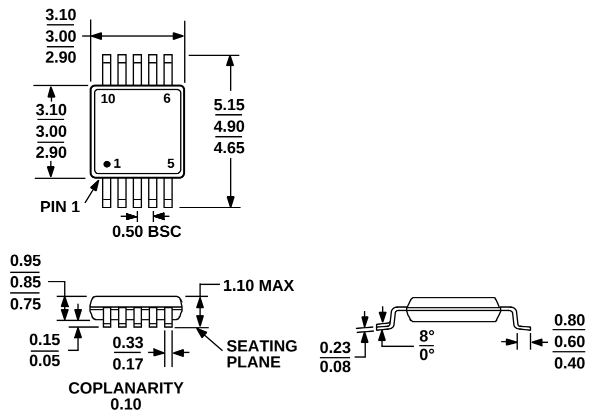


Figure 30. Kelvin Sense Connections

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 31. 10-Lead Mini Small Outline Package [MSOP]
(RM-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
ADM1192-1ARMZ-R7[1]	−40°C to +85°C	10-Lead MSOP	RM-10	M5M
EVAL-ADM1192EBZ[1]		Evaluation Board		

[1] Z = Pb-free part.

NOTES

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