3.2 Gbps, 3.3 V, Low Noise, Transimpedance Amplifier

ADN2880

FEATURES

Bandwidth: 2.5 GHz
Optical sensitivity: −24.2 dBm[1]
Differential transimpedance: 4400 V/A
Power dissipation: 70 mW
Differential output swing: 260 mV p-p
Input overload current: 4.3 mA p-p
On-chip RSSI function
Low frequency cutoff: 20 kHz
On-chip PD filter: R_F = 200 Ω, C_F = 20 pF
Die size: 0.7 mm × 1.2 mm

APPLICATIONS

3.2 Gbps or below optical receivers
SONET/GbE/FC optical receivers
SFF-8472-compliant receivers
PIN/APD-TIA receive optical subassemblies (ROSA)

GENERAL DESCRIPTION

The ADN2880 is a 3.3 V, high gain SiGe transimpedance amplifier (TIA). The TIA converts the small signal current of a photo detector into differential voltage output. The ADN2880 features a 315 nA typical input-referred noise, enabling an optical sensitivity of −24.2 dBm (0.85 A/W PIN). With a bandwidth of 2.5 GHz, the ADN2880 allows a data rate operation up to 3.2 Gbps. Typical power dissipation is approximately 70 mW.

To facilitate the assembly in small form factor packages, such as TO-46 headers, the ADN2880 provides an on-chip RC filter (200 Ω, 20 pF) and features a 20 kHz low frequency cutoff without using an external capacitor. An on-chip RSSI circuit, which generates a voltage proportional to the average photodiode current, is also available for power monitoring and assembly alignment.

The ADN2880 is available in die form. With a chip area of 1.2 mm × 0.7 mm, the TIA layout is specifically optimized for TO-Can-based packages.

[1] Based on 1550 nm PIN, responsivity = 0.85 A/W, ER = 9 dB, BER < 10^{-10}.

FUNCTIONAL BLOCK DIAGRAM

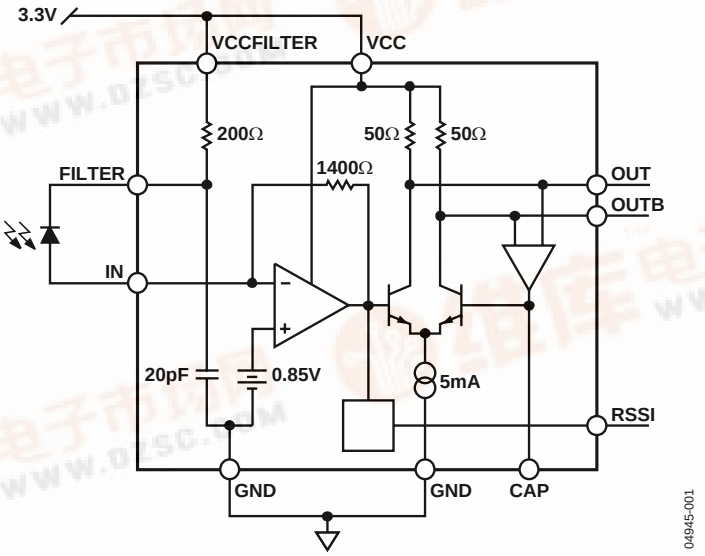

Figure 1.

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REVISION HISTORY

7/05—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

Minimum/maximum VCC = 3.3 V ± 0.3 V, $T_{AMBIENT}$ = −40°C to +95°C; typical VCC = 3.3 V, $T_{AMBIENT}$ = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth (BW)[1]	−3 dB	1.9	2.5		GHz
Total Input Referred RMS Noise (I_{RMS})	C_D = 0.8 pF, dc to 2.1 GHz		315	485	nA
Total Input Referred RMS Noise (I_{RMS})	C_D = 0.6 pF, dc to 2.1 GHz		300		nA
Small Signal Transimpedance (Z_T)[1]	100 MHz, differential	2700	4400	6200	V/A
	100 MHz, single-ended	1350	2200	3100	V/A
Low Frequency Cutoff	CAP = open, I_{IN} = 20 µA		20		kHz
	CAP = 1 nF, I_{IN} = 20 µA		1.0		kHz
Output Return Loss	DC to 3.5 GHz, differential		−26	−20	dB
Input Overload Current	ER = 10 dB, at 95°C[1]	2.1[1]	4.3		mA p-p
Maximum Differential Output Swing	$I_{IN, P-P}$ = 2.0 mA	170	260	375	mV p-p
Output Data Transition Time	$I_{IN, P-P}$ = 1.0 mA; 20% to 80% rise/fall time		60		ps
PSRR	I_{IN} = 0 mA, <10 MHz		39		dB
Group Delay Variation	1.0 GHz to 3.0 GHz		50		ps
Transimpedance Ripple	50 MHz to 1.0 GHz, single-ended		0.93		dB
Deterministic Jitter	10 µA < $I_{IN, P-P}$ ≤ 100 µA, K28.5 @ 3.2 Gbps		16		ps p-p
	100 µA < $I_{IN, P-P}$ ≤ 2.0 mA, K28.5 @ 3.2 Gbps		25		ps p-p
	10 µA < $I_{IN, P-P}$ ≤ 2.0 mA, PRBS $2^{31} - 1$ at OC48 (FEC)		38		ps p-p
Linear Output Range	Differential, <1 dB compression		210		mV p-p
Linear Input Current Range	Single-ended, <1 dB compression		53		µA p-p
DC PERFORMANCE					
Power Dissipation	$I_{IN, AVE}$ = 0 mA		70	110	mW
Input Voltage	Compliance voltage		0.85		V
Output Common-Mode Voltage	DC (50 Ω) terminated to VCC		VCC − 0.12		V
Output Impedance	Single-ended		50		Ω
PD FILTER Resistance	R_F		200		Ω
PD FILTER Capacitance	C_F		20		pF
RSSI Gain	$I_{IN, AVE}$ = 5 µA to 1 mA		0.85		V/mA
RSSI Offset	$I_{IN, AVE}$ = 10 µA		8.0		mV
RSSI Accuracy	5 µA < $I_{IN, P-P}$ ≤ 20 µA		±7		%
	20 µA < $I_{IN, P-P}$ ≤ 1 mA		±3		%

[1] An equivalent $I_{IN, P-P}$ = 13 µA current signal is applied to the TIA input. No input capacitor is applied.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (VCC to GND)	5 V
Maximum Voltage to All Input and Output Signal Pins	VCC + 0.4 V
Minimum Voltage to All Input and Output Signal Pins	GND – 0.4 V
Maximum Input Current	10 mA
Storage Temperature Range	–65°C to +125°C
Operating Ambient Temperature Range	–40°C to +95°C
Maximum Junction Temperature	125°C
Die Attach Temperature (<30 sec)	410°C

Stresses above those listed under Absolute Maximum Rating may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PAD LAYOUT AND FUNCTION DESCRIPTIONS

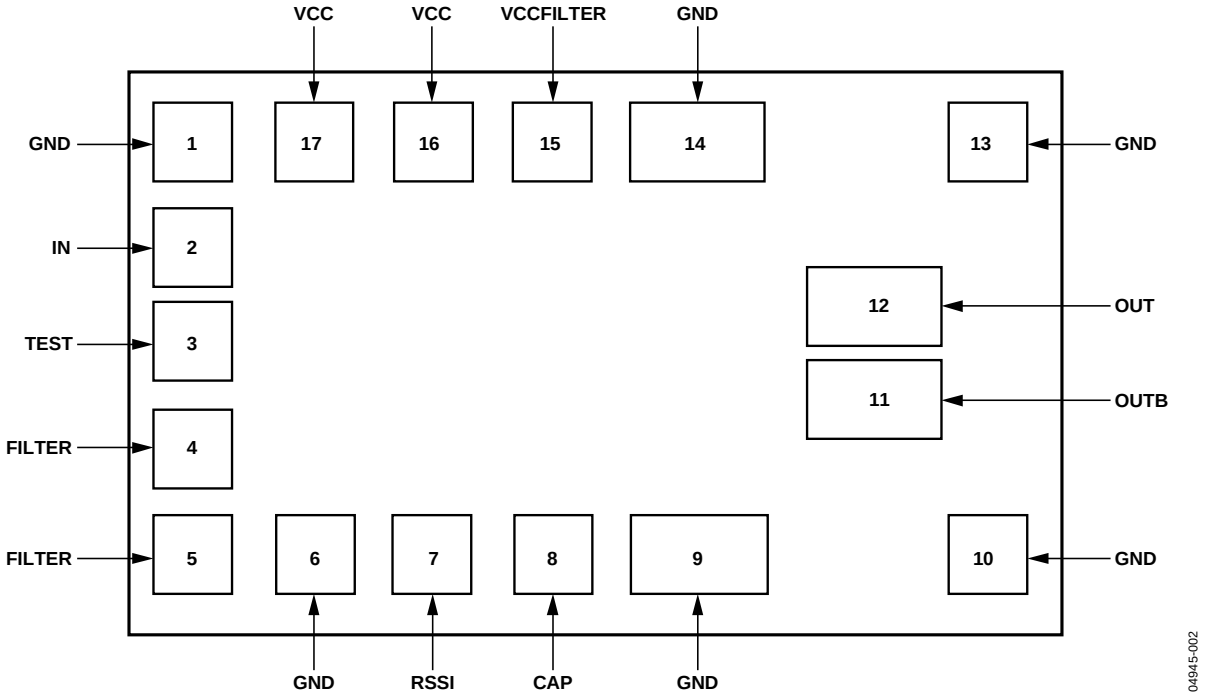

Figure 2. Pad Layout

Table 3. Pad Function Descriptions

Pad No.	Mnemonic	Pin Type[1]	Description
1	GND	P	Ground. (Input return.)
2	IN	AI	Current Input. Bond directly to a photodiode (PD) anode.
3	TEST	AI	Test Probe Pad. Do not connect.
4, 5	FILTER	AO	Filter Output. Pad 4 and Pad 5 are metal connected. Optional bond to a PD cathode.
6	GND	P	Ground.
7	RSSI	AO	Voltage Output. Provides average input current monitoring. If not used, connect to ground.
8	CAP	AI	Low Frequency Cutoff (LFC) Setpoint. For SONET applications, see Figure 10 and contact sales for assembly details.
9, 10, 13, 14	GND	P	Ground. (Output return.)
11	OUTB	AO	Negative Output, CML, On-Chip 50 Ω Termination (AC or DC Termination).
12	OUT	AO	Positive Output, CML, On-Chip 50 Ω Termination (AC or DC Termination).
15	VCCFILTER	P	On-Chip Filter Supply. Connect to VCC to Enable On-Chip RC Filter (200 Ω, 20 pF). Leave unconnected if not used.
16, 17	VCC	P	3.3 V Supply. Place a 200 pF, RF decoupling capacitor close to the power pad to reduce the power noise.

[1] P = power; AI = analog input; and AO = analog output.

TYPICAL PERFORMANCE CHARACTERISTICS

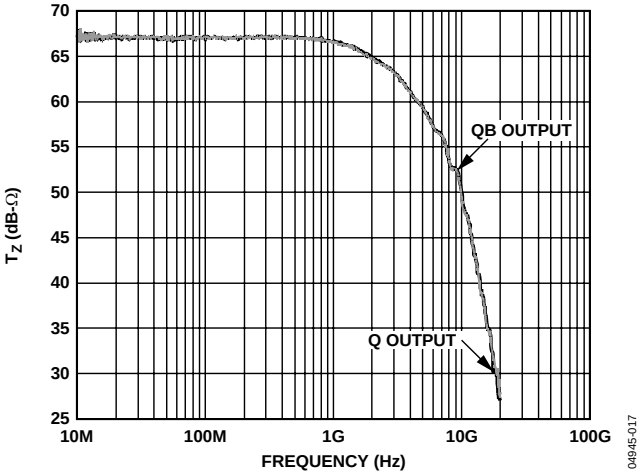

Figure 3. Single-Ended Transimpedance vs. Frequency

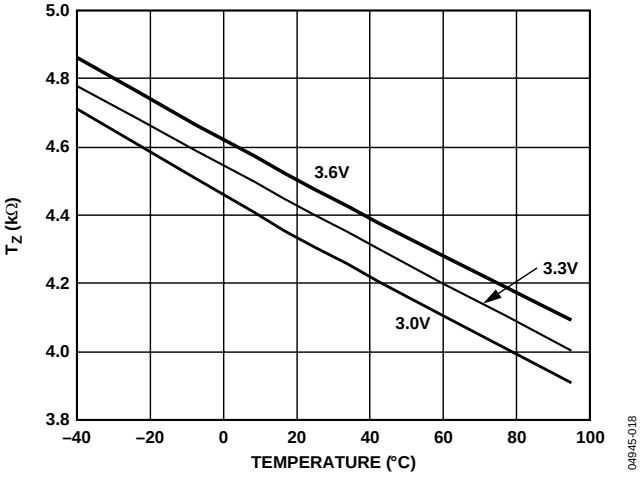

Figure 4. Differential Transimpedance vs. VCC and Temperature

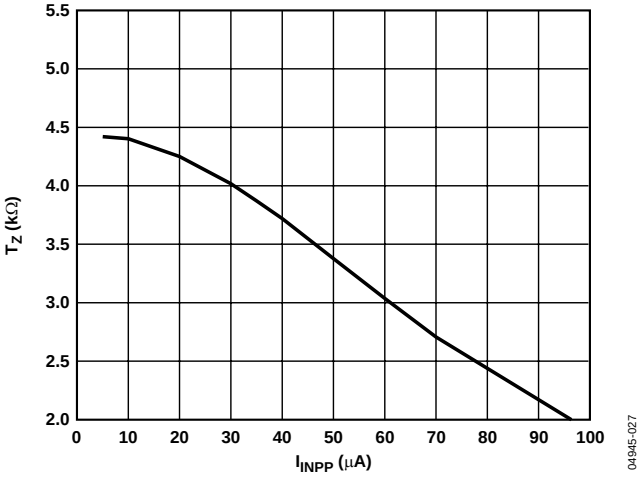

Figure 5. Differential Transimpedance vs. Input Current

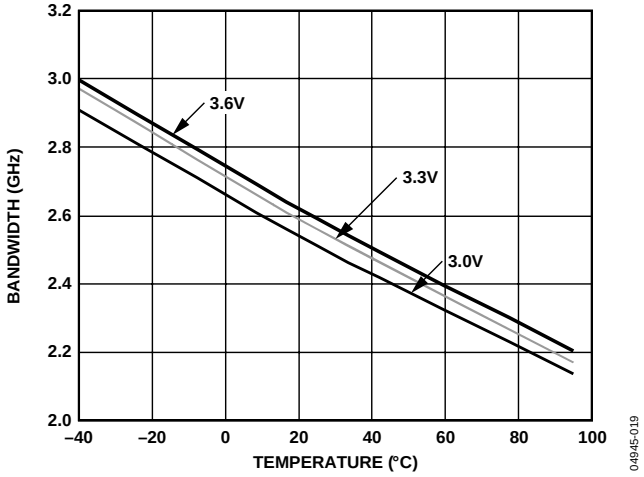

Figure 6. Bandwidth vs. VCC and Temperature

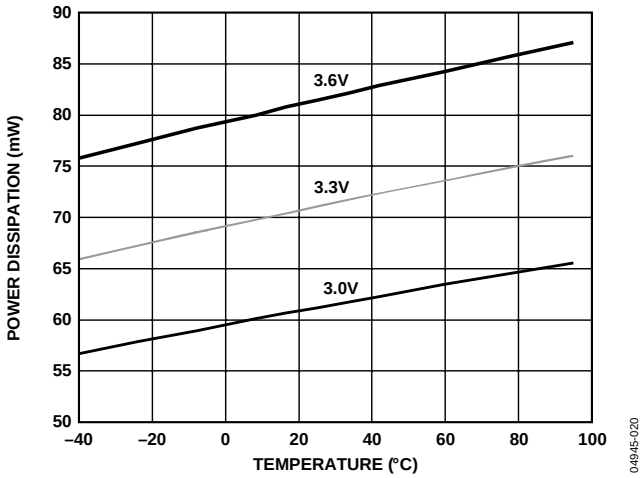

Figure 7. Power Dissipation vs. VCC and Temperature

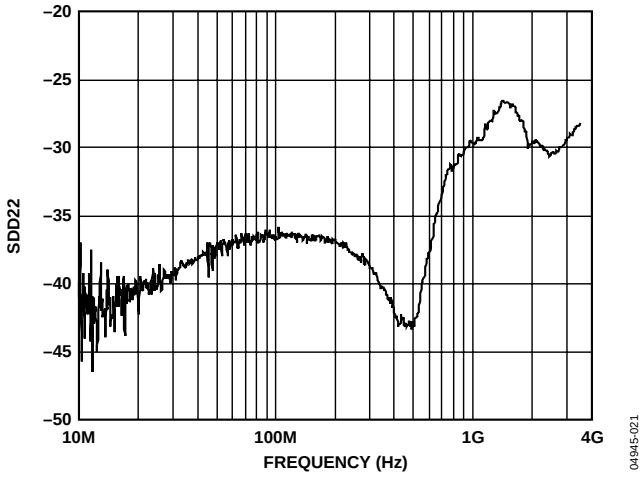

Figure 8. SDD22 vs. Frequency up to 3.5 GHz, CAP = Open

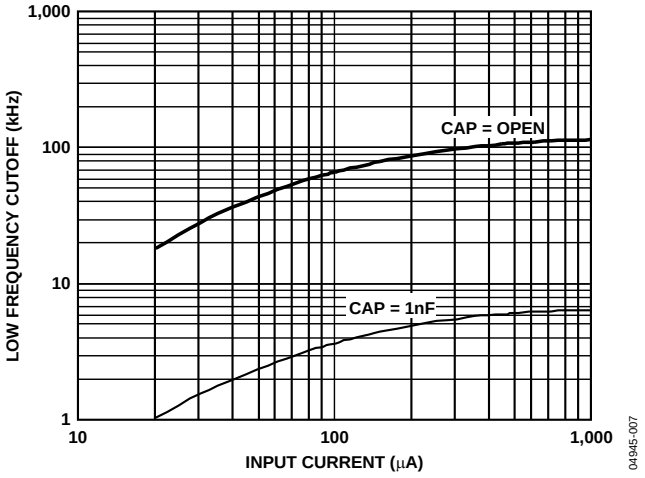

Figure 9. Low Frequency Cutoff vs. Input Current

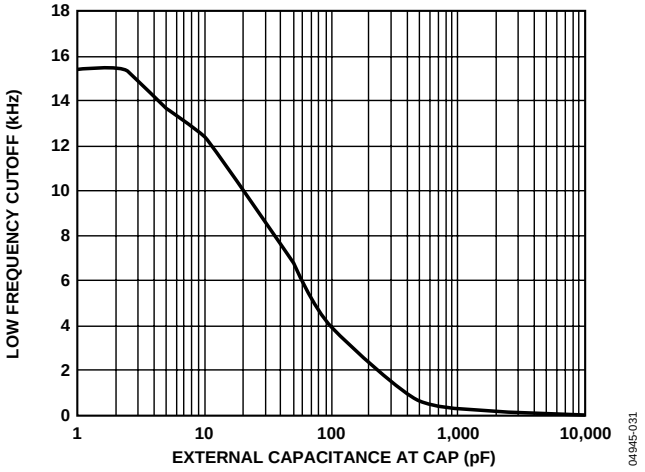

Figure 10. Low Frequency Cutoff vs. Capacitance at CAP

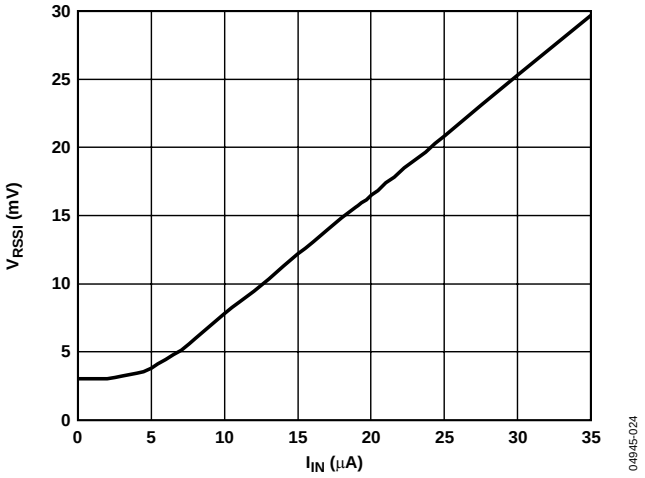

Figure 11. RSSI Voltage Output vs. Input Current (0 µA to 35 µA)

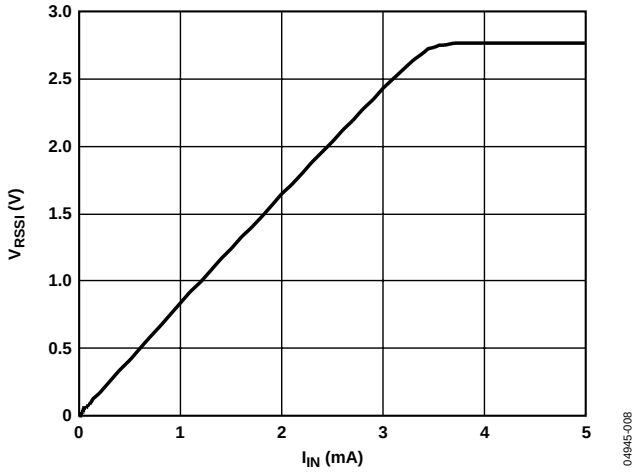

Figure 12. Full-Scale of RSSI Voltage Output vs. Input Current

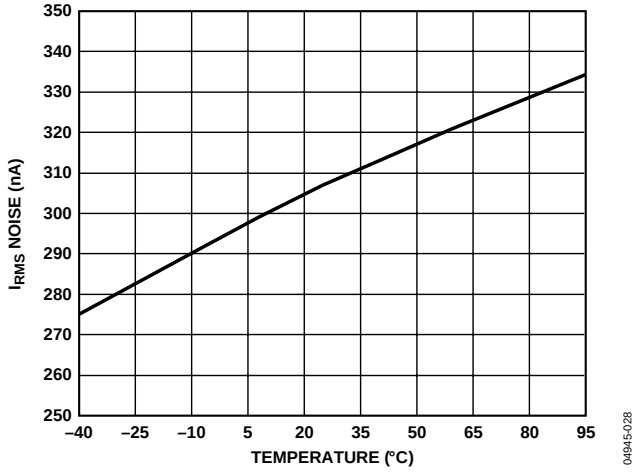

Figure 13. Input Noise vs. Temperature with 2 GHz Low-Pass Filter

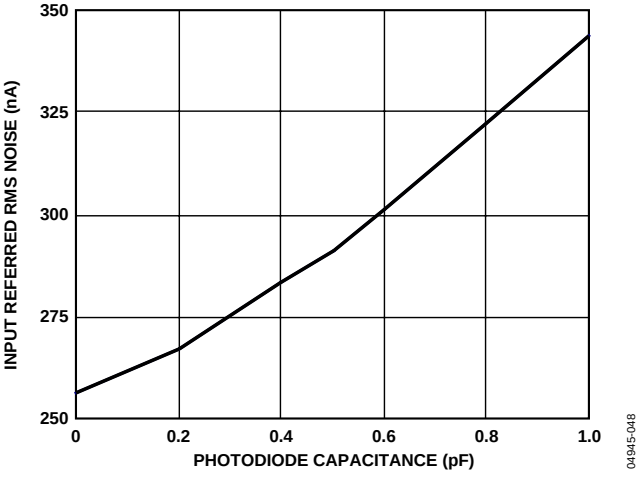

Figure 14. Input Referred Noise (DC to 2.0 GHz) vs. Photodiode Capacitance C_D (pF)

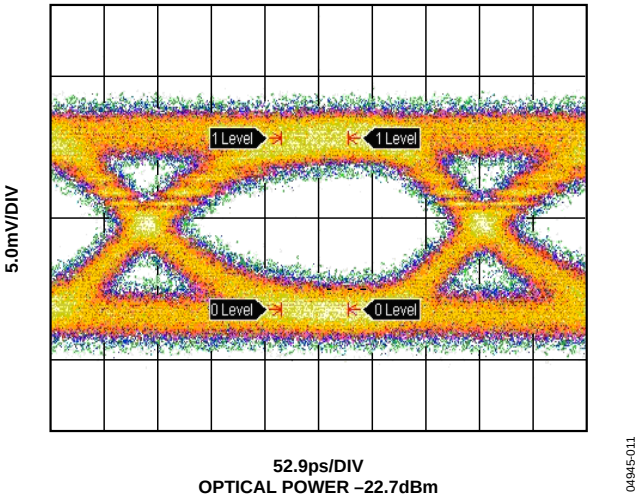

Figure 15. Output Eye at 3.2 Gbps with BER <10^{-10} (Based on a 1550 nm PIN, Responsivity = 0.91 A/W, ER = 9 dB, PRBS 2^{31})

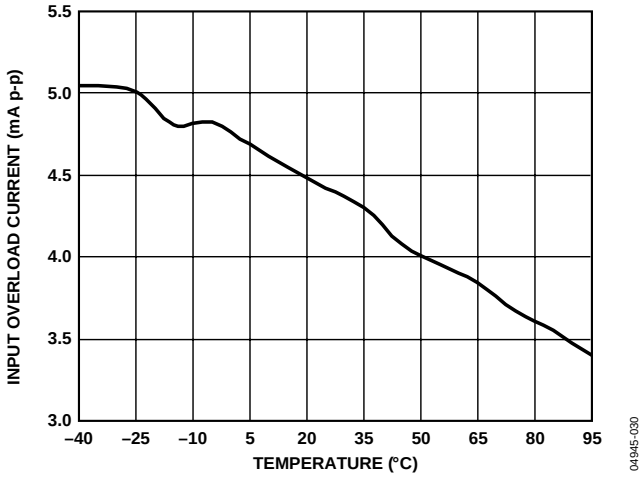

Figure 17. Input Overload Current vs. Temperature

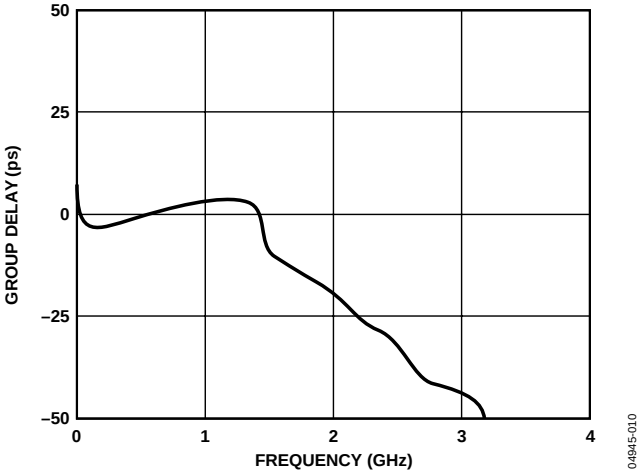

Figure 16. Group Delay vs. Frequency

ASSEMBLY RECOMMENDATIONS

Coplanar PIN Photodiode for SDH/SONET

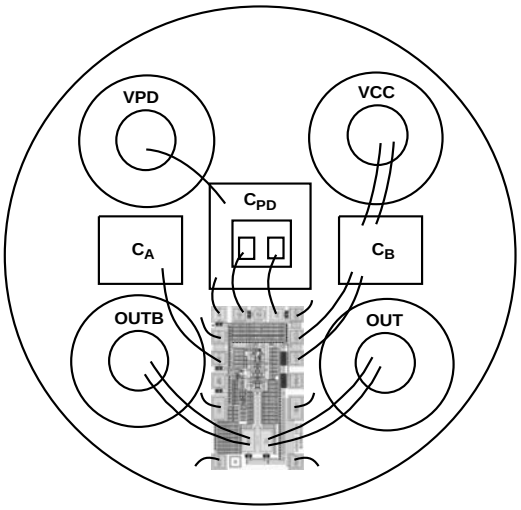

Figure 18. 5-Pin TO-46 with External Photodiode Supply V_{PD} Connected Through the FILTER Pin

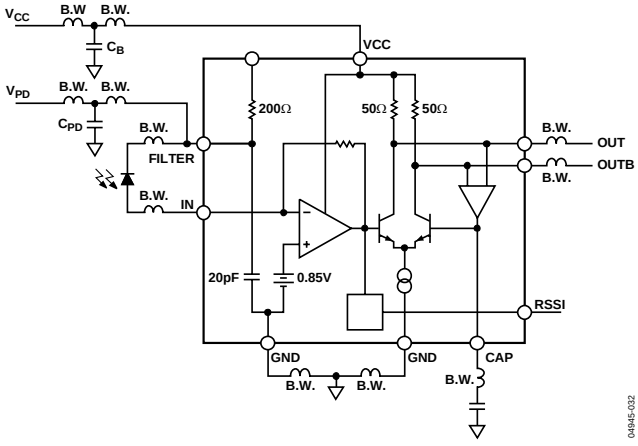

Figure 19. Equivalent Circuit of the Assembly Including Bond Wires

Dual Planar PIN/APD Photodiode for SDH/SONET

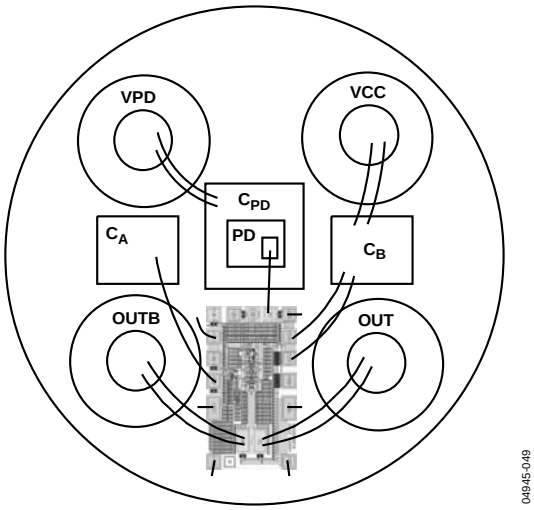

Figure 20. 5-Pin TO-46 with External Photodiode Supply V_{PD} to a Dual Planar PIN or APD

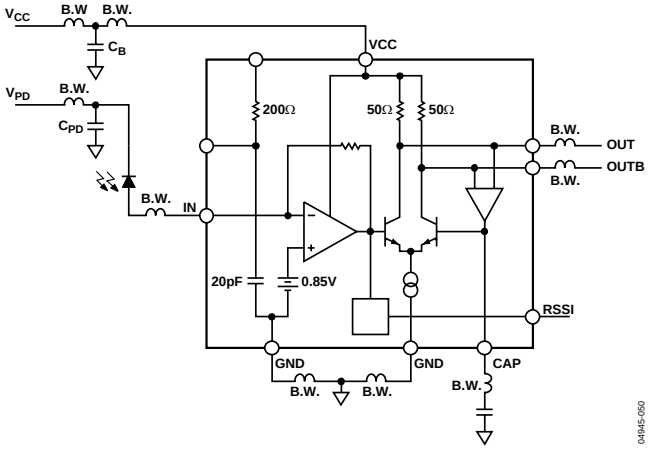

Figure 21. For Dual Planar PDs, No Connection to FILTER Pin

Table 4. Bill of Materials (BOM)

Component	Description
PD	1× vendor specific, 2.5 Gbps, photodiode
TIA	1× ADN2880 (0.7 mm × 1.2 mm), 3.2 Gbps, transimpedance amplifier
C_B	1× 200 pF, RF single-layer capacitor
C_{PD}	1× 560 pF, RF single-layer capacitor
C_A	1× 1000 pF, ceramic capacitor (optional for SDH)

Notes

One mil thickness, gold wire, ball bond recommended.

Minimize all GND bond-wire lengths.

Minimize IN, FILTER, OUT, and OUTB bond-wire lengths.

Maintain symmetry in length and orientation between OUT and OUTB bond wires.

Maintain symmetry in length and orientation between IN and FILTER bond wires.

Maintain symmetry between IN/FILTER and OUT/OUTB bond wires.

PIN Photodiode for a Non-SDH/SONET Application

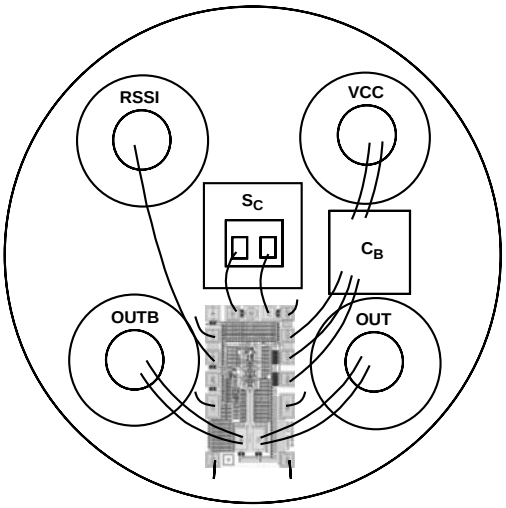

Figure 22. Coplanar PIN and RSSI Layout for a 5-Pin TO-46

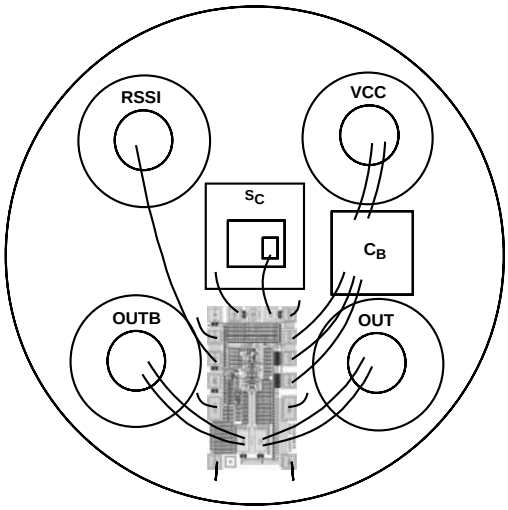

Figure 24. Dual Planar PIN and RSSI Layout for a 5-Pin TO-46

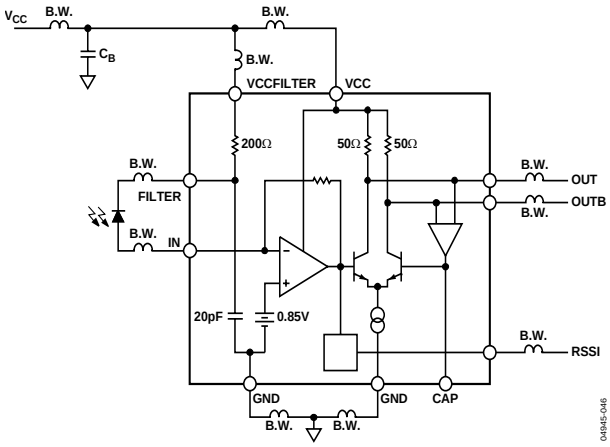

Figure 23. Equivalent Circuit with Bond Wires, as Shown in Figure 22

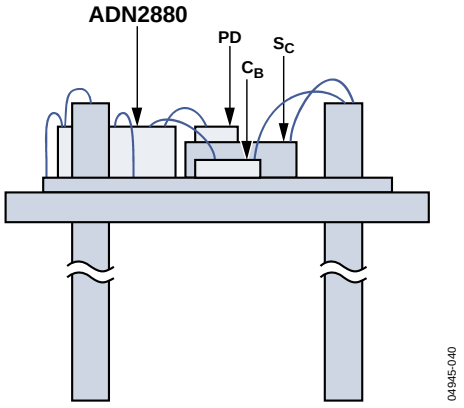

Figure 25. Side View of the Assembly, as Shown in Figure 22

Table 5. Bill of Materials (BOM)

Component	Description
PD	1× vendor specific, 2.5 Gbps, photodiode
TIA	1× ADN2880 (0.7 mm × 1.2 mm), 3.2 Gbps, transimpedance amplifier
C_B	1× 200 pF, RF single-layer capacitor
Sc	1× ceramic standoff or 1× optional capacitor

Notes

One mil thickness, gold wire, ball bond recommended.

Minimize all GND bond-wire lengths.

Minimize IN, FILTER, OUT, and OUTB bond-wire lengths.

Maintain symmetry in length and orientation between OUT and OUTB bond wires.

Maintain symmetry in length and orientation between IN and FILTER bond wires.

Maintain symmetry between IN/FILTER and OUT/OUTB bond wires.

PIN Photodiode for Non-SDH/SONET Applications

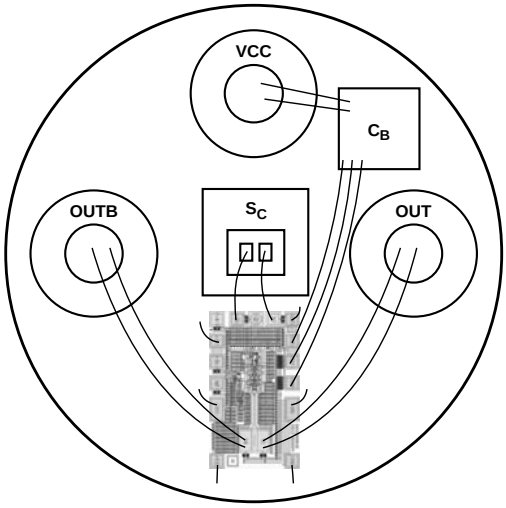

Figure 26. Coplanar PIN for a 4-Pin TO-46

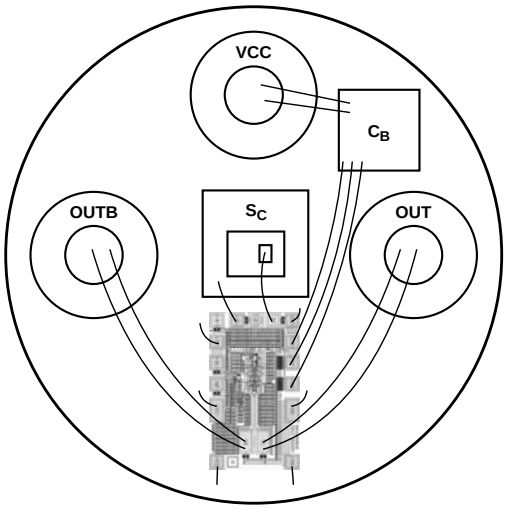

Figure 28. Dual Planar PIN for a 4-Pin TO-46

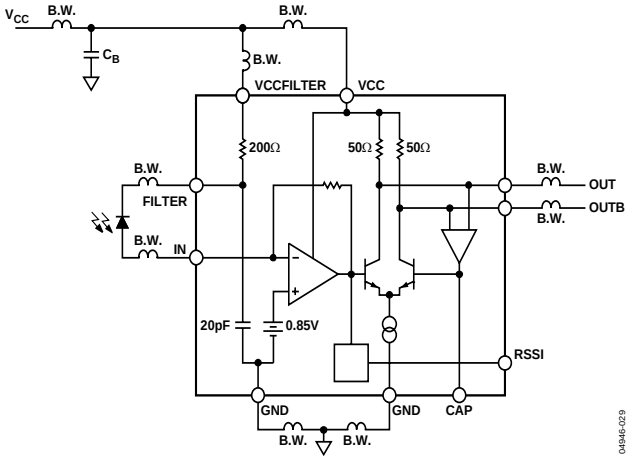

Figure 27. Equivalent Circuit with Bond Wires, as Shown in Figure 26

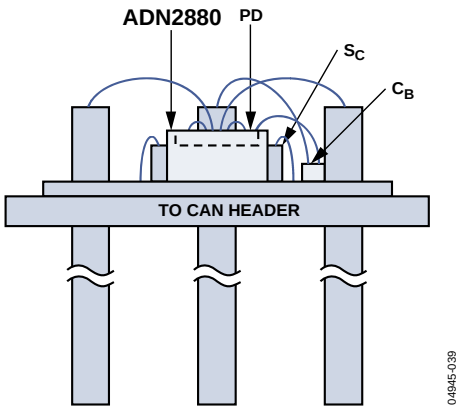

Figure 29. Side View of the Assembly, as Shown in Figure 26

Table 6. Bill of Materials (BOM)

Component	Description
PD	1× vendor specific, 2.5 Gbps, photodiode
TIA	1× ADN2880 (0.7 mm × 1.2 mm), 3.2 Gbps, transimpedance amplifier
C_B	1× 200 pF, RF single-layer capacitor
Sc	1× ceramic standoff or 1× optional 1000 pF capacitor

Notes

One mil thickness, gold wire, ball bond recommended.

Minimize all GND bond-wire lengths.

Minimize IN, FILTER, OUT, and OUTB bond-wire lengths.

Maintain symmetry in length and orientation between OUT and OUTB bond wires.

Maintain symmetry in length and orientation between IN and FILTER bond wires.

Maintain symmetry between IN/FILTER and OUT/OUTB bond wires.

OUTLINE DIMENSIONS

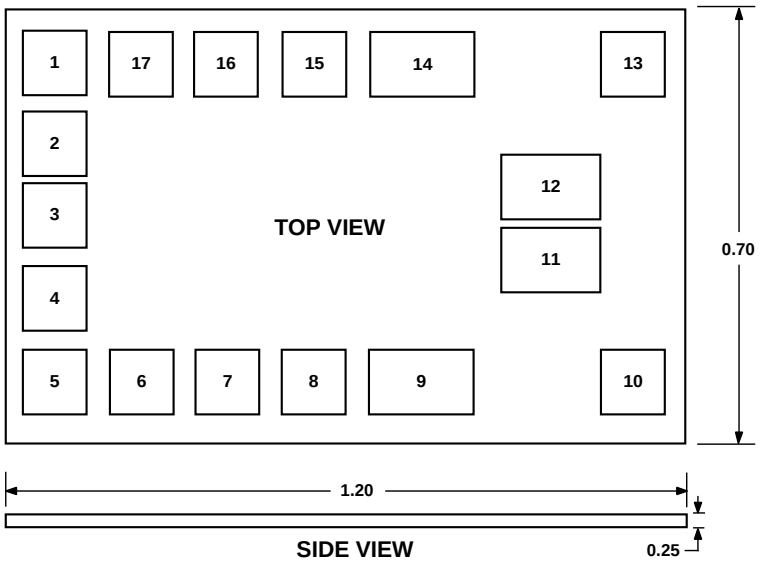

Figure 30. 17-Pad Bare Die Sales [CHIP]
Dimensions shown in millimeters

Table 7. Pad Coordinates

Pad No.	Mnemonic	X (µm)	Y (µm)
1	GND	−500	+260
2	IN	−500	+130
3	TEST	−500	+10
4	FILTER	−500	−120
5	FILTER	−500	−260
6	GND	−350	−260
7	RSSI	−200	−260
8	CAP	−50	−260
9	GND	+130	−260
10	GND	+500	−260
11	OUTB	+350	−60
12	OUT	+350	+60
13	GND	+500	+260
14	GND	+130	+260
15	VCCFILTER	−50	+260
16	VCC	−200	+260
17	VCC	−350	+260

DIE INFORMATION

Die Size

0.7 mm × 1.2 mm (edge-to-edge, including 1 mil scribe)

Die Thickness

10 mils = 0.25 mm

Passivation Openings

0.075 mm × 0.075 mm (Pad 1 to Pad 8, Pad 10, Pad 13, Pad 15 to Pad 17)

0.144 mm × 0.075 mm (Pad 9, Pad 11, Pad 12, Pad 14)

Passivation Composition

5000 Å Si_3N_4 (top)

5000 Å SiO_2 (bottom)

Pad Composition

Al/1%Cu

Substrate Contact

To ground

ORDERING GUIDE

Model	Temperature	Package Description
ADN2880ACHIPS	−40°C to +95°C	17-Pad Die Sales