3.75 Gbps Quad Bidirectional CX4 Equalizer

ADN8102

FEATURES

- Optimized for dc to 3.75 Gbps data
- Programmable input equalization
  - Up to 22 dB boost at 1.875 GHz
  - Compensates up to 30 meters of CX4 cable up to 3.75 Gbps
  - Compensates up to 40 inches of FR4 up to 3.75 Gbps
- Programmable output pre-emphasis/de-emphasis
  - Up to 12 dB boost at 1.875 GHz (3.75 Gbps)
  - Compensates up to 15 meters of CX4 cable up to 3.75 Gbps
  - Compensates up to 40 inches of FR4 up to 3.75 Gbps
- Flexible 1.8 V to 3.3 V core supply
- Per lane P/N pair inversion for routing ease
- Low power: 125 mW/channel up to 3.75 Gbps
- DC- or ac-coupled differential CML inputs
- Programmable CML output levels
- 50 Ω on-chip termination
- Loss-of-signal detection
- Temperature range operation: −40°C to +85°C
- Supports 8b10b, scrambled, or uncoded NRZ data
- I²C control interface
- 64-lead LFSCP (QFN) package

APPLICATIONS

- 10GBase-CX4
- HiGig™
- InfiniBand
- 1×, 2× Fibre Channel
- XAUI
- Gigabit Ethernet over backplane or cable
- CPRI™
- 50 Ω cables

FUNCTIONAL BLOCK DIAGRAM

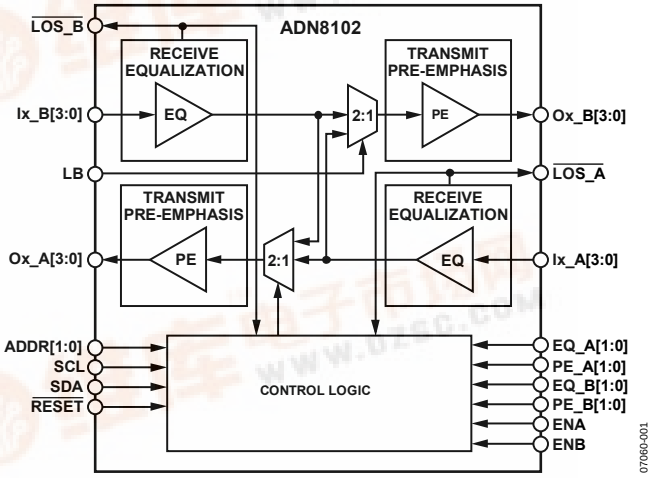

Figure 1.

GENERAL DESCRIPTION

The ADN8102 is a quad bidirectional CX4 cable/backplane equalizer with eight differential PECL-/CML-compatible inputs with programmable equalization and eight differential CML outputs with programmable output levels and pre-emphasis or de-emphasis. The operation of this device is optimized for NRZ data at rates up to 3.75 Gbps.

The receive inputs provide programmable equalization to compensate for up to 30 meters of CX4 cable (24 AWG) or 40 inches of FR4, and programmable pre-emphasis to compensate for up to 15 meters of CX4 cable (24 AWG) or 40 inches of FR4 at 3.75 Gbps. Each channel also provides programmable loss-of-signal detection and loopback capability for system testing and debugging.

The ADN8102 is controlled through toggle pins, an I²C® control interface that provides more flexible control, or a combination of both. Every channel implements an asynchronous path supporting dc to 3.75 Gbps NRZ data, fully independent of other channels. The ADN8102 has low latency and very low channel-to-channel skew.

The main application for the ADN8102 is to support switching in chassis-to-chassis applications over CX4 or InfiniBand® cables.

The ADN8102 is packaged in a 9 mm × 9 mm 64-lead LFCSP (QFN) package and operates from −40°C to +85°C.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

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REVISION HISTORY

8/08—Rev. 0 to Rev. A

Changes to Features Section 1
Changes to Loss of Signal/Signal Detect Section 18
Added Recommended LOS Settings Section 18
Deleted Figure 39; Renumbered Sequentially 18
Exposed Paddle Notation Added to Outline Dimensions 31

5/08—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 1.8 V, V_{EE} = 0 V, V_{TTI} = V_{TTO} = V_{CC}, R_L = 50 Ω, differential output swing = 800 mV p-p differential, 3.75 Gbps, PRBS $2^7 - 1$, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Maximum Data Rate/Channel (NRZ)		3.75			Gbps
Deterministic Jitter	Data rate < 3.75 Gbps; BER = 1×10^{-12}		33		ps p-p
Random Jitter	V_{CC} = 1.8 V		1.5		ps rms
Residual Deterministic Jitter					
With Input Equalization	Data rate < 3.25 Gbps; 0 inches to 40 inches FR4		0.20		UI
	Data rate < 3.25 Gbps; 0 meters to 30 meters CX4		0.19		UI
	Data rate < 3.75 Gbps; 0 inches to 40 inches FR4		0.24		UI
	Data rate < 3.75 Gbps; 0 meters to 30 meters CX4		0.21		UI
With Output Pre-Emphasis	Data rate < 3.25 Gbps; 0 inches to 40 inches FR4		0.13		UI
	Data rate < 3.25 Gbps; 0 meters to 15 meters CX4		0.37		UI
	Data rate < 3.75 Gbps; 0 inches to 40 inches FR4		0.14		UI
	Data rate < 3.75 Gbps; 0 meters to 15 meters CX4		0.41		UI
Output Rise/Fall Time	20% to 80%		75		ps
Propagation Delay			1		ns
Channel-to-Channel Skew			50		ps
OUTPUT PRE-EMPHASIS					
Equalization Method	1-tap programmable pre-emphasis				
Maximum Boost	800 mV p-p output swing		6		dB
	200 mV p-p output swing		12		dB
Pre-Emphasis Tap Range	Minimum		2		mA
	Maximum		12		mA
INPUT EQUALIZATION					
Minimum Boost	EQBY = 1		1.5		dB
Maximum Boost	Maximum boost occurs at 1.875 GHz		22		dB
Number of Equalization Settings			8		
Gain Step Size			2.5		dB
INPUT CHARACTERISTICS					
Input Voltage Swing	Differential, V_{ICM}[1] = V_{CC} − 0.6 V	300		2000	mV p-p
Input Voltage Range	Single-ended absolute voltage level, V_L minimum		V_{EE} + 0.4		V p-p
	Single-ended absolute voltage level, V_H maximum		V_{CC} + 0.5		V p-p
Input Resistance	Single-ended	45	50	55	Ω
Input Return Loss	Measured at 2.5 GHz		5		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	DC, differential, PE = 0, default, V_{CC} = 1.8 V	635	740	870	mV p-p
	DC, differential, PE = 0, default, V_{CC} = 3.3 V		800		mV p-p
	DC, differential, PE = 0, minimum output level,[2] V_{CC} = 1.8 V		100		mV p-p
	DC, differential, PE = 0, minimum output level,[2] V_{CC} = 3.3 V		100		mV p-p
	DC, differential, PE = 0, maximum output level,[2] V_{CC} = 1.8 V		1300		mV p-p
	DC, differential, PE = 0, maximum output level,[2] V_{CC} = 3.3 V		1800		mV p-p

Parameter	Conditions	Min	Typ	Max	Unit
Output Voltage Range	Single-ended absolute voltage level, TxHeadroom = 0; V_L minimum		V_{CC} − 1.1		V
	Single-ended absolute voltage level, TxHeadroom = 0; V_H maximum		V_{CC} + 0.6		V
	Single-ended absolute voltage level, TxHeadroom = 1; V_L minimum		V_{CC} − 1.2		V
	Single-ended absolute voltage level, TxHeadroom = 1; V_H maximum		V_{CC} + 0.6		V
Output Current	Minimum output current per channel		2		mA
	Maximum output current per channel, V_{CC} = 1.8 V		21		mA
Output Resistance	Single-ended	43	50	57	Ω
Output Return Loss	Measured at 2.5 GHz		5		dB
LOS CHARACTERISTICS					
Assert Level	IN_A/IN_B THRESH = 0x0C		20		mV diff
Deassert Level	IN_A/IN_B HYST = 0x0D		225		mV diff
POWER SUPPLY					
Operating Range					
V_{CC}	V_{EE} = 0 V	1.7	1.8	3.6	V
DV_{CC}	V_{EE} = 0 V, $DV_{CC} \le (V_{CC} + 1.3\ V)$	3.0	3.3	3.6	V
V_{TTI}	$(V_{EE} + 0.4\ V + 0.5 \times V_{ID}) < V_{TTI} < (V_{CC} + 0.5\ V)$	V_{EE} + 0.4	1.8	3.6	V
V_{TTO}	$(V_{CC} - 1.1\ V + 0.5 \times V_{OD}) < V_{TTO} < (V_{CC} + 0.5\ V)$	V_{CC} − 1.1	1.8	3.6	V
Supply Current					
V_{TTO}	All outputs enabled		63	69	mA
V_{CC}	All outputs enabled		460	565	mA
V_{EE}	All outputs enabled		586		mA
LOGIC CHARACTERISTICS					
Input High, V_{IH}	DV_{CC} = 3.3 V	2.5			V
Input Low, V_{IL}				1.0	V
Output High, V_{OH}		2.5			V
Output Low, V_{OL}				1.0	V
THERMAL CHARACTERISTICS					
Operating Temperature Range		−40		+85	°C
θ_{JA}			22		°C/W

[1] V_{ICM} is the input common-mode voltage.
[2] Programmable via I^2C.

TIMING SPECIFICATIONS

Table 2. I²C Timing Parameters

Parameter	Min	Max	Unit	Description
f_{SCL}	0	400	kHz	SCL clock frequency
$t_{HD:STA}$	0.6	N/A	µs	Hold time for a start condition
$t_{SU:STA}$	0.6	N/A	µs	Setup time for a repeated start condition
t_{LOW}	1.3	N/A	µs	Low period of the SCL clock
t_{HIGH}	0.6	N/A	µs	High period of the SCL clock
$t_{HD:DAT}$	0	N/A	µs	Data hold time
$t_{SU:DAT}$	10	N/A	ns	Data setup time
t_R	1	300	ns	Rise time for both SDA and SCL
t_F	1	300	ns	Fall time for both SDA and SCL
$t_{SU:STO}$	0.6	N/A	µs	Setup time for a stop condition
t_{BUF}	1	N/A	ns	Bus free time between a stop and a start condition
C_{IO}	5	7	pF	Capacitance for each I/O pin

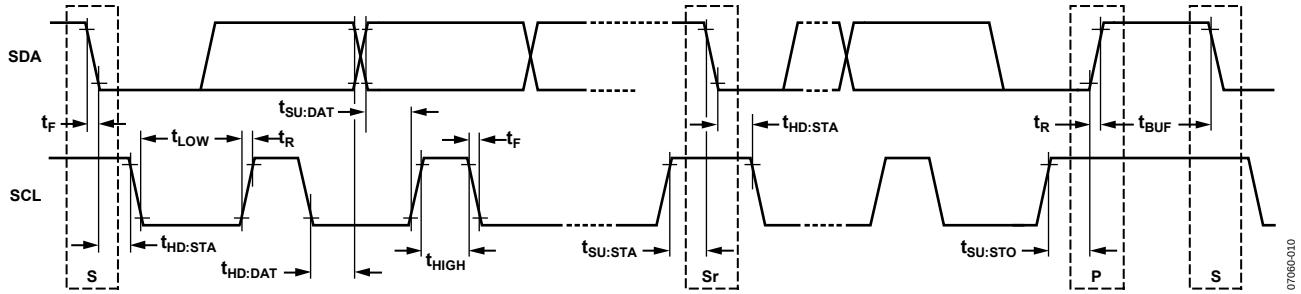

Figure 2. I²C Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V_{CC} to V_{EE}	3.7 V
V_{TTI}	V_{CC} + 0.6 V
V_{TTO}	V_{CC} + 0.6 V
Internal Power Dissipation	4.26 W
Differential Input Voltage	2.0 V
Logic Input Voltage	V_{EE} − 0.3 V < V_{IN} < V_{CC} + 0.6 V
Storage Temperature Range	−65°C to +125°C
Lead Temperature	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

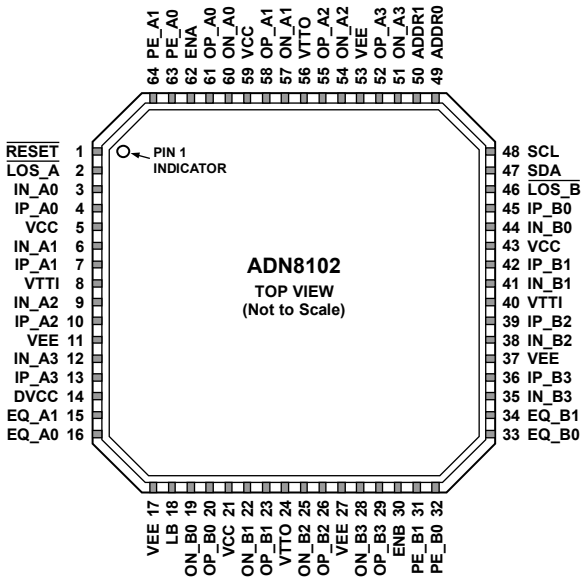

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1	$\overline{\text{RESET}}$	Control	Reset Input, Active Low
2	$\overline{\text{LOS\_A}}$	Digital I/O	Port A Loss of Signal Status, Active Low
3	IN_A0	I/O	High Speed Input Complement
4	IP_A0	I/O	High Speed Input
5	VCC	Power	Positive Supply
6	IN_A1	I/O	High Speed Input Complement
7	IP_A1	I/O	High Speed Input
8	VTTI	Power	Input Termination Supply
9	IN_A2	I/O	High Speed Input Complement
10	IP_A2	I/O	High Speed Input
11	VEE	Power	Negative Supply
12	IN_A3	I/O	High Speed Input Complement
13	IP_A3	I/O	High Speed Input
14	DVCC	Power	Digital Power Supply
15	EQ_A1	Control	Port A Input Equalization MSB
16	EQ_A0	Control	Port A Input Equalization LSB
17	VEE	Power	Negative Supply
18	LB	Control	Loopback Control
19	ON_B0	I/O	High Speed Output Complement
20	OP_B0	I/O	High Speed Output
21	VCC	Power	Positive Supply
22	ON_B1	I/O	High Speed Output Complement
23	OP_B1	I/O	High Speed Output
24	VTTO	Power	Output Termination Supply
25	ON_B2	I/O	High Speed Output Complement
26	OP_B2	I/O	High Speed Output
27	VEE	Power	Negative Supply

Pin No.	Mnemonic	Type	Description
28	ON_B3	I/O	High Speed Output Complement
29	OP_B3	I/O	High Speed Output
30	ENB	Control	Port B Enable
31	PE_B1	Control	Port B Output Pre-Emphasis MSB
32	PE_B0	Control	Port B Output Pre-Emphasis LSB
33	EQ_B0	Control	Port B Input Equalization LSB
34	EQ_B1	Control	Port B Input Equalization MSB
35	IN_B3	I/O	High Speed Input Complement
36	IP_B3	I/O	High Speed Input
37	VEE	Power	Negative Supply
38	IN_B2	I/O	High Speed Input Complement
39	IP_B2	I/O	High Speed Input
40	VTTI	Power	Input Termination Supply
41	IN_B1	I/O	High Speed Input Complement
42	IP_B1	I/O	High Speed Input
43	VCC	Power	Positive Supply
44	IN_B0	I/O	High Speed Input Complement
45	IP_B0	I/O	High Speed Input
46	$\overline{\text{LOS\_B}}$	Digital I/O	Port B Loss of Signal Status, Active Low
47	SDA	Control	I^2C Control Interface Data Input/Output
48	SCL	Control	I^2C Control Interface Clock Input
49	ADDR0	Control	I^2C Control Interface Address LSB
50	ADDR1	Control	I^2C Control Interface Address MSB
51	ON_A3	I/O	High Speed Output Complement
52	OP_A3	I/O	High Speed Output
53	VEE	Power	Negative Supply
54	ON_A2	I/O	High Speed Output Complement
55	OP_A2	I/O	High Speed Output
56	VTTO	Power	Output Termination Supply
57	ON_A1	I/O	High Speed Output Complement
58	OP_A1	I/O	High Speed Output
59	VCC	Power	Positive Supply
60	ON_A0	I/O	High Speed Output Complement
61	OP_A0	I/O	High Speed Output
62	ENA	Control	Port A Enable
63	PE_A0	Control	Port A Output Pre-Emphasis LSB
64	PE_A1	Control	Port A Output Pre-Emphasis MSB
EP	EPAD	Power	EPAD Must Be Connected to VEE

TYPICAL PERFORMANCE CHARACTERISTICS

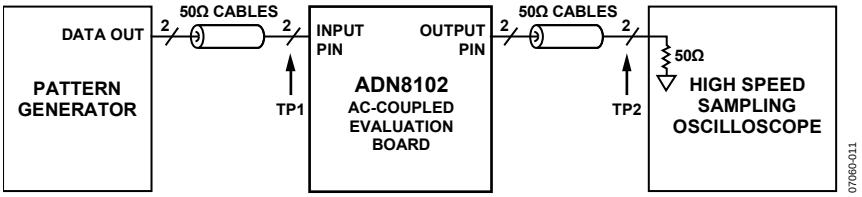

Figure 4. Standard Test Circuit (No Channel)

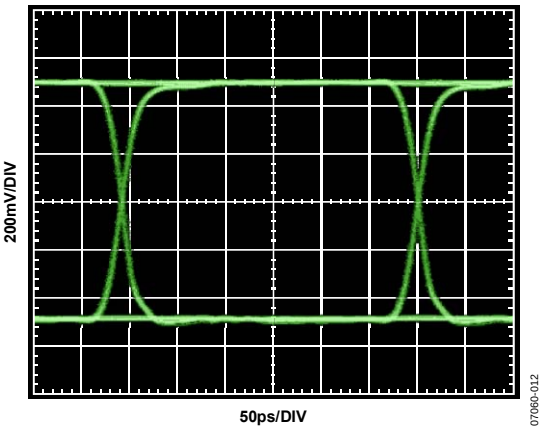

Figure 5. 3.25 Gbps Input Eye (TP1 from Figure 4)

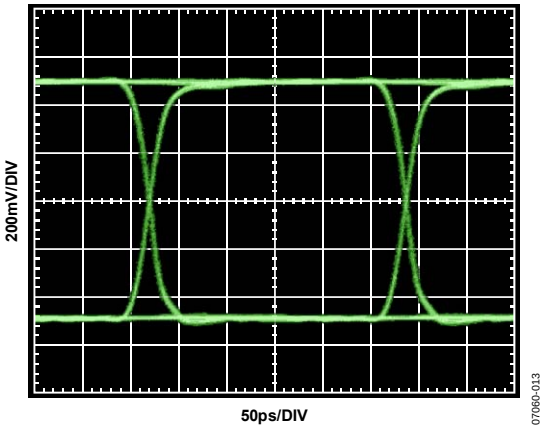

Figure 6. 3.75 Gbps Input Eye (TP1 from Figure 4)

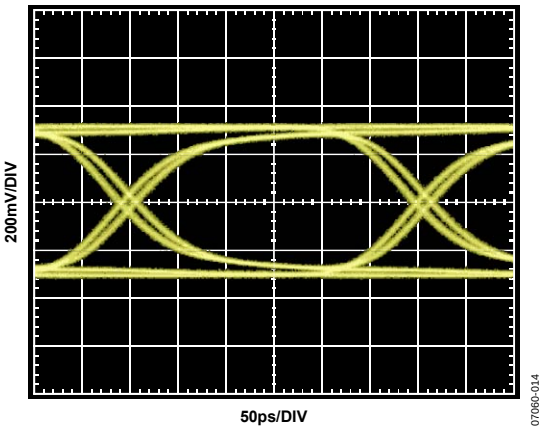

Figure 7. 3.25 Gbps Output Eye, No Channel (TP2 from Figure 4)

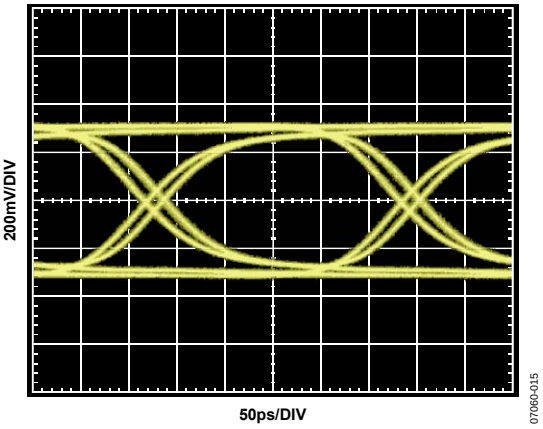

Figure 8. 3.75 Gbps Output Eye, No Channel (TP2 from Figure 4)

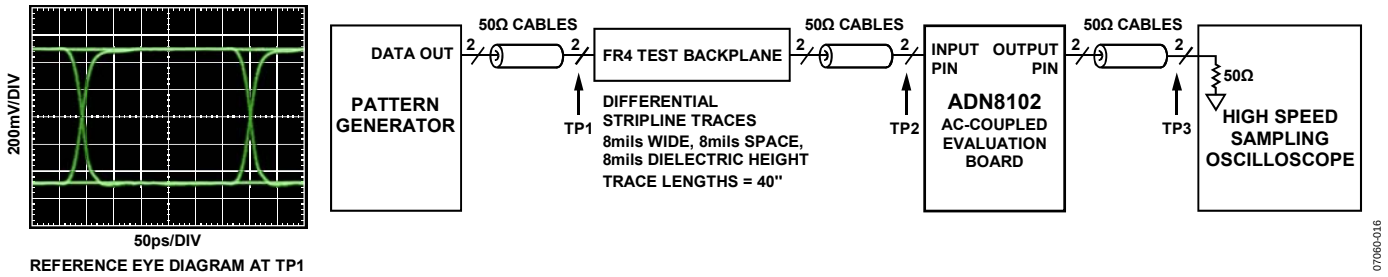

Figure 9. Input Equalization Test Circuit, FR4

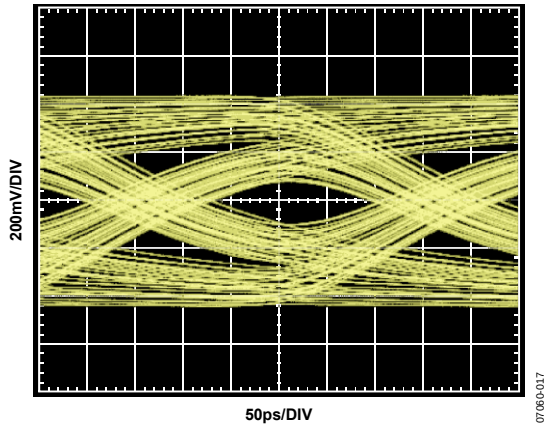

Figure 10. 3.25 Gbps Input Eye, 40 Inch FR4 Input Channel (TP2 from Figure 9)

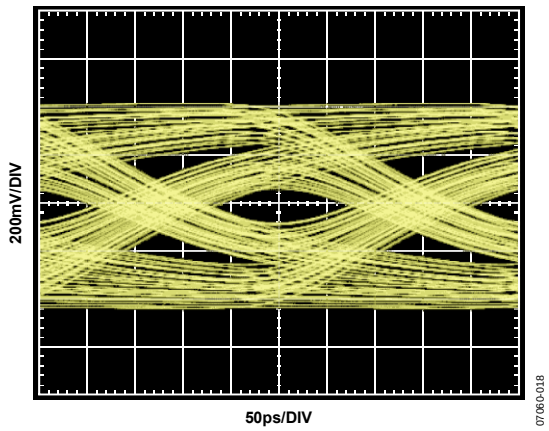

Figure 11. 3.75 Gbps Input Eye, 40 Inch FR4 Input Channel (TP2 from Figure 9)

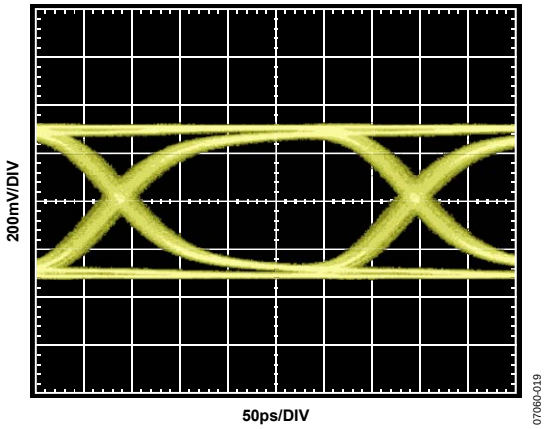

Figure 12. 3.25 Gbps Output Eye, 40 Inch FR4 Input Channel, Best EQ Setting (TP3 from Figure 9)

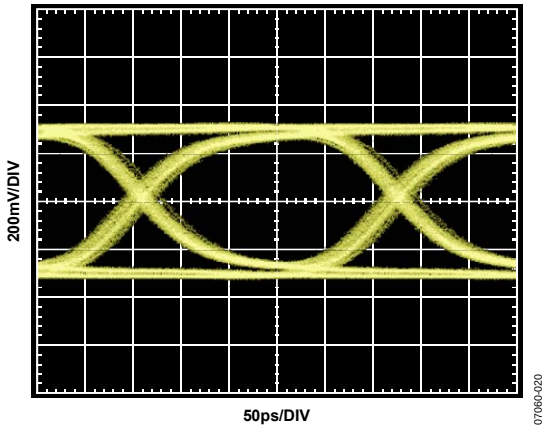

Figure 13. 3.75 Gbps Output Eye, 40 Inch FR4 Input Channel, Best EQ Setting (TP3 from Figure 9)

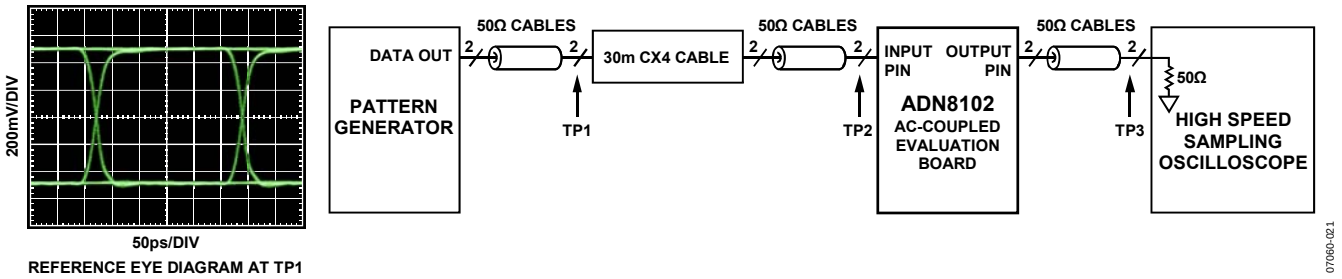

Figure 14. Input Equalization Test Circuit, CX4

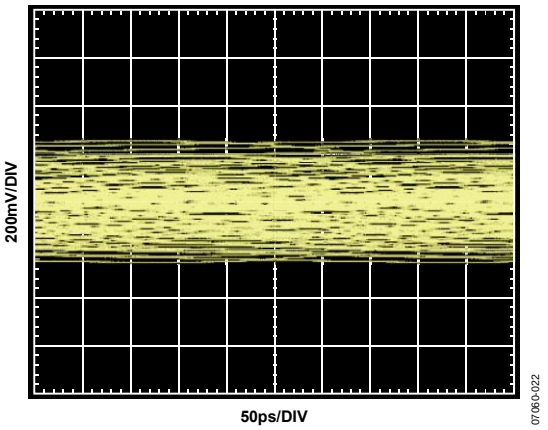

Figure 15. 3.25 Gbps Input Eye, 30 Meters CX4 Cable (TP2 from Figure 14)

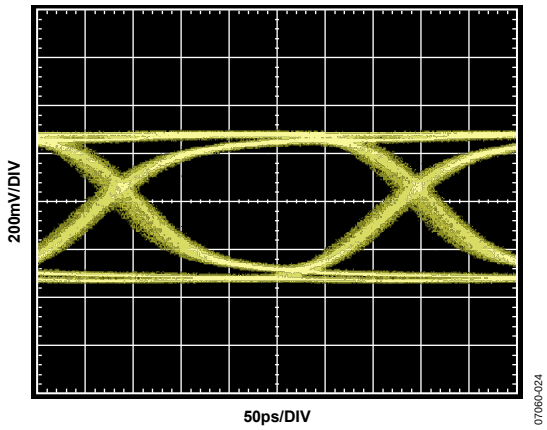

Figure 17. 3.25 Gbps Output Eye, 30 Meters CX4 Cable, Best EQ Setting (TP3 from Figure 14)

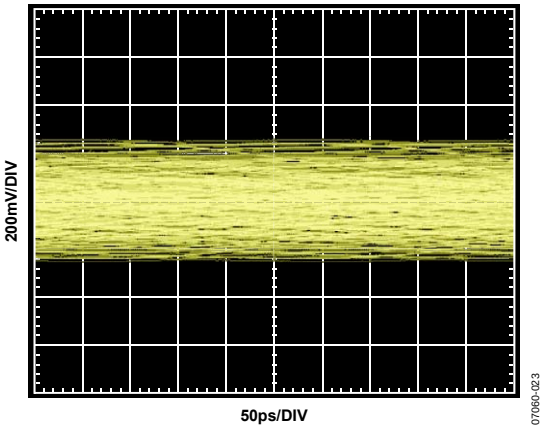

Figure 16. 3.75 Gbps Input Eye, 30 Meters CX4 Cable (TP2 from Figure 14)

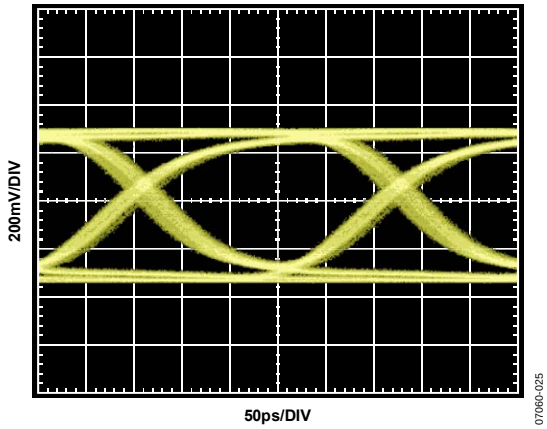

Figure 18. 3.75 Gbps Output Eye, 30 Meters CX4 Cable, Best EQ Setting (TP3 from Figure 14)

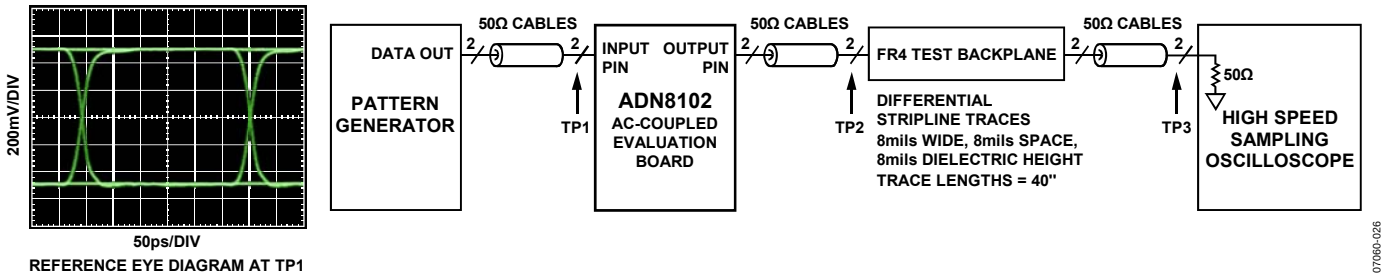

Figure 19. Output Pre-Emphasis Test Circuit, FR4

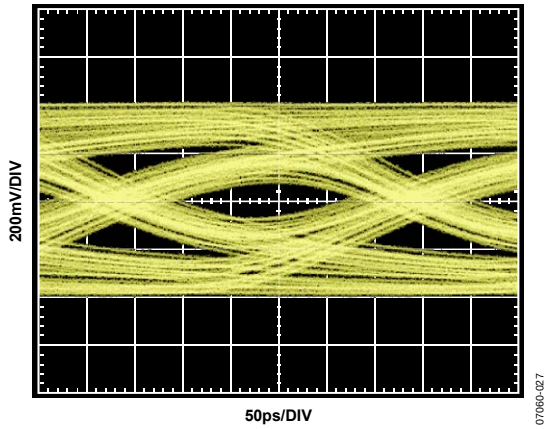

Figure 20. 3.25 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = 0 (TP3 from Figure 19)

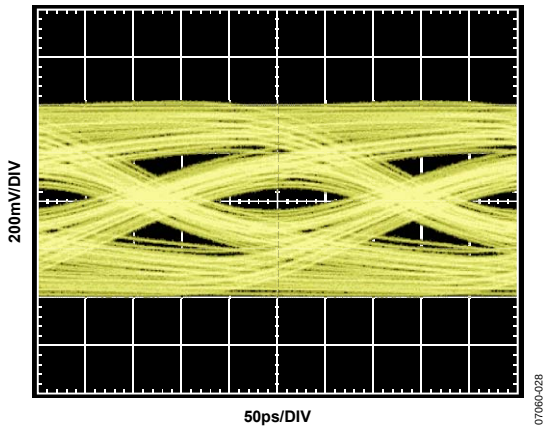

Figure 21. 3.75 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = 0 (TP3 from Figure 19)

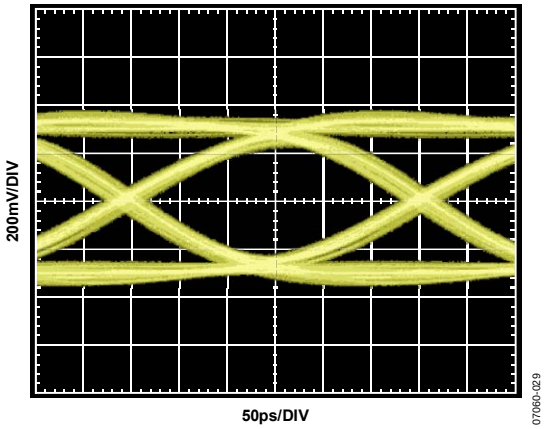

Figure 22. 3.25 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = Best Setting (TP3 from Figure 19)

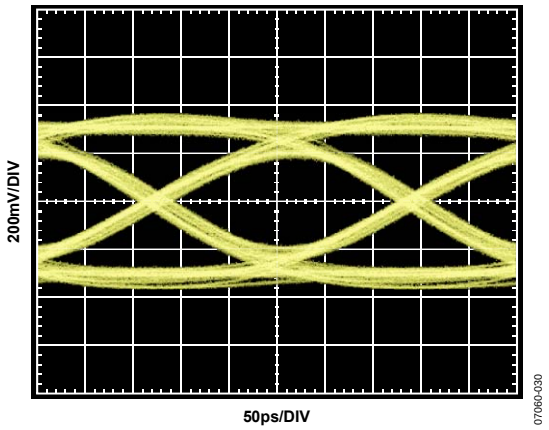

Figure 23. 3.75 Gbps Output Eye, 40 Inch FR4 Output Channel, PE = Best Setting (TP3 from Figure 19)

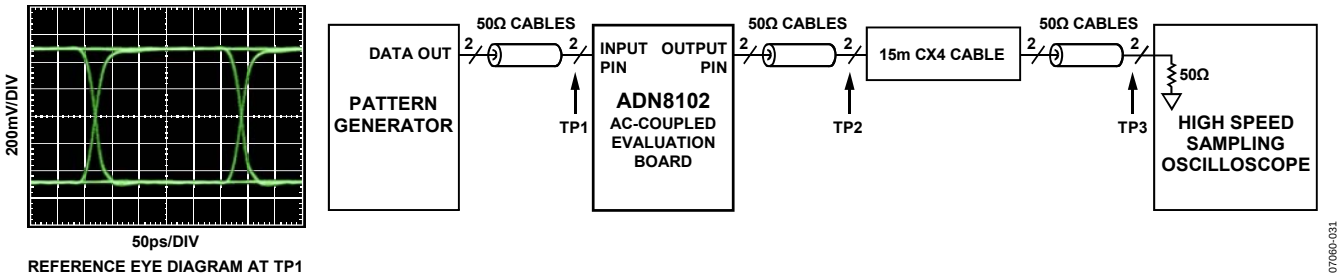

Figure 24. Output Pre-Emphasis Test Circuit, CX4

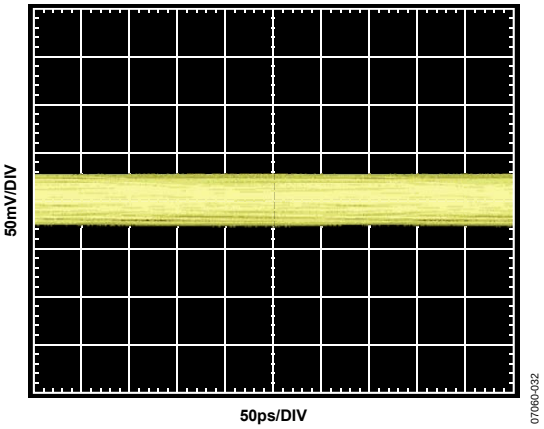

Figure 25. 3.25 Gbps Output Eye, 15 Meters CX4 Cable, PE = 0 (TP3 from Figure 24)

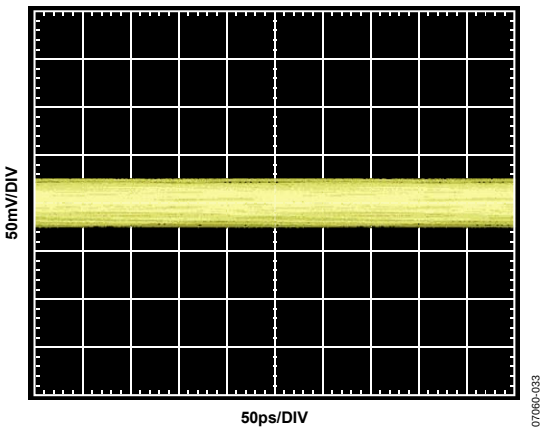

Figure 26. 3.75 Gbps Output Eye, 15 Meters CX4 Cable, PE = 0 (TP3 from Figure 24)

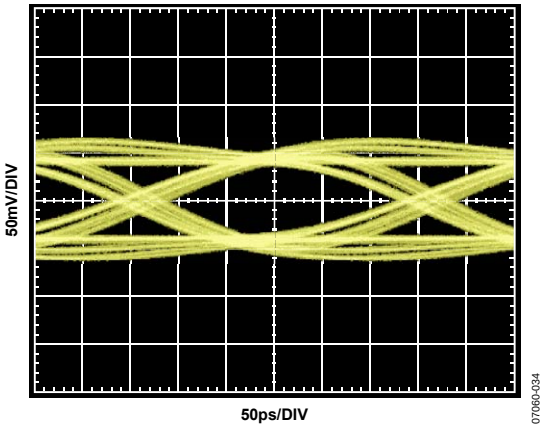

Figure 27. 3.25 Gbps Output Eye, 15 Meters CX4 Cable, PE = Best Setting (TP3 from Figure 24)

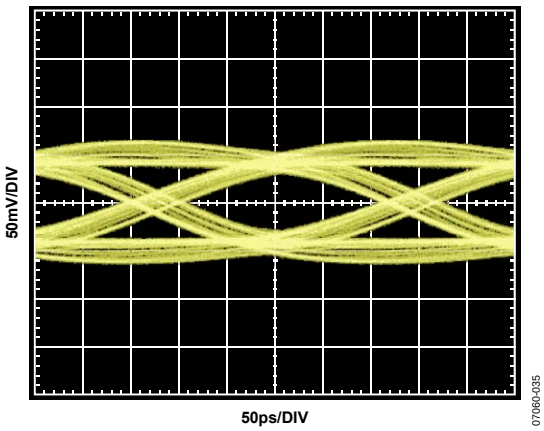

Figure 28. 3.75 Gbps Output Eye, 15 Meters CX4 Cable, PE = Best Setting (TP3 from Figure 24)

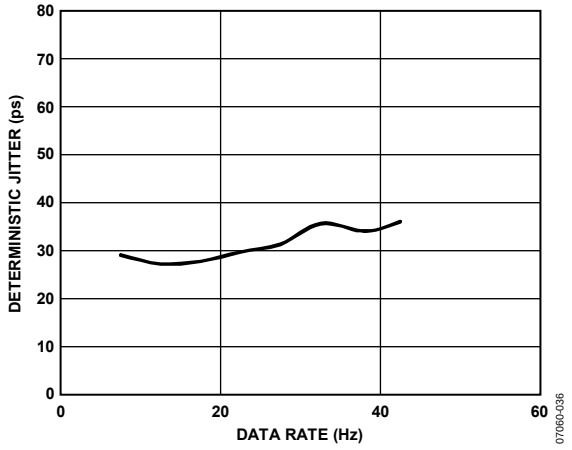

Figure 29. Deterministic Jitter vs. Data Rate

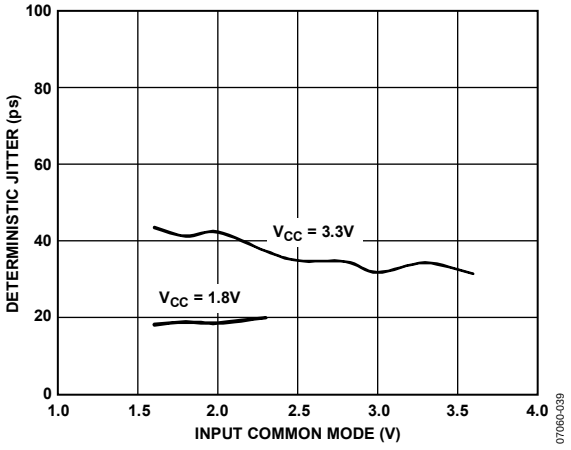

Figure 32. Deterministic Jitter vs. Input Common Mode

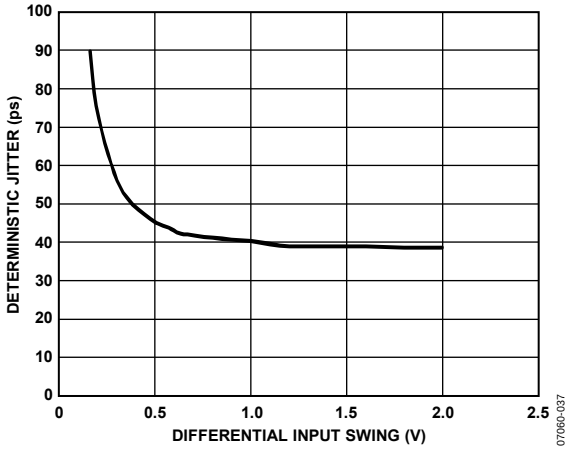

Figure 30. Deterministic Jitter vs. Differential Input Swing

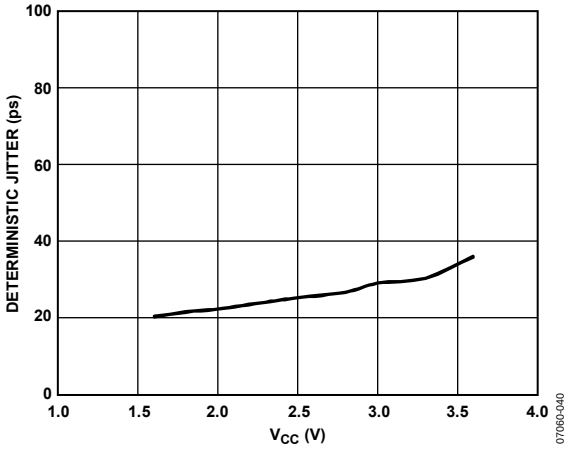

Figure 33. Deterministic Jitter vs. Supply Voltage

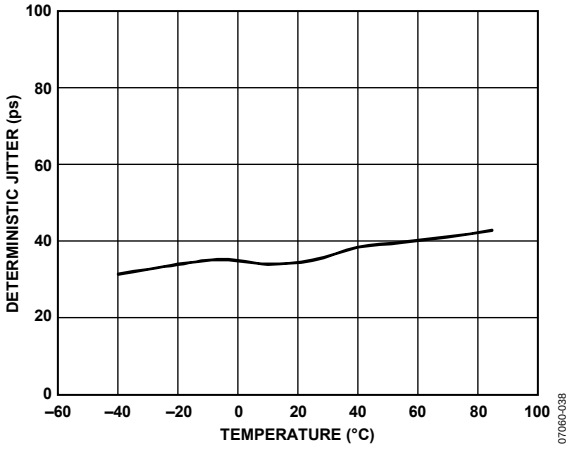

Figure 31. Deterministic Jitter vs. Temperature

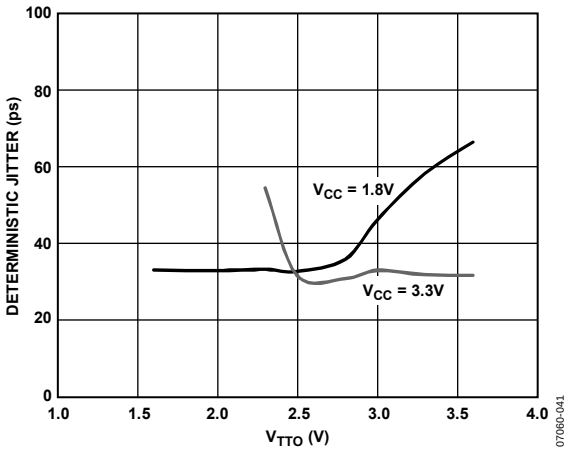

Figure 34. Deterministic Jitter vs. Output Termination Voltage

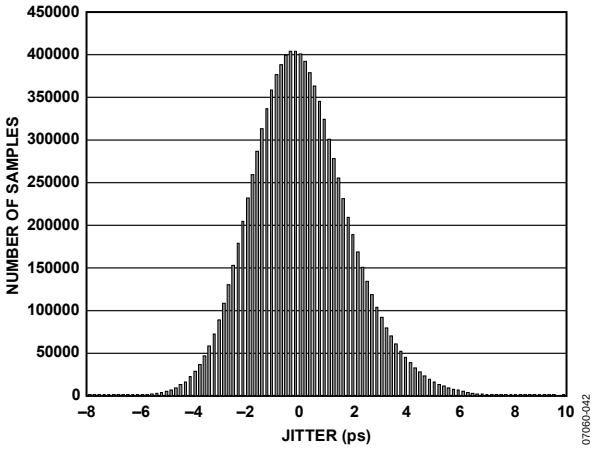

Figure 35. Random Jitter Histogram

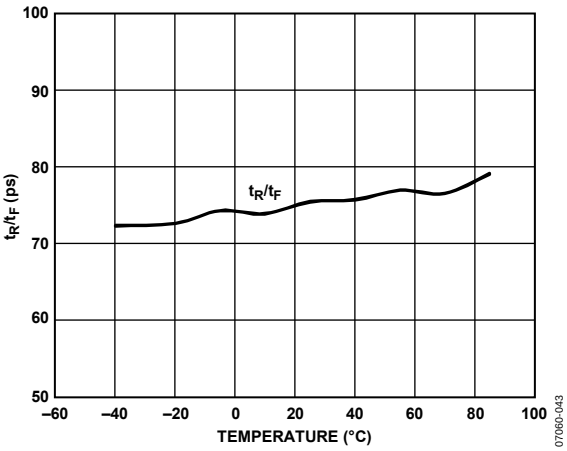

Figure 36. Rise Time (t_R)/Fall Time (t_F) vs. Temperature

THEORY OF OPERATION

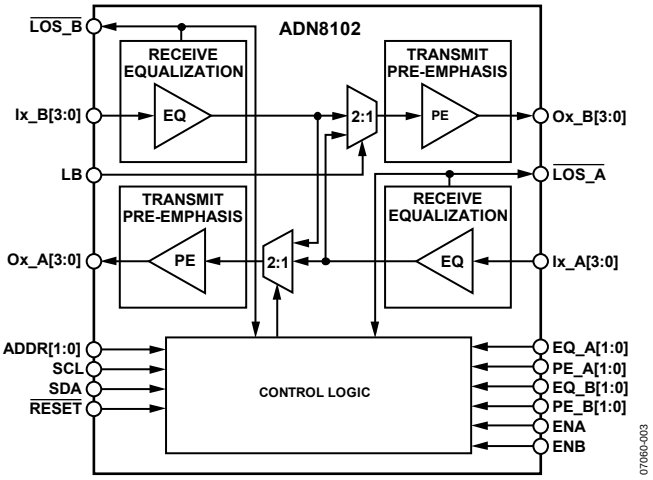

Figure 37. Simplified Functional Block Diagram

INTRODUCTION

The ADN8102 is a quad bidirectional cable and backplane equalizer that provides both input equalization and output pre-emphasis on both the line card and cable sides of the device. The device supports full loopback and through connectivity of the two unidirectional half-links, each consisting of four differential signal pairs.

The ADN8102 offers extensively programmable output levels and pre-emphasis as well as the ability to disable the output current. The receivers integrate a programmable, multizero equalizer transfer function that is optimized to compensate either typical backplane or typical cable losses.

The I/O on-chip termination resistors are terminated to user-settable supplies to support dc coupling in a wide range of logic styles. The ADN8102 supports a wide core supply range; V_{CC} can be set from 1.8 V to 3.3 V. These features, together with programmable output levels, allow for a wide range of dc- and ac-coupled I/O configurations.

RECEIVERS

Input Structure and Input Levels

The ADN8102 receiver inputs incorporate 50 Ω termination resistors, ESD protection, and a multizero transfer function equalizer that can be optimized for backplane or cable operation. Each channel also provides a programmable loss-of-signal (LOS) function that provides an interrupt that can be used to squelch or disable the associated output when the differential input voltage falls below the programmed threshold value. Each receive channel also provides a P/N inversion function that allows the user to swap the sign of the input signal path to eliminate the need for board-level crossovers in the receiver channel.

Table 5 illustrates some, but not all, possible combinations of input supply voltages.

Table 5. Common Input Voltage Levels

Configuration	V_{CC} (V)	V_{TTI} (V)
Low V_{TTI}, AC-Coupled Input	1.8	1.6
Single 1.8 V Supply	1.8	1.8
3.3 V Core	3.3	1.8
Single 3.3 V Supply	3.3	3.3

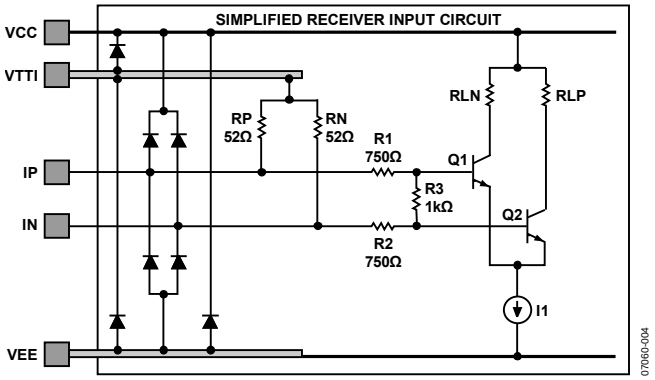

Figure 38. Simplified Input Structure

EQUALIZATION SETTINGS

The ADN8102 receiver incorporates a multizero transfer function continuous time equalizer that provides up to 22 dB of high frequency boost at 1.875 GHz to compensate up to 30 meters of CX4 cable or 40 inches of FR4 at 3.75 Gbps. The ADN8102 allows joint control of the equalizer transfer function of the four equalizer channels in a single port through the I²C control interface. Port A and Port B equalizer transfer functions are controlled via Register 0x80 and Register 0xA0, respectively. The equalizer transfer function allows independent control of the boost in two different frequency ranges for optimal matching with the loss shape of the user's channel (for example, skin-effect loss dominated or dielectric loss dominated). By default, the equalizer control is simplified to two independent maps of basic settings that provide nine settings, each optimized for CX4 cable and FR4 to ease programming for typical channels. The default state of the part selects the CX4 optimized equalization map for the IN_A[3:0] channels that interface with the cable and the FR4 optimized equalization map for the IN_B[3:0] channels that interface with the board. Full control of the equalizer is available via the I²C control interface by writing register bit MODE[0] = 1 at Address 0x0F. Table 6 summarizes the high frequency boost for each of the basic control settings and the typical length of CX4 cable and FR4 trace that each setting compensates. Setting the EQBY bit of the IN_A/IN_B configuration registers high sets the equalization to 1.5 dB of boost, which compensates 0 meters to 2 meters of CX4 or 0 inches to 10 inches of FR4.

Setting the LUT SELECT bit = 1 (Bit 1 in the IN_Ax/IN_Bx FR4 control registers) allows the default map selection (CX4 or FR4 optimized) to be overwritten via the LUT FR4/CX4 bit (Bit 0) in the IN_Ax/IN_Bx FR4 control registers. Setting this bit high selects the FR4 optimized map, and setting it low selects the CX4 optimized map. These settings are set on a per channel basis (see Table 7 and Table 17).

The user can also specify the boost in the mid frequency and high frequency ranges independently. This is done by writing to the IN_A/IN_B EQ1 control and IN_A/IN_B EQ2 control registers for the channel of interest. Each of these registers provides 32 settings of boost, with IN_A/IN_B EQ1 control setting the mid-frequency boost and IN_A/IN_B EQ2 control setting the high frequency boost. The IN_A/IN_B EQx control registers are ordered such that Bit 5 is a sign bit, and midlevel boost is centered on 0x00; setting Bit 5 low and increasing the LSBs results in decreasing boost, while setting Bit 5 high and increasing the LSBs results in increasing boost. The EQ CTL SRC bit (Bit 6) in the IN_A/IN_B EQ1 Control registers determines whether the equalization control for the channel of interest is selected from the optimized map or directly from the IN_A/IN_B EQx control registers (per port). Setting this bit high selects equalization control directly from the IN_A/IN_B EQx control registers, and setting it low selects equalization control from the selected optimized map.

Table 6. Receive Equalizer Boost vs. Setting (CX4 and FR4 Optimized Maps)

IN_Ax/IN_Bx Configuration, EQ[2:0]	Cable Optimized		FR4 Optimized	
	Boost (dB)	Typical CX4 Cable Length (Meters)	Boost (dB)	Typical FR4 Trace Length (Inches)
0[1]	10	4 to 6	3.5	5 to 10
1	12	8 to 10	3.9	10 to 15
2[1]	14	12 to 14	4.25	15 to 20
3	17	16 to 18	4.5	20 to 25
4	19	20 to 22	4.75	25 to 30
5[1]	20	24 to 26	5.0	30 to 35
6	21	28 to 30	5.3	35 to 40
7[1]	22	30 to 32	5.5	35 to 40

[1] These EQ settings are also available via the external device pins, EQ_A[1:0] and EQ_B[1:0].

Table 7. Receive Configuration and Equalization Registers

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
IN_A/IN_B Configuration	0x80, 0xA0		PNSWAP	EQBY	EN		EQ[2]	EQ[1]	EQ[0]	0x30
IN_A/IN_B EQ1 Control	0x83, 0xA3		EQ CTL SRC	EQ1[5]	EQ1[4]	EQ1[3]	EQ1[2]	EQ1[1]	EQ1[0]	0x00
IN_A/IN_B EQ2 Control	0x84, 0xA4			EQ2[5]	EQ2[4]	EQ2[3]	EQ2[2]	EQ2[1]	EQ2[0]	0x00
IN_Ax/IN_Bx FR4 Control	0x85, 0x8D, 0x95, 0x9D, 0xA5, 0xAD, 0xB5, 0xBD							LUT SELECT	LUT FR4/CX4	0x00

Loss of Signal/Signal Detect

An independent signal detect output is provided for all eight input ports of the device. The signal-detect function measures the low frequency amplitude of the signal at the receiver input and compares this measurement with a defined threshold level. If the measurement indicates that the input signal swing is smaller than the threshold for 250 µs, the channel indicates a loss-of-signal event. Assertion and deassertion of the LOS signal occurs within 100 µs of the event.

The LOS-assert and LOS-deassert levels are set on a per channel basis through the I²C control interface, by writing to the IN_A/IN_B LOS threshold and IN_A/IN_B LOS hysteresis registers, respectively. The recommended settings are IN_A/IN_B THRESH = 0x0C and IN_A/IN_B HYST = 0x0D. All ports are factory tested with these settings to ensure that an LOS event is asserted for single-ended dc input swings less than 20 mV and is deasserted for single-ended dc input swings greater than 225 mV.

The LOS status for each individual channel can be accessed through the I²C control interface. The independent channel LOS status can be read from the IN_A/IN_B LOS status registers (Address 0x1F and Address 0x3F). The four LSBs of each register represent the current LOS status of each channel, with high representing an ongoing LOS event. The four MSBs of each register represent the historical LOS status of each channel, with high representing a LOS event at any time on a specific channel. The MSBs are sticky and remain high once asserted until cleared by the user by overwriting the bits to 0.

Recommended LOS Settings

Recommended settings for LOS are as follows:

- Set IN_A/IN_B THRESH to 0x0C for an assert voltage of 20 mV differential (40 mV p-p differential).
- Set IN_A/IN_B HYST to 0x0D for a deassert voltage of 225 mV differential (450 mV p-p differential).

LANE INVERSION

The input P/N inversion is a feature intended to allow the user to implement the equivalent of a board-level crossover in a much smaller area and without additional via impedance discontinuities that degrade the high frequency integrity of the signal path. The P/N inversion is available on a per port basis and is controlled through the I²C control interface. The P/N inversion is accomplished by writing to the PNSWAP bit (Bit 6) of the IN_A/IN_B configuration register (see Table 7) with low representing a noninverting configuration and high representing an inverting configuration. Note that using this feature to account for signal inversions downstream of the receiver requires additional attention when switching connectivity.

Table 8. LOS Threshold and Hysteresis Control Registers

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
IN_A/IN_B LOS Threshold	0x81, 0xA1		THRESH[6]	THRESH[5]	THRESH[4]	THRESH[3]	THRESH[2]	THRESH[1]	THRESH[0]	0x04
IN_A/IN_B LOS Hysteresis	0x82, 0xA2		HYST[6]	HYST[5]	HYST[4]	HYST[3]	HYST[2]	HYST[1]	HYST[0]	0x12

Table 9. LOS Status Registers

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IN_A/IN_B LOS Status	0x1F, 0x3F	STICKY LOS[3]	STICKY LOS[2]	STICKY LOS[1]	STICKY LOS [0]	REAL-TIME LOS[3]	REAL-TIME LOS[2]	REAL-TIME LOS[1]	REAL-TIME LOS[0]

LOOPBACK

The ADN8102 provides loopback on both input ports (Port A: cable interface input, Port B: line card interface input). The external loopback toggle pin, LB, controls the loopback of the Port B input only (board side loopback). When loopback is asserted, valid data continues to pass through the Port B link, but the Port B input signals are also shunted to the Port A output to allow testing and debugging without disrupting valid data. This loopback, as well as loopback of the Port A input (cable side loopback), can be programmed through the I²C interface. The loopbacks are controlled through the I²C interface by writing to Bit 0 and Bit 1 of the global configuration control register (Register 0x02).

Bit 1 represents loopback of the Port A inputs to the Port B outputs (cable side loopback). Bit 0 represents loopback of the Port B inputs to the Port A outputs (board side loopback), with high representing loopback for both bits. Bit 0 is also controlled through the LB pin with I²C data overwriting the pin state. Both input ports can be looped back simultaneously (full loopback) by writing high to both Bit 0 and Bit 1, but in this case, valid data is disrupted on each channel. Figure 39 illustrates the three loopback modes.

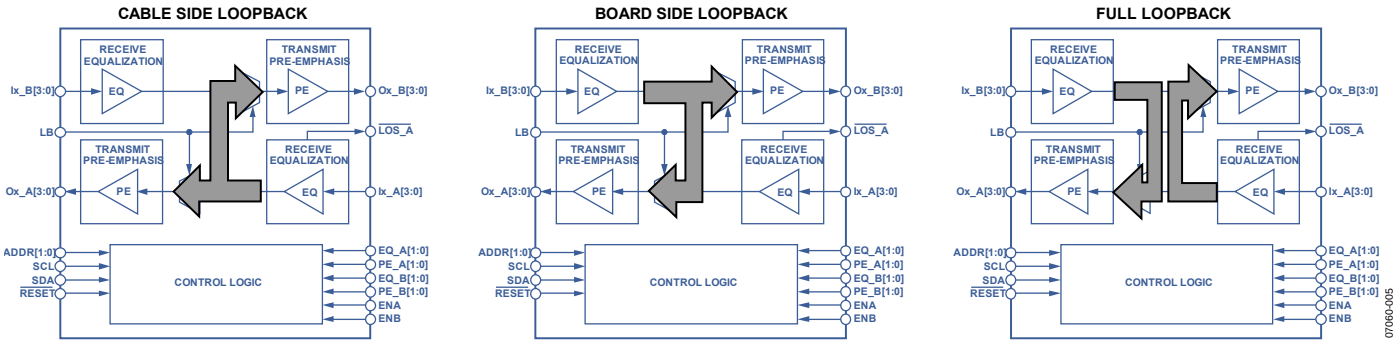

Figure 39. Loopback Modes of Operation

Table 10. Global Configuration Register, Loopback Controls

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Global Configuration Control	0x02							LB[1]	LB[0]	0x00

TRANSMITTERS

Output Structure and Output Levels

The ADN8102 transmitter outputs incorporate 50 Ω termination resistors, ESD protection, and an output current switch. Each port provides control of both the absolute output level and the pre-emphasis output level. It should be noted that the choice of output level affects the output common-mode level. A 600 mV peak-to-peak differential output level with full pre-emphasis range requires an output termination voltage of 2.5 V or greater (V_{TTO}, $V_{CC} \geq 2.5$ V).

Pre-Emphasis

The total output amplitude and pre-emphasis setting space is reduced to a single map of basic settings that provides seven settings of output equalization to ease programming for typical channels. The PE_A/PE_B[1:0] pins provide selections 0, 2, 4, and 6 of the seven pre-emphasis settings through toggle pin control, covering the entire range of settings at lower resolution. The full resolution of seven settings is available through the I²C interface by writing to Bits[2:0] (PE[2:0] of the OUT_A/OUT_B configuration registers) with I²C settings overriding the toggle pin control. Similar to the receiver settings, the ADN8102 allows joint control of all four channels in a transmit port. Table 11 summarizes the absolute output level, pre-emphasis level, and high frequency boost for each of the basic control settings and the typical length of the CX4 cable and FR4 trace that each setting compensates.

Full control of the transmit output levels is available through the I²C control interface. This full control is achieved by writing to the OUT_A/OUT_B Output Level Control[1:0] registers for the channel of interest. Table 13 shows the supported output level settings of the OUT_A/OUT_B Output Level Control[1:0] registers. Register settings not listed in Table 13 are not supported by the ADN8102.

The output equalization is optimized for less than 1.75 Gbps operation but can be optimized for higher speed applications at up to 3.75 Gbps through the I²C control interface by writing to the DATA RATE bit (Bit 4) of the OUT_A/OUT_B configuration registers, with high representing 3.75 Gbps and low representing 1.75 Gbps. The PE CTL SRC bit (Bit 7) in the OUT_A/OUT_B Output Level Control 1 register determines whether the pre-emphasis and output current controls for the channel of interest are selected from the optimized map or directly from the OUT_A/OUT_B Output Level Control[1:0] registers (per channel). Setting this bit high selects pre-emphasis control directly from the OUT_A/OUT_B Output Level Control[1:0] registers, and setting it low selects pre-emphasis control from the optimized map.

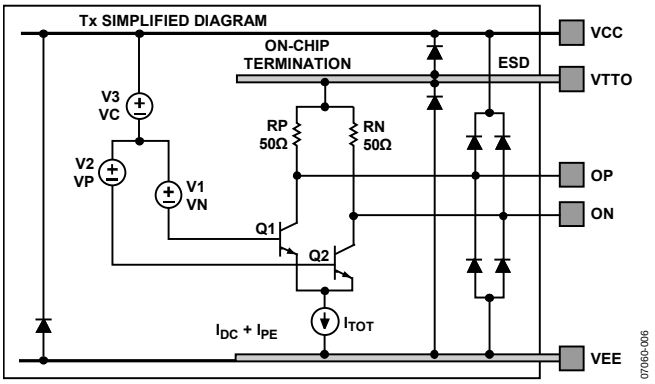

Figure 40. Simplified Output Structure

Table 11. Transmit Pre-Emphasis Boost and Overshoot vs. Setting

PE	Boost (dB)	Overshoot	DC Swing (mV p-p diff)	Typical CX4 Cable Length (Meters)	Typical FR4 Trace Length (Inches)
0[1]	0	0%	800	0 to 2.5	0 to 5
1	2	25%	800	2.5 to 5	0 to 5
2[1]	3.5	50%	800	5 to 7.5	10 to 15
3	4.9	75%	800	7.5 to 10	10 to 15
4[1]	6	100%	800	10 to 12.5	15 to 20
5	7.4	133%	600	15 to 17.5	20 to 25
6[1]	9.5	200%	400	20 to 22.5	25 to 30

[1] These PE settings are also available via external device pins, PE_A[1:0] and PE_B[1:0].

Table 12. Output Configuration Registers

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
OUT_A/OUT_B Configuration	0xC0, 0xE0			EN	DATA RATE		PE[2]	PE[1]	PE[0]	0x20
OUT_A/OUT_B Output Level Control 1	0xC1, 0xE1	PE CTL SRC	OUTx_OLEV1[6:0]							0x40
OUT_A/OUT_B Output Level Control 0	0xC2, 0xE2		OUTx_OLEV0[6:0]							0x40

Table 13. Output Level Settings

V_{OD} (mV)	V_D Peak (mV)	PE (dB)	I_{TOT} (mA)	OUT_A/OUT_B Output Level Control 0	OUT_A/OUT_B Output Level Control 1
50	50	0.00	2	0x00	0x81
50	150	9.54	6	0x11	0x81
50	250	13.98	10	0x22	0x81
50	350	16.90	14	0x33	0x81
50	450	19.08	18	0x44	0x81
50	550	20.83	22	0x55	0x81
50	650	22.28	26	0x66	0x81
100	100	0.00	4	0x00	0x91
100	200	6.02	8	0x11	0x91
100	300	9.54	12	0x22	0x91
100	400	12.04	16	0x33	0x91
100	500	13.98	20	0x44	0x91
100	600	15.56	24	0x55	0x91
100	700	16.90	28	0x66	0x91
150	150	0.00	6	0x00	0x92
150	250	4.44	10	0x11	0x92
150	350	7.36	14	0x22	0x92
150	450	9.54	18	0x33	0x92
150	550	11.29	22	0x44	0x92
150	650	12.74	26	0x55	0x92
150	750	13.98	30	0x66	0x92
200	200	0.00	8	0x00	0xA2
200	300	3.52	12	0x11	0xA2
200	400	6.02	16	0x22	0xA2
200	500	7.96	20	0x33	0xA2
200	600	9.54	24	0x44	0xA2
200	700	10.88	28	0x55	0xA2
200	800	12.04	32	0x66	0xA2
250	250	0.00	10	0x00	0xA3
250	350	2.92	14	0x11	0xA3
250	450	5.11	18	0x22	0xA3
250	550	6.85	22	0x33	0xA3
250	650	8.30	26	0x44	0xA3
250	750	9.54	30	0x55	0xA3
250	850	10.63	34	0x66	0xA3
300	300	0.00	12	0x00	0xB3
300	400	2.50	16	0x11	0xB3
300	500	4.44	20	0x22	0xB3
300	600	6.02	24	0x33	0xB3
300	700	7.36	28	0x44	0xB3
300	800	8.52	32	0x55	0xB3
300	900	9.54	36	0x66	0xB3
350	350	0.00	14	0x00	0xB4
350	450	2.18	18	0x11	0xB4
350	550	3.93	22	0x22	0xB4
350	650	5.38	26	0x33	0xB4
350	750	6.62	30	0x44	0xB4
350	850	7.71	34	0x55	0xB4
350	950	8.67	38	0x66	0xB4
400	400	0.00	16	0x00	0xC4
400	500	1.94	20	0x11	0xC4
400	600	3.52	24	0x22	0xC4
400	700	4.86	28	0x33	0xC4
400	800	6.02	32	0x44	0xC4
400	900	7.04	36	0x55	0xC4
400	1000	7.96	40	0x66	0xC4

V_{OD} (mV)	V_D Peak (mV)	PE (dB)	I_{TOT} (mA)	OUT_A/OUT_B Output Level Control 0	OUT_A/OUT_B Output Level Control 1
450	450	0.00	18	0x00	0xC5
450	550	1.74	22	0x11	0xC5
450	650	3.19	26	0x22	0xC5
450	750	4.44	30	0x33	0xC5
450	850	5.52	34	0x44	0xC5
450	950	6.49	38	0x55	0xC5
450	1050	7.36	42	0x66	0xC5
500	500	0.00	20	0x00	0xD5
500	600	1.58	24	0x11	0xD5
500	700	2.92	28	0x22	0xD5
500	800	4.08	32	0x33	0xD5
500	900	5.11	36	0x44	0xD5
500	1000	6.02	40	0x55	0xD5
500	1100	6.85	44	0x66	0xD5
550	550	0.00	22	0x00	0xD6
550	650	1.45	26	0x11	0xD6
550	750	2.69	30	0x22	0xD6
550	850	3.78	34	0x33	0xD6
550	950	4.75	38	0x44	0xD6
550	1050	5.62	42	0x55	0xD6
550	1150	6.41	46	0x66	0xD6
600	600	0.00	24	0x00	0xE6
600	700	1.34	28	0x11	0xE6
600	800	2.50	32	0x22	0xE6
600	900	3.52	36	0x33	0xE6
600	1000	4.44	40	0x44	0xE6
600	1100	5.26	44	0x55	0xE6
600	1200	6.02	48	0x66	0xE6
650	650	0.00	26	0x01	0xE6
650	750	1.24	30	0x12	0xE6
650	850	2.33	34	0x23	0xE6
650	950	3.30	38	0x34	0xE6
650	1050	4.17	42	0x45	0xE6
650	1150	4.96	46	0x56	0xE6
700	700	0.00	28	0x02	0xE6
700	800	1.16	32	0x13	0xE6
700	900	2.18	36	0x24	0xE6
700	1000	3.10	40	0x35	0xE6
700	1100	3.93	44	0x46	0xE6
750	750	0.00	30	0x03	0xE6
750	850	1.09	34	0x14	0xE6
750	950	2.05	38	0x25	0xE6
750	1050	2.92	42	0x36	0xE6
800	800	0.00	32	0x04	0xE6
800	900	1.02	36	0x15	0xE6
800	1000	1.94	40	0x26	0xE6
850	850	0.00	34	0x05	0xE6
850	950	0.97	38	0x16	0xE6
900	900	0.00	36	0x06	0xE6

High Current Setting and Output Level Shift

In low voltage applications, users must pay careful attention to both the differential and common-mode signal levels (see Figure 41 and Table 14 and Table 15. Failure to understand the implications of signal level and choice of ac or dc coupling almost certainly leads to transistor saturation and poor transmitter performance.

TxHeadroom

The TxHeadroom register (Register 0x23) allows configuration of the individual transmitters for extra headroom at the output for high current applications. The bits in this register are active high (default) and are one per output (see Table 17). Setting a bit high puts the respective transmitter in a configuration for extra headroom and setting a bit low does not provide extra headroom. The TxHeadroom bits should only be set high when V_{CC} exceeds the value listed in Table 14 for a given output swing.

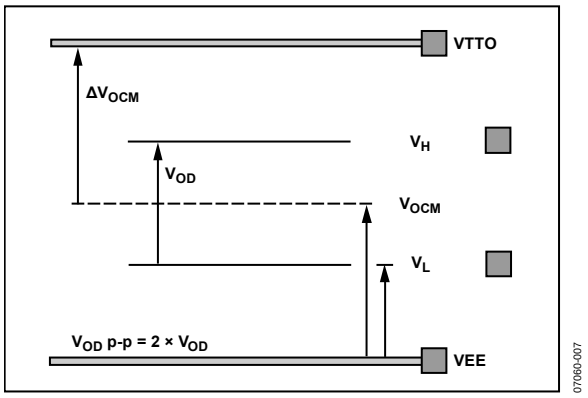

Figure 41. Simplified Output Voltage Levels Diagram

Signal Levels and Common-Mode Shift for DC- and AC-Coupled Outputs

Table 14.

Output Levels and Output Compliance						AC-Coupled Transmitter					DC-Coupled Transmitter					TxHeadroom = 0			TxHeadroom = 1	
V_{OD} (mV)	I_{TOT} (mA)	V_D Peak (mV)	PE Boost	PE (dB)	dV_{OCM} (mV)	V_H (V)	V_L (V)	V_H Peak (V)	V_L Peak (V)	dV_{OCM} (mV)	V_H (V)	V_L (V)	V_H Peak (V)	V_L Peak (V)	Min V_L (V)	Max $V_{CC} - V_L$ (V)	Min V_{CC} (V)	Min V_L (V)	Max $V_{CC} - V_L$ (V)	Min V_{CC} (V)
V_{TTO} and V_{CC} = 3.3 V																				
200	8	200	1.00	0.00	200	3.2	3	3.2	3	100	3.3	3.1	3.3	3.1	2.225	1.1	1.8	2	1.2	2
200	12	300	1.50	3.52	300	3.1	2.9	3.15	2.85	150	3.25	3.05	3.3	3	2.225	1.1	1.8	2	1.2	2
200	16	400	2.00	6.02	400	3	2.8	3.1	2.7	200	3.2	3	3.3	2.9	2.225	1.1	1.8	2	1.2	2
200	20	500	2.50	7.96	500	2.9	2.7	3.05	2.55	250	3.15	2.95	3.3	2.8	2.225	1.1	1.8	2	1.2	2
200	24	600	3.00	9.54	600	2.8	2.6	3	2.4	300	3.1	2.9	3.3	2.7	2.225	1.1	1.8	2	1.2	2
200	28	700	3.50	10.88	700	2.7	2.5	2.95	2.25	350	3.05	2.85	3.3	2.6	2.225	1.1	1.9	2	1.2	2.2
200	32	800	4.00	12.04	800	2.6	2.4	2.9	2.1	400	3	2.8	3.3	2.5	2.225	1.1	1.9	2	1.2	2.2
300	12	300	1.00	0.00	300	3.15	2.85	3.15	2.85	150	3.3	3	3.3	3	2.225	1.1	1.8	2	1.2	2
300	16	400	1.33	2.50	400	3.05	2.75	3.1	2.7	200	3.25	2.95	3.3	2.9	2.225	1.1	1.8	2	1.2	2
300	20	500	1.67	4.44	500	2.95	2.65	3.05	2.55	250	3.2	2.9	3.3	2.8	2.225	1.1	1.8	2	1.2	2
300	24	600	2.00	6.02	600	2.85	2.55	3	2.4	300	3.15	2.85	3.3	2.7	2.225	1.1	1.8	2	1.2	2
300	28	700	2.33	7.36	700	2.75	2.45	2.95	2.25	350	3.1	2.8	3.3	2.6	2.225	1.1	1.8	2	1.2	2
300	32	800	2.67	8.52	800	2.65	2.35	2.9	2.1	400	3.05	2.75	3.3	2.5	2.225	1.1	1.9	2	1.2	2.2
300	36	900	3.00	9.54	900	2.55	2.25	2.85	1.95	450	3	2.7	3.3	2.4	2.225	1.1	1.9	2	1.2	2.2
400	16	400	1.00	0.00	400	3.1	2.7	3.1	2.7	200	3.3	2.9	3.3	2.9	2.225	1.1	1.8	2	1.2	2
400	20	500	1.25	1.94	500	3	2.6	3.05	2.55	250	3.25	2.85	3.3	2.8	2.225	1.1	1.8	2	1.2	2
400	24	600	1.50	3.52	600	2.9	2.5	3	2.4	300	3.2	2.8	3.3	2.7	2.225	1.1	1.8	2	1.2	2
400	28	700	1.75	4.86	700	2.8	2.4	2.95	2.25	350	3.15	2.75	3.3	2.6	2.225	1.1	1.8	2	1.2	2
400	32	800	2.00	6.02	800	2.7	2.3	2.9	2.1	400	3.1	2.7	3.3	2.5	2.225	1.1	1.8	2	1.2	2
400	36	900	2.25	7.04	900	2.6	2.2	2.85	1.95	450	3.05	2.65	3.3	2.4	2.225	1.1	1.9	2	1.2	2.2
400	40	1000	2.50	7.96	1000	2.5	2.1	2.8	1.8	500	3	2.6	3.3	2.3	2.225	1.1	1.9	2	1.2	2.2
600	24	600	1.00	0.00	600	3	2.4	3	2.4	300	3.3	2.7	3.3	2.7	2.1	1.1	1.9	2	1.2	2.2
600	28	700	1.17	1.34	700	2.9	2.3	2.95	2.25	350	3.25	2.65	3.3	2.6	2.225	1.1	1.9	2	1.2	2.2
600	32	800	1.33	2.50	800	2.8	2.2	2.9	2.1	400	3.2	2.6	3.3	2.5	2.225	1.1	1.9	2	1.2	2.2
600	36	900	1.50	3.52	900	2.7	2.1	2.85	1.95	450	3.15	2.55	3.3	2.4	2.225	1.1	1.9	2	1.2	2.2
600	40	1000	1.67	4.44	1000	2.6	2	2.8	1.8	500	3.1	2.5	3.3	2.3	2.225	1.1	1.9	2	1.2	2.2
600	44	1200	1.83	5.26	1100	2.5	1.9	2.75	1.65	550	3.05	2.45	3.3	2.2	2.1	1.1	1.9	2	1.2	2.2
600	48	1400	2.00	6.02	1200	2.4	1.8	2.7	1.5	600	3	2.4	3.3	2.1	2.1	1.1	1.9	2	1.2	2.2
V_{TTO} and V_{CC} = 1.8 V[1]																				
200	8	200	1.00	0.00	200	1.7	1.5	1.7	1.5	100	1.8	1.6	1.8	1.6	0.725	1.1	1.8	0.5	NA	NA
200	12	300	1.50	3.52	300	1.6	1.4	1.65	1.35	150	1.75	1.55	1.8	1.5	0.725	1.1	1.8	0.5	NA	NA
200	16	400	2.00	6.02	400	1.5	1.3	1.6	1.2	200	1.7	1.5	1.8	1.4	0.725	1.1	1.8	0.5	NA	NA
200	20	500	2.50	7.96	500	1.4	1.2	1.55	1.05	250	1.65	1.45	1.8	1.3	0.725	1.1	1.8	0.5	NA	NA
200	24	600	3.00	9.54	600	1.3	1.1	1.5	0.9	300	1.6	1.4	1.8	1.2	0.725	1.1	1.8	0.5	NA	NA
300	12	300	1.00	0.00	300	1.65	1.35	1.65	1.35	150	1.8	1.5	1.8	1.5	0.725	1.1	1.8	0.5	NA	NA
300	16	400	1.33	2.50	400	1.55	1.25	1.6	1.2	200	1.75	1.45	1.8	1.4	0.725	1.1	1.8	0.5	NA	NA
300	20	500	1.67	4.44	500	1.45	1.15	1.55	1.05	250	1.7	1.4	1.8	1.3	0.725	1.1	1.8	0.5	NA	NA
300	24	600	2.00	6.02	600	1.35	1.05	1.5	0.9	300	1.65	1.35	1.8	1.2	0.725	1.1	1.8	0.5	NA	NA
300	28	700	2.33	7.36	700	1.25	0.95	1.45	0.75	350	1.6	1.3	1.8	1.1	0.725	1.1	1.8	0.5	NA	NA
400	16	400	1.00	0.00	400	1.6	1.2	1.6	1.2	200	1.8	1.4	1.8	1.4	0.725	1.1	1.8	0.5	NA	NA
400	20	500	1.25	1.94	500	1.5	1.1	1.55	1.05	250	1.75	1.35	1.8	1.3	0.725	1.1	1.8	0.5	NA	NA
400	24	600	1.50	3.52	600	1.4	1	1.5	0.9	300	1.7	1.3	1.8	1.2	0.725	1.1	1.8	0.5	NA	NA
400	28	700	1.75	4.86	700	1.3	0.9	1.45	0.75	350	1.65	1.25	1.8	1.1	0.725	1.1	1.8	0.5	NA	NA
400	32	800	2.00	6.02	800	1.2	0.8	1.4	0.6	400	1.6	1.2	1.8	1	0.725	1.1	1.8	0.5	NA	NA
600	24	600	1.00	0.00	600	1.5	0.9	1.5	0.9	300	1.8	1.2	1.8	1.2	0.6	1.1	1.9	0.5	NA	NA

[1] TxHeadroom = 1 is not an option at V_{TTO} and V_{CC} = 1.8 V.

Table 15. Symbol Definitions for Output Levels vs. Setting

Symbol	Formula	Definition
V_{OD}	$25\ \Omega \times I_{DC}$	Peak differential output voltage
V_{OD} p-p	$25\ \Omega \times I_{DC} \times 2 = 2 \times V_{OD}$	Peak-to-peak differential output voltage
$dV_{OCM\_DC\text{-}COUPLED}$	$25\ \Omega \times I_{TOT}/2 = V_{OD}$ p-p/4 + ($I_{PE}/2 \times 25$)	Output common-mode shift
$dV_{OCM\_AC\text{-}COUPLED}$	$50\ \Omega \times I_{TOT}/2 = V_{OD}$ p-p/2 + ($I_{PE}/2 \times 50$)	Output common-mode shift
I_{DC}	V_{OD}/R_{TERM}	Output current that sets output level
I_{PE}	—	Output current used for PE
I_{TOT}	$I_{DC} + I_{PE}$	Total transmitter output current
V_H	$V_{TTO} - dV_{OCM} + V_{OD}/2$	Maximum single-ended output voltage
V_L	$V_{TTO} - dV_{OCM} - V_{OD}/2$	Minimum single-ended output voltage

SELECTIVE SQUELCH AND DISABLE

Each transmitter is equipped with output disable and output squelch controls. Disable is a full power-down state: the transmitter current is reduced to zero and the output pins pull up to VTTO, but there is a delay of approximately 1 µs associated with re-enabling the transmitter. The output disable control is accessed through the EN bit (Bit 5) of the OUT_A/OUT_B configuration registers through the I²C control interface.

Squelch is not a full power-down state but a state in which only the output current is reduced to zero and the output pins pull up to VTTO, and there is a much smaller delay to bring back the output current. The output squelch and the output disable control can both be accessed through the OUT_A/OUT_B squelch control registers, with the top nibble representing the squelch control for one entire output port and the bottom nibble representing the output disable for one entire output port. The ports are disabled or squelched by writing 0s to the corresponding nibbles. The ports are enabled by writing all 1s, which is the default setting. For example, to squelch Port A, Register 0xC3 must be set to 0x0F. The entire nibble must be written to all 0s for this functionality.

Table 16. Squelch Programming

Name	Address	Data		Default
OUT_A/ OUT_B Squelch Control	0xC3, 0xE3	$\overline{\text{SQUELCH[3:0]}}$	$\overline{\text{DISABLE[3:0]}}$	0xFF

I²C CONTROL INTERFACE

SERIAL INTERFACE GENERAL FUNCTIONALITY

The ADN8102 register set is controlled through a 2-wire I²C interface. The ADN8102 acts only as an I²C slave device. Therefore, the I²C bus in the system needs to include an I²C master to configure the ADN8102 and other I²C devices that may be on the bus. Data transfers are controlled using the two I²C wires: the SCL input clock pin and the SDA bidirectional data pin.

The ADN8102 I²C interface can be run in the standard (100 kHz) and fast (400 kHz) modes. The SDA line only changes value when the SCL pin is low with two exceptions. To indicate the beginning or continuation of a transfer, the SDA pin is driven low while the SCL pin is high, and to indicate the end of a transfer, the SDA line is driven high while the SCL line is high. Therefore, it is important to control the SCL clock to toggle only when the SDA line is stable, unless indicating a start, repeated start, or stop condition.

I²C INTERFACE DATA TRANSFERS—DATA WRITE

To write data to the ADN8102 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the ADN8102 slave device. The steps that need to be completed are listed as follows, where the signals are controlled by the I²C master, unless otherwise specified. A diagram of the procedure can be seen in Figure 42.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the ADN8102 part address (seven bits) whose upper five bits are the static value 10010b and whose lower two bits are controlled by the ADDR[1:0] input pins. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN8102 to acknowledge the request.
5. Send the register address (eight bits) to which data is to be written. This transfer should be MSB first.
6. Wait for the ADN8102 to acknowledge the request.
7. Send the data (eight bits) to be written to the register whose address was set in Step 5. This transfer should be MSB first.
8. Wait for the ADN8102 to acknowledge the request.

9a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.

9b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 in this procedure to perform another write.

9c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the read procedure (in the I2C Interface Data Transfers—Data Read section) to perform a read from another address.

9d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of the read procedure (in the I2C Interface Data Transfers—Data Read section) to perform a read from the same address set in Step 5.

Figure 42 shows the ADN8102 write process. The SCL signal is shown along with a general write operation and a specific example. In the example, Data 0x92 is written to Address 0x6D of an ADN8102 part with a part address of 0x4B. The part address is seven bits wide. The upper five bits of the ADN8102 are internally set to 10010b. The lower two bits are controlled by the ADDR[1:0] pins. In this example, the bits controlled by the ADDR[1:0] pins are set to 11b. In Figure 42, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the ADN8102 slave. As for the SDA line, the data in the shaded polygons is driven by the ADN8102, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of Step 9a.

Note that the SDA line only changes when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, Step 1 and Step 9 in this case.

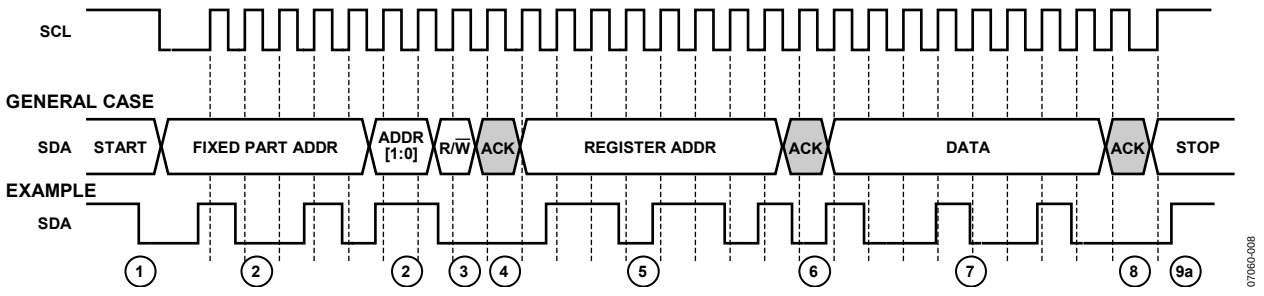

Figure 42. I²C Write Diagram

I²C INTERFACE DATA TRANSFERS—DATA READ

To read data from the ADN8102 register set, a microcontroller, or any other I²C master, needs to send the appropriate control signals to the ADN8102 slave device. The steps that need to be completed are listed as follows, where the signals are controlled by the I²C master, unless otherwise specified. A diagram of the procedure can be seen in Figure 43.

1. Send a start condition (while holding the SCL line high, pull the SDA line low).
2. Send the ADN8102 part address (seven bits) whose upper five bits are the static value 10010b and whose lower two bits are controlled by the input pins ADDR[1:0]. This transfer should be MSB first.
3. Send the write indicator bit (0).
4. Wait for the ADN8102 to acknowledge the request.
5. Send the register address (eight bits) from which data is to be read. This transfer should be MSB first. The register address is kept in memory in the ADN8102 until the part is reset or the register address is written over with the same procedure (Step 1 to Step 6).
6. Wait for the ADN8102 to acknowledge the request.
7. Send a repeated start condition (while holding the SCL line high, pull the SDA line low).
8. Send the ADN8102 part address (seven bits) whose upper five bits are the static value 10010b and whose lower two bits are controlled by the input pins ADDR[1:0]. This transfer should be MSB first.
9. Send the read indicator bit (1).
10. Wait for the ADN8102 to acknowledge the request.
11. The ADN8102 then serially transfers the data (eight bits) held in the register indicated by the address set in Step 5.
12. Acknowledge the data.

13a. Send a stop condition (while holding the SCL line high, pull the SDA line high) and release control of the bus.

13b. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of the write procedure (in the I2C Interface Data Transfers—Data Write section) to perform a write.

13c. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 2 of this procedure to perform a read from a another address.

13d. Send a repeated start condition (while holding the SCL line high, pull the SDA line low) and continue with Step 8 of this procedure to perform a read from the same address.

Figure 43 shows the ADN8102 read process. The SCL signal is shown along with a general read operation and a specific example. In the example, Data 0x49 is read from Address 0x6D of an ADN8102 part with a part address of 0x4B. The part address is seven bits wide. The upper five bits of the ADN8102 are internally set to 10010b. The lower two bits are controlled by the ADDR[1:0] pins. In this example, the bits controlled by the ADDR[1:0] pins are set to 11b. In Figure 43, the corresponding step number is visible in the circle under the waveform. The SCL line is driven by the I²C master and never by the ADN8102 slave. As for the SDA line, the data in the shaded polygons is driven by the ADN8102, whereas the data in the nonshaded polygons is driven by the I²C master. The end phase case shown is that of Step 13a.

Note that the SDA line changes only when the SCL line is low, except for the case of sending a start, stop, or repeated start condition, as in Step 1, Step 7, and Step 13. In Figure 43, A is the same as ACK in Figure 42. Equally, Sr represents a repeated start where the SDA line is brought high before SCL is raised. SDA is then dropped while SCL is still high.

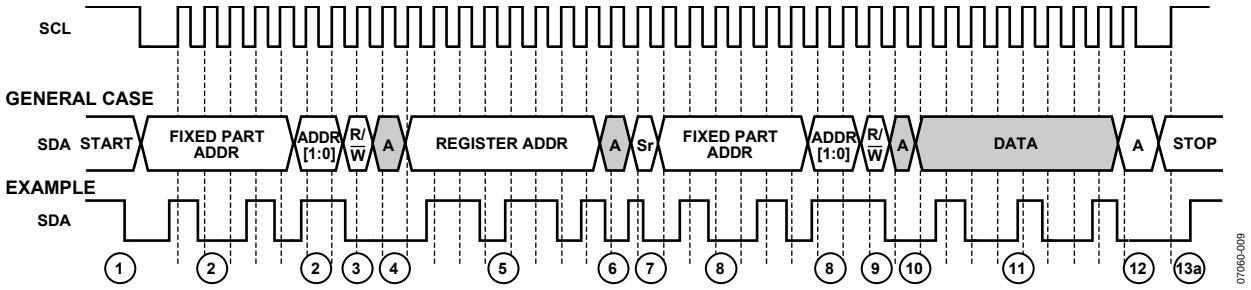

Figure 43. I²C Read Diagram

PCB DESIGN GUIDELINES

Proper RF PCB design techniques must be used for optimal performance.

POWER SUPPLY CONNECTIONS AND GROUND PLANES

Use of one low impedance ground plane is recommended. The VEE pins should be soldered directly to the ground plane to reduce series inductance. If the ground plane is an internal plane and connections to the ground plane are made through vias, multiple vias can be used in parallel to reduce the series inductance. The exposed pad should be connected to the VEE plane using plugged vias so that solder does not leak through the vias during reflow.

Use of a 10 μF electrolytic capacitor between VCC and VEE is recommended at the location where the 3.3 V supply enters the printed circuit board (PCB). It is recommended that 0.1 μF and 1 nF ceramic chip capacitors be placed in parallel at each supply pin for high frequency power supply decoupling. When using 0.1 μF and 1 nF ceramic chip capacitors, they should be placed between the IC power supply pins (VCC, VTTI, and VTTO) and VEE, as close as possible to the supply pins.

By using adjacent power supply and GND planes, excellent high frequency decoupling can be realized by using close spacing between the planes. This capacitance is given by

$$C_{PLANE} = 0.88\varepsilon_r \times A/d \text{ (pF)}$$

where:
ε_r is the dielectric constant of the PCB material.
A is the area of the overlap of power and GND planes (cm^2).
d is the separation between planes (mm).

For FR4, $\varepsilon_r = 4.4$, and 0.25 mm spacing, C ≈ 15 pF/cm^2.

TRANSMISSION LINES

Use of 50 Ω transmission lines is required for all high frequency input and output signals to minimize reflections. It is also necessary for the high speed pairs of differential input traces to be matched in length, as well as the high speed pairs of differential output traces, to avoid skew between the differential traces.

SOLDERING GUIDELINES FOR CHIP SCALE PACKAGE

The lands on the LFCSP are rectangular. The PCB pad for these should be 0.1 mm longer than the package land length and 0.05 mm wider than the package land width. Center the land on the pad, which ensures that the solder joint size is maximized. The bottom of the chip scale package has a central exposed pad. The pad on the PCB should be at least as large as this exposed pad. The user must connect the exposed pad to VEE using plugged vias so that solder does not leak through the vias during reflow. This ensures a solid connection from the exposed pad to VEE.

REGISTER MAP

Table 17. I²C Register Definitions

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Reset	0x00								RESET	
Global Configuration Control	0x02							LB[1]	LB[0]	0x00
Mode	0x0F							MODE[1]	MODE[0]	0x00
TxHeadroom	0x23	TxH_B3	TxH_B2	TxH_B1	TxH_B0	TxH_A3	TxH_A2	TxH_A1	TxH_A0	0x00
IN_A Configuration	0x80		PNSWAP	EQBY	EN		EQ[2]	EQ[1]	EQ[0]	0x30
IN_A LOS Threshold	0x81		THRESH[6]	THRESH[5]	THRESH[4]	THRESH[3]	THRESH[2]	THRESH[1]	THRESH[0]	0x04
IN_A LOS Hysteresis	0x82		HYST[6]	HYST[5]	HYST[4]	HYST[3]	HYST[2]	HYST[1]	HYST[0]	0x12
IN_A LOS Status[1]	0x1F	STICKY LOS[3]	STICKY LOS[2]	STICKY LOS[1]	STICKY LOS[0]	REAL-TIME LOS[3]	REAL-TIME LOS[2]	REAL-TIME LOS[1]	REAL-TIME LOS[0]	
IN_A EQ1 Control	0x83		EQ CTL SRC	EQ1[5]	EQ1[4]	EQ1[3]	EQ1[2]	EQ1[1]	EQ1[0]	0x00
IN_A EQ2 Control	0x84			EQ2[5]	EQ2[4]	EQ2[3]	EQ2[2]	EQ2[1]	EQ2[0]	0x00
IN_A0 FR4 Control	0x85							LUT SELECT	LUT FR4/CX4	0x00
IN_A1 FR4 Control	0x8D							LUT SELECT	LUT FR4/CX4	0x00
IN_A2 FR4 Control	0x95							LUT SELECT	LUT FR4/CX4	0x00
IN_A3 FR4 Control	0x9D							LUT SELECT	LUT FR4/CX4	0x00
IN_B Configuration	0xA0		PNSWAP	EQBY	EN		EQ[2]	EQ[1]	EQ[0]	0x30
IN_B LOS Threshold	0xA1		THRESH[6]	THRESH[5]	THRESH[4]	THRESH[3]	THRESH[2]	THRESH[1]	THRESH[0]	0x04
IN_B LOS Hysteresis	0xA2		HYST[6]	HYST[5]	HYST[4]	HYST[3]	HYST[2]	HYST[1]	HYST[0]	0x12
IN_B LOS Status[1]	0x3F	STICKY LOS [3]	STICKY LOS [2]	STICKY LOS [1]	STICKY LOS[0]	REAL-TIME LOS[3]	REAL-TIME LOS[2]	REAL-TIME LOS[1]	REAL-TIME LOS[0]	
IN_B EQ1 Control	0xA3		EQ CTL SRC	EQ1[5]	EQ1[4]	EQ1[3]	EQ1[2]	EQ1[1]	EQ1[0]	0x00
IN_B EQ2 Control	0xA4			EQ2[5]	EQ2[4]	EQ2[3]	EQ2[2]	EQ2[1]	EQ2[0]	0x00
IN_B3 FR4 Control	0xA5							LUT SELECT	LUT FR4/CX4	0x00
IN_B2 FR4 Control	0xAD							LUT SELECT	LUT FR4/CX4	0x00
IN_B1 FR4 Control	0xB5							LUT SELECT	LUT FR4/CX4	0x00
IN_B0 FR4 Control	0xBD							LUT SELECT	LUT FR4/CX4	0x00

Name	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
OUT_A Configuration	0xC0			EN	DATA RATE		PE[2]	PE[1]	PE[0]	0x20
OUT_A Output Level Control 1	0xC1	PE CTL SRC	OUTA_OLEV1[6:0]							0x40
OUT_A Output Level Control 0	0xC2		OUTA_OLEV0[6:0]							0x40
OUT_A Squelch Control	0xC3	$\overline{\text{SQUELCH}}$[3:0]				$\overline{\text{DISABLE}}$[3:0]				0xFF
OUT_B Configuration	0xE0			EN	DATA RATE		PE[2]	PE[1]	PE[0]	0x20
OUT_B Output Level Control 1	0xE1	PE CTL SRC	OUTB_OLEV1[6:0]							0x40
OUT_B Output Level Control 0	0xE2		OUTB_OLEV0[6:0]							0x40
OUT_B Squelch Control	0xE3	$\overline{\text{SQUELCH}}$[3:0]				$\overline{\text{DISABLE}}$[3:0]				0xFF

[1] Read-only register.

OUTLINE DIMENSIONS

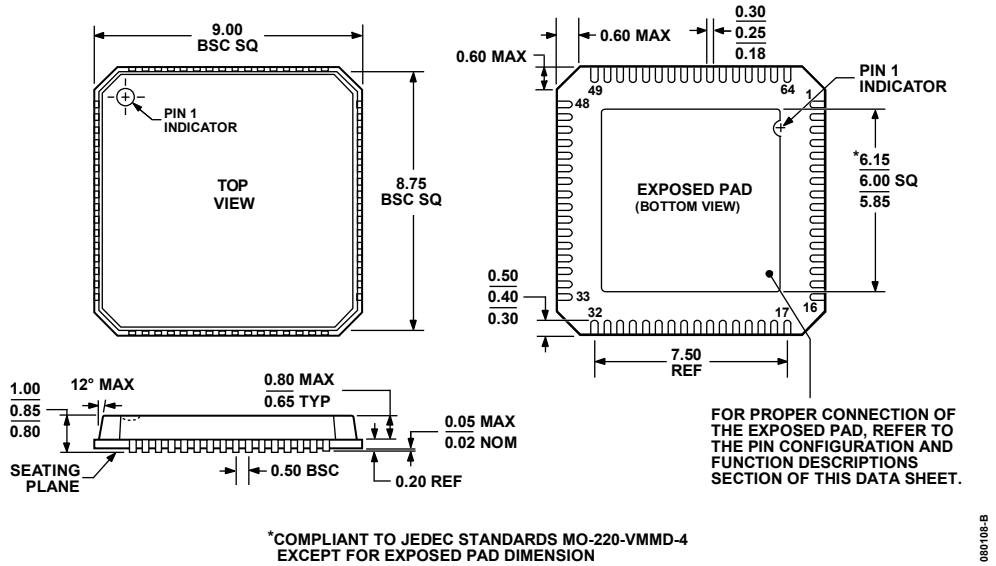

Figure 44. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm × 9 mm Body, Very Thin Quad
(CP-64-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADN8102ACPZ[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-2
ADN8102ACPZ-R7[1]	−40°C to +85°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-2
ADN8102-EVALZ[1]		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES