# 4-Bit Programmable 2-Phase Synchronous Buck Controller

# ADP3161

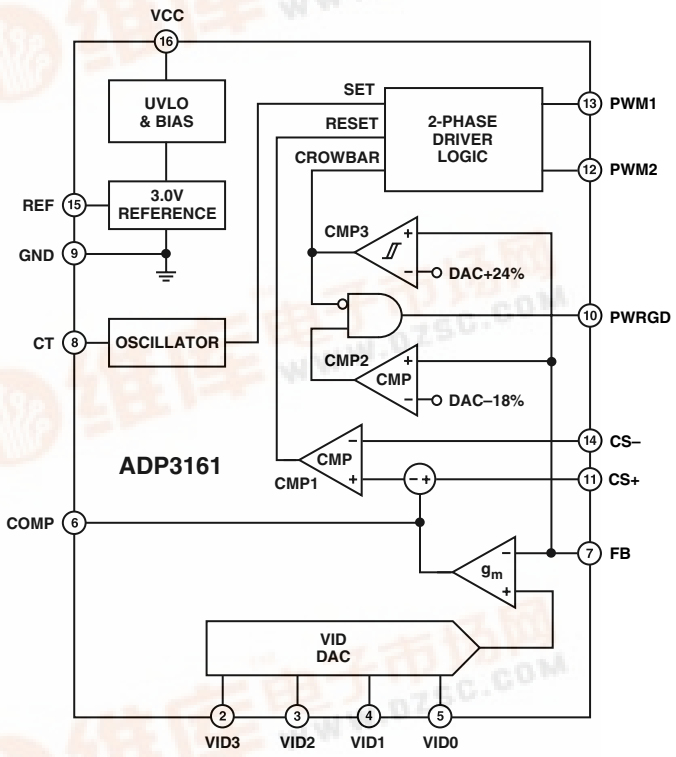
## FEATURES

- ADOPT™ Optimal Positioning Technology for Superior Load Transient Response and Fewest Output Capacitors
- Active Current Balancing Between Both Output Phases
- VRM 8.4-Compatible Digitally Programmable 1.3 V to 2.05 V Output
- Dual Logic-Level PWM Outputs for Interface to External High-Power Drivers
- Total Output Accuracy ±0.8% Over Temperature
- Current-Mode Operation
- Short Circuit Protection
- Power-Good Output
- Overvoltage Protection Crowbar Protects Microprocessors with No Additional External Components

## APPLICATIONS

- Desktop PC Power Supplies for:
  - Intel Pentium® III Processors
  - VRM Modules

## FUNCTIONAL BLOCK DIAGRAM




## GENERAL DESCRIPTION

The ADP3161 is a highly efficient dual output synchronous buck switching regulator controller optimized for converting a 5 V or 12 V main supply into the core supply voltage required by high-performance processors such as Pentium® III. The ADP3161 uses an internal 4-bit DAC to read a voltage identification (VID) code directly from the processor, which is used to set the output voltage between 1.3 V and 2.05 V. The ADP3161 uses a current mode PWM architecture to drive two logic-level outputs at a programmable switching frequency that can be optimized for VRM size and efficiency. The output signals are 180 degrees out of phase, allowing for the construction of two complementary buck switching stages. These two stages share the dc output current to reduce overall output voltage ripple. An active current balancing function ensures that both phases carry equal portions of the total load current, even under large transient loads, to minimize the size of the inductors.

The ADP3161 also uses a unique supplemental regulation technique called active voltage positioning to enhance load transient performance. Active voltage positioning results in a dc/dc converter that meets the stringent output voltage specifications for high-performance processors, with the minimum number of output capacitors and smallest footprint. Unlike voltage-mode and standard current-mode architectures, active voltage positioning adjusts the output voltage as a function of the load current so that it is always optimally positioned for a system transient. The ADP3161 also provides accurate and reliable short circuit protection and adjustable current limiting.

The ADP3161 is specified over the commercial temperature range of 0°C to 70°C and is available in a 16-lead narrow body SOIC package.

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# ADP3161–SPECIFICATIONS[1] (VCC = 12 V, $I_{REF}$ = 150 µA, $T_A$ = 0°C to 70°C, unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FEEDBACK INPUT | | | | | | |
| Accuracy | $V_{FB}$ | | | | | |
| 1.3 V Output | | TPC 1 | 1.290 | 1.3 | 1.310 | V |
| 1.6 V Output | | TPC 1 | 1.587 | 1.6 | 1.613 | V |
| 2.05 V Output | | TPC 1 | 2.034 | 2.05 | 2.066 | V |
| Line Regulation | $\Delta V_{FB}$ | VCC = 10 V to 14 V | | 0.05 | | % |
| Input Bias Current | $I_{FB}$ | | | 5 | 50 | nA |
| Crowbar Trip Point | $V_{CROWBAR}$ | Percent of Nominal Output | 114 | 124 | 134 | % |
| Crowbar Reset Point | | Percent of Nominal Output | 50 | 60 | 70 | % |
| Crowbar Response Time | $t_{CROWBAR}$ | Overvoltage to PWM Going Low | | 300 | | ns |
| FB Low Comparator Threshold | $V_{FB(LOW)}$ | | 375 | 425 | 500 | mV |
| REFERENCE | | | | | | |
| Output Voltage | $V_{REF}$ | | 2.952 | 3.0 | 3.048 | V |
| Output Current | $I_{REF}$ | | 300 | | | µA |
| VID INPUTS | | | | | | |
| Input Low Voltage | $V_{IL(VID)}$ | | | | 0.6 | V |
| Input High Voltage | $V_{IH(VID)}$ | | 2.2 | | | V |
| Input Current | $I_{VID}$ | VID(X) = 0 V | | 180 | 250 | µA |
| Pull-Up Resistance | $R_{VID}$ | | 20 | 28 | | kΩ |
| Internal Pull-Up Voltage | | | 4.5 | 5.0 | 5.5 | V |
| OSCILLATOR | | | | | | |
| Maximum Frequency[2] | $f_{CT(MAX)}$ | | 2000 | | | kHz |
| Frequency Variation | $\Delta f_{CT}$ | $T_A$ = 25°C, CT = 91 pF | 430 | 500 | 570 | kHz |
| CT Charge Current | $I_{CT}$ | $T_A$ = 25°C, $V_{FB}$ in Regulation | 130 | 150 | 170 | µA |
| | | $T_A$ = 25°C, $V_{FB}$ = 0 V | 26 | 36 | 46 | µA |
| ERROR AMPLIFIER | | | | | | |
| Output Resistance | $R_{O(ERR)}$ | | | 200 | | kΩ |
| Transconductance | $g_{m(ERR)}$ | | 2.0 | 2.2 | 2.45 | mmho |
| Output Current | $I_{O(ERR)}$ | $V_{FB}$ = 0 V | | 1 | | mA |
| Maximum Output Voltage | $V_{COMP(MAX)}$ | FB Forced to $V_{OUT}$ – 3% | | 3.0 | | V |
| Output Disable Threshold | $V_{COMP(OFF)}$ | | 560 | 720 | 800 | mV |
| –3 dB Bandwidth | $BW_{ERR}$ | COMP = Open | | 500 | | kHz |
| CURRENT SENSE | | | | | | |
| Threshold Voltage | $V_{CS(TH)}$ | CS+ = VCC, FB Forced to $V_{OUT}$ – 3% | 69 | 79 | 89 | mV |
| | | 0.8 V ≤ COMP ≤ 1 V | | 0 | 15 | mV |
| | $V_{CS(FOLD)}$ | FB ≤ 375 mV | 37 | 47 | 58 | mV |
| $\Delta V_{COMP}/\Delta V_{CS}$ | $n_i$ | 1 V ≤ $V_{COMP}$ ≤ 3 V | | 25 | | V/V |
| Input Bias Current | $I_{CS+}$, $I_{CS-}$ | CS+ = CS– = VCC | | 0.5 | 5 | µA |
| Response Time | $t_{CS}$ | CS+ – (CS–) ≥ 89 mV to PWM Going Low | | 50 | | ns |
| POWER GOOD COMPARATOR | | | | | | |
| Undervoltage Threshold | $V_{PWRGD(UV)}$ | Percent of Nominal Output | 76 | 82 | 88 | % |
| Overvoltage Threshold | $V_{PWRGD(OV)}$ | Percent of Nominal Output | 114 | 124 | 134 | % |
| Output Voltage Low | $V_{OL(PWRGD)}$ | $I_{PWRGD(SINK)}$ = 100 µA | | 30 | 200 | mV |
| Response Time | | FB Going High | | 2 | | µs |
| | | FB Going Low | | 200 | | ns |
| PWM OUTPUTS | | | | | | |
| Output Voltage Low | $V_{OL(PWM)}$ | $I_{PWM(SINK)}$ = 400 µA | | 100 | 500 | mV |
| Output Voltage High | $V_{OH(PWM)}$ | $I_{PWM(SOURCE)}$ = 400 µA | 4.5 | 5.0 | 5.5 | V |
| Output Current | $I_{PWM}$ | | 0.4 | 1 | | mA |
| Duty Cycle Limit[2] | DC | Per Phase, Relative to $f_{CT}$ | | | 50 | % |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SUPPLY | | | | | | |
| DC Supply Current | | | | | | |
| Normal Mode | $I_{CC}$ | | | 3.8 | 5.5 | mA |
| UVLO Mode | $I_{CC(UVLO)}$ | VCC ≤ $V_{UVLO}$, VCC Rising | | 220 | 400 | µA |
| UVLO Threshold Voltage | $V_{UVLO}$ | | 5.9 | 6.4 | 6.9 | V |
| UVLO Hysteresis | | | 0.1 | 0.4 | 0.6 | V |

NOTES
[1]All limits at temperature extremes are guaranteed via correlation using standard Statistical Quality Control (SQC) methods.
[2]Guaranteed by design, not tested in production.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS***

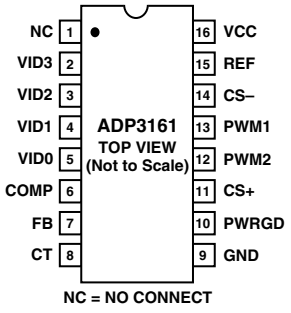
VCC . . . . . –0.3 V to +15 V
CS+, CS– . . . . . –0.3 V to VCC + 0.3 V
All Other Inputs and Outputs . . . . . –0.3 V to +10 V
Operating Ambient Temperature Range . . . . . 0°C to 70°C
Operating Junction Temperature . . . . . 125°C
Storage Temperature Range . . . . . –65°C to +150°C
$\theta_{JA}$
Two-Layer Board . . . . . 125°C/W
Four-Layer Board . . . . . 81°C/W
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Vapor Phase (60 sec) . . . . . 215°C
Infrared (15 sec) . . . . . 220°C

*This is a stress rating only; operation beyond these limits can cause the device to be permanently damaged. Unless otherwise specified, all voltages are referenced to GND.

**ORDERING GUIDE**

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADP3161JR | 0°C to 70°C | Narrow Body SOIC | R-16A (SO-16) |

**PIN CONFIGURATION**
**R-16A**



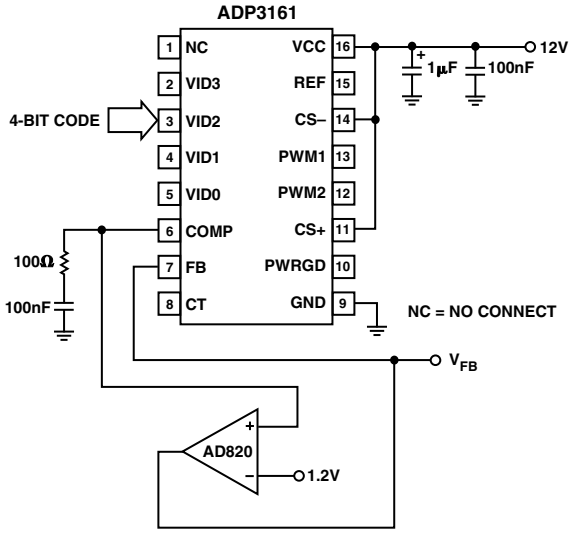

**PIN FUNCTION DESCRIPTIONS**

| Pin No. | Name | Function |
|---|---|---|
| 1 | NC | No Connect. |
| 2–5 | VID3–VID0 | Voltage Identification DAC Inputs. These pins are pulled up to an internal reference, providing a Logic 1 if left open. The DAC output programs the FB regulation voltage from 1.3 V to 2.05 V. |
| 6 | COMP | Error Amplifier Output and Compensation Point. The voltage at this output programs the output current control level between CS+ and CS–. |
| 7 | FB | Feedback Input. Error amplifier input for remote sensing of the output voltage. |
| 8 | CT | External capacitor CT connection to ground sets the frequency of the device. |
| 9 | GND | Ground. All internal signals of the ADP3161 are referenced to this ground. |
| 10 | PWRGD | Open drain output that signals when the output voltage is in the proper operating range. |
| 11 | CS+ | Current Sense Positive Node. Positive input for the current comparator. The output current is sensed as a voltage at this pin with respect to CS–. |
| 12 | PWM2 | Logic-level output for the phase 2 driver. |
| 13 | PWM1 | Logic-level output for the phase 1 driver. |
| 14 | CS– | Current Sense Negative Node. Negative input for the current comparator. |
| 15 | REF | 3.0 V Reference Output. |
| 16 | VCC | Supply Voltage for the ADP3161. |

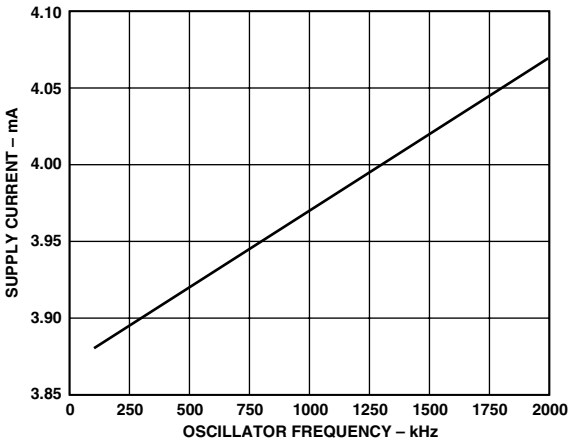
**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADP3161 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

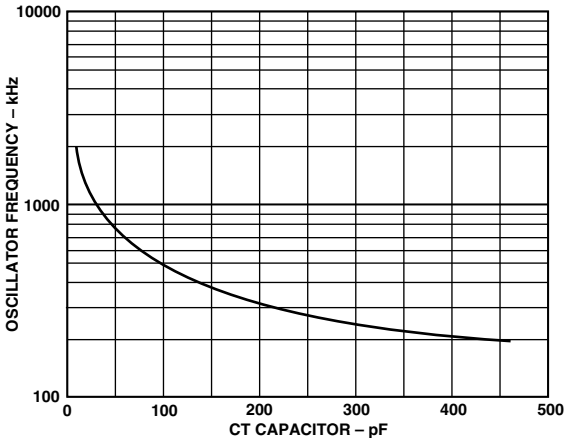
# ADP3161–Typical Performance Characteristics



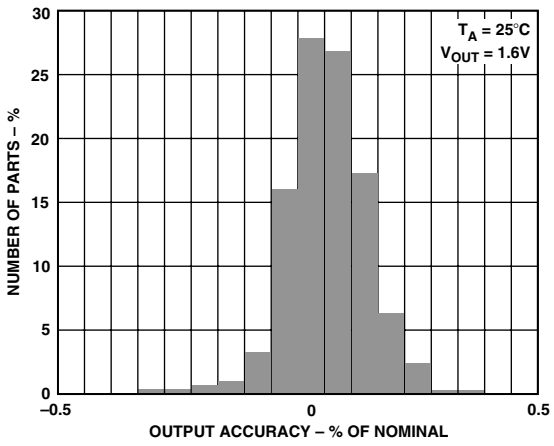

*TPC 1. Closed-Loop Output Voltage Accuracy Test Circuit*



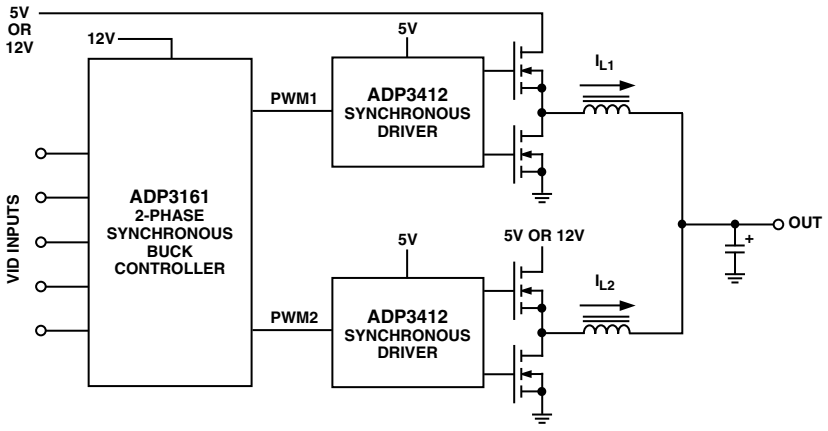

*TPC 3. Supply Current vs. Oscillator Frequency*

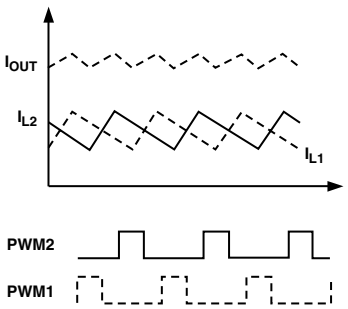



*TPC 2. Oscillator Frequency vs. Timing Capacitor*




*TPC 4. Output Accuracy Distribution*




*TPC 5. 2-Phase CPU Supply System Level Block Diagram*

**Table I. Output Voltage vs. VID Code**

| VID3 | VID2 | VID1 | VID0 | $V_{OUT(NOM)}$ |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | 1.30 V |
| 1 | 1 | 1 | 0 | 1.35 V |
| 1 | 1 | 0 | 1 | 1.40 V |
| 1 | 1 | 0 | 0 | 1.45 V |
| 1 | 0 | 1 | 1 | 1.50 V |
| 1 | 0 | 1 | 0 | 1.55 V |
| 1 | 0 | 0 | 1 | 1.60 V |
| 1 | 0 | 0 | 0 | 1.65 V |
| 0 | 1 | 1 | 1 | 1.70 V |
| 0 | 1 | 1 | 0 | 1.75 V |
| 0 | 1 | 0 | 1 | 1.80 V |
| 0 | 1 | 0 | 0 | 1.85 V |
| 0 | 0 | 1 | 1 | 1.90 V |
| 0 | 0 | 1 | 0 | 1.95 V |
| 0 | 0 | 0 | 1 | 2.00 V |
| 0 | 0 | 0 | 0 | 2.05 V |

## THEORY OF OPERATION

The ADP3161 combines a current-mode, fixed frequency PWM controller with antiphase logic outputs in a controller for a two-phase synchronous buck power converter. Two-phase operation is important for switching the high currents required by high performance microprocessors. Handling the high current in a single-phase converter would place difficult requirements on the power components such as inductor wire size, MOSFET ON-resistance, and thermal dissipation. The ADP3161's high-side current sensing topology ensures that the load currents are balanced in each phase, such that neither phase has to carry more than half of the power. An additional benefit of high-side current sensing over output current sensing is that the average current through the sense resistor is reduced by the duty cycle of the converter, allowing the use of a lower power, lower cost resistor. The outputs of the ADP3161 are logic drivers only and are not intended to directly drive external power MOSFETs. Instead, the ADP3161 should be paired with drivers such as the ADP3412, ADP3413, or ADP3414. A system level block diagram of a 2-phase power supply for high current CPUs is shown in TPC 5.

The frequency of the ADP3161 is set by an external capacitor connected to the CT pin. Each output phase of the ADP3161 operates at half of the frequency set by the CT pin. The error amplifier and current sense comparator control the duty cycle of the PWM outputs to maintain regulation. The maximum duty cycle per phase is inherently limited to 50% because the PWM outputs toggle in two-phase operation. While one phase is on, the other phase is off. In no case can both outputs be high at the same time.

### Output Voltage Sensing

The output voltage is sensed at the FB pin allowing for remote sensing. To maintain the accuracy of the remote sensing, the GND pin should also be connected close to the load. A voltage error amplifier ($g_m$) amplifies the difference between the output voltage and a programmable reference voltage. The reference voltage is programmed between 1.3 V and 2.05 V by an internal 5-bit DAC, which reads the code at the voltage identification (VID) pins. (Refer to Table I for the output voltage versus VID pin code information.)

### Active Voltage Positioning

The ADP3161 uses Analog Devices Optimal Positioning Technology (ADOPT), a unique supplemental regulation technique that uses active voltage positioning and provides optimal compensation for load transients. When implemented, ADOPT adjusts the output voltage as a function of the load current, so that it is always optimally positioned for a load transient. Standard (passive) voltage positioning has poor dynamic performance, rendering it ineffective under the stringent repetitive transient conditions required by high performance processors. ADOPT, however, provides optimal bandwidth for transient response that yields optimal load transient response with the minimum number of output capacitors.

### Reference Output

A 3.0 V reference is available on the ADP3161. This reference is normally used to set the voltage positioning accurately using a resistor divider to the COMP pin. In addition, the reference can be used for other functions such as generating a regulated voltage with an external amplifier. The reference is bypassed with a 1 nF capacitor to ground. It is not intended to supply current to large capacitive loads, and it should not be used to provide more than 1 mA of output current.

### Cycle-by-Cycle Operation

During normal operation (when the output voltage is regulated), the voltage-error amplifier and the current comparator are the main control elements. The voltage at the CT pin of the oscillator ramps between 0 V and 3 V. When that voltage reaches 3 V, the oscillator sets the driver logic, which sets PWM1 high. During the ON time of Phase 1, the driver IC turns on the high-side MOSFET. The CS+ and CS– pins monitor the current through the sense resistor that feeds both high-side MOSFETs. When the voltage between the two pins exceeds the threshold level set by the voltage error amplifier ($g_m$), the driver logic is reset and the PWM output goes low. This signals the driver IC to turn off the high-side MOSFET and turn on the low-side MOSFET. On the next cycle of the oscillator, the driver logic toggles and sets PWM2 high. On each following cycle of the oscillator, the outputs toggle between PWM1 and PWM2. In each case, the current comparator resets the PWM output low when the current comparator threshold is reached. As the load current increases, the output voltage starts to decrease. This causes an increase in the output of the $g_m$ amplifier, which in turn leads to an increase in the current comparator threshold, thus programming more current to be delivered to the output so that voltage regulation is maintained.

### Active Current Sharing

The ADP3161 ensures current balance in the two phases by actively sensing the current through a single sense resistor. During one phase's ON time, the current through the respective high-side MOSFET and inductor is measured through the sense resistor (R4 in TPC 6). When the comparator (CMP1 in the Functional Block Diagram) threshold programmed by the $g_m$ amplifier is reached, the high-side MOSFET turns off. In the next cycle the ADP3161 switches to the second phase. The current is measured with the same sense resistor and the same internal comparator, ensuring accurate matching. This scheme is immune to imbalances in the MOSFETs' $R_{DS(ON)}$ and inductors' parasitic resistances.

If for some reason one of the phases fails, the other phase will still be limited to its maximum output current (one-half of the short circuit current limit). If this is not sufficient to supply the load,

the output voltage will droop and cause the PWRGD output to signal that the output voltage has fallen out of its specified range.

**Short Circuit Protection**

The ADP3161 has multiple levels of short circuit protection to ensure fail-safe operation. The sense resistor and the maximum current sense threshold voltage given in the specifications set the peak current limit.

When the load current exceeds the current limit, the excess current discharges the output capacitor. When the output voltage is below the foldback threshold $V_{FB(LOW)}$, the maximum deliverable output current is cut by reducing the current sense threshold from the current limit threshold, $V_{CS(CL)}$, to the foldback threshold, $V_{CS(FOLD)}$. Along with the resulting current foldback, the oscillator frequency is reduced by a factor of five when the output is 0 V. This further reduces the average current in short circuit.

**Power-Good Monitoring**

The Power-Good comparator monitors the output voltage of the supply via the FB pin. The PWRGD pin is an open drain output whose high level (when connected to a pull-up resistor) indicates that the output voltage is within the specified range of the nominal output voltage requested by the VID DAC. PWRGD will go low if the output is outside this range.

**Output Crowbar**

The ADP3161 includes a crowbar comparator that senses when the output voltage rises higher than the specified trip threshold, $V_{CROWBAR}$. This comparator overrides the control loop and sets both PWM outputs low. The driver ICs turn off the high side MOSFETs and turn on the low-side MOSFETs, thus pulling the output down as the reversed current builds up in the inductors. If the output overvoltage is due to a short of the high side MOSFET, this action will current limit the input supply or blow its fuse, protecting the microprocessor from destruction. The crowbar comparator releases when the output drops below the specified reset threshold, and the controller returns to normal operation if the cause of the overvoltage failure does not persist.

**Output Disable**

The ADP3161 includes an output disable function that turns off the control loop to bring the output voltage to 0 V. Because an extra pin is not available, the disable feature is accomplished by pulling the COMP pin to ground. When the COMP pin drops below 0.56 V, the oscillator stops and both PWM signals are driven low. This function does not place the part in a low quiescent current shutdown state, and the reference voltage is still available. The COMP pin should be pulled down with an open collector or open drain type of output capable of sinking at least 2 mA.

## APPLICATION INFORMATION

**A VRM 8.4–Compliant Design Example**

The design parameters for a typical high-performance Intel Pentium III CPU application designed to meet Intel's VRM 8.4 FMB specification (see Figure 1) are as follows:

Input Voltage ($V_{IN}$) = 5 V

Nominal Output Voltage ($V_{OUT}$) = 1.8 V

Static Output Voltage Tolerance ($V_{\Delta}$) = (V+) – (V–) = 40 mV – (–80 mV) = 120 mV

Average Output Voltage ($V_{AVG}$) = $V_{OUT} + \frac{(V+)+(V-)}{2}$ = 1.780 $V$

Maximum Output Current ($I_O$) = 26 A

Output Current di/dt < 20 A/µs.

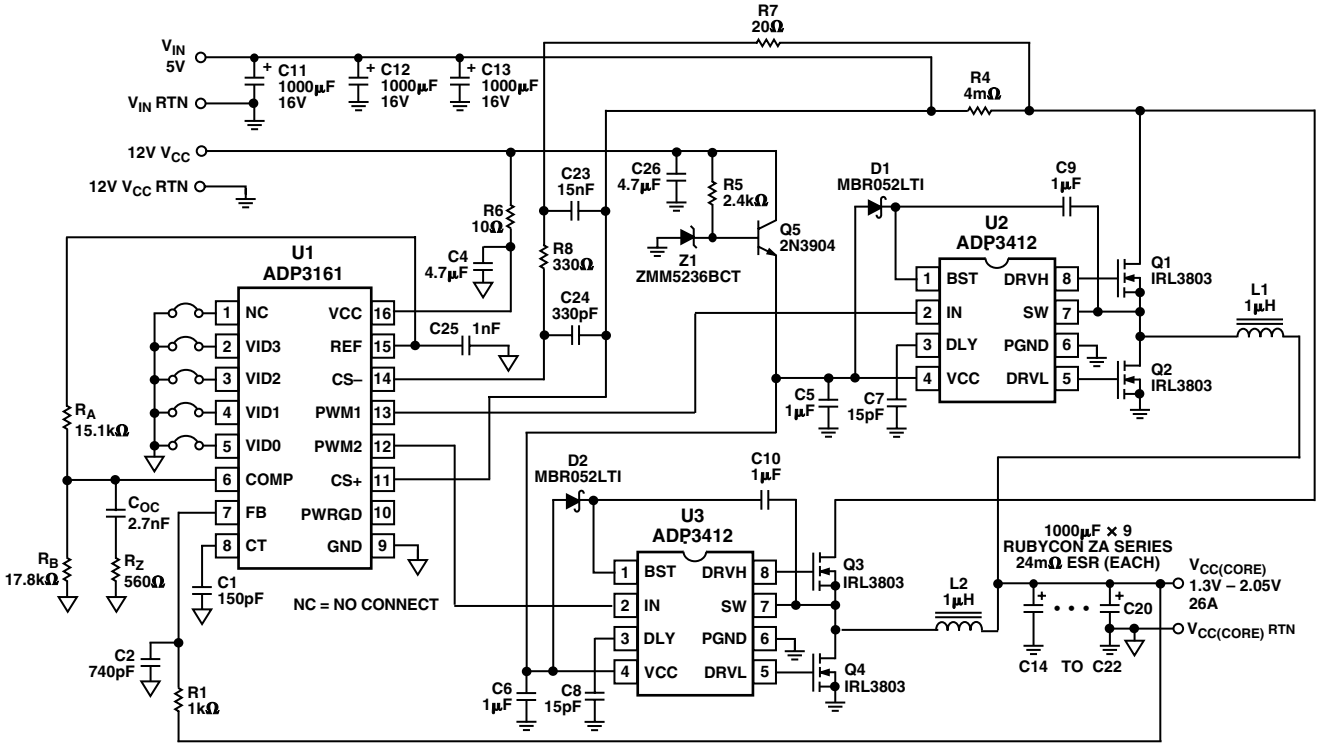



*Figure 1. 26 A Pentium III CPU Supply Circuit*

**$C_T$ Selection—Choosing the Clock Frequency**

The ADP3161 uses a fixed-frequency control architecture. The frequency is set by an external timing capacitor, $C_T$. The value of $C_T$ for a given clock frequency can be selected using the graph in TPC 2.

The clock frequency determines the switching frequency, which relates directly to switching losses and the sizes of the inductors and input and output capacitors. A clock frequency of 400 kHz sets the switching frequency of each phase, $f_{SW}$, to 200 kHz, which represents a practical trade-off between the switching losses and the sizes of the output filter components. From TPC 2, for 400 kHz the required timing capacitor value is 150 pF. For good frequency stability and initial accuracy, it is recommended to use a capacitor with low temperature coefficient and tight tolerance, e.g., an MLC capacitor with NPO dielectric and with 5% or less tolerance.

**Inductance Selection**

The choice of inductance determines the ripple current in the inductor. Less inductance leads to more ripple current, which increases the output ripple voltage and the conduction losses in the MOSFETs, but allows using smaller-size inductors and, for a specified peak-to-peak transient deviation, output capacitors with less total capacitance. Conversely, a higher inductance means lower ripple current and reduced conduction losses, but requires larger-size inductors and more output capacitance for the same peak-to-peak transient deviation. In a two-phase converter a practical value for the peak-to-peak inductor ripple current is under 50% of the dc current in the same inductor. A choice of 46% for this particular design example yields a total peak-to-peak output ripple current of 23% of the total dc output current. The following equation shows the relationship between the inductance, oscillator frequency, peak-to-peak ripple current in an inductor and input and output voltages.

$$L = \frac{(V_{IN} - V_{AVG}) \times V_{AVG}}{V_{IN} \times f_{SW} \times I_{L(RIPPLE)}} \quad (1)$$

For 6 A peak-to-peak ripple current, which corresponds to just under 50% of the 13 A full-load dc current in an inductor, Equation 1 yields an inductance of

$$L = \frac{(5V - 1.780V) \times 1.780V}{5V \times 400\,kHz/2 \times 6\,A} = 955\,nH$$

A 1 µH inductor can be used, which gives a calculated ripple current of 5.7 A at no load. The inductor should not saturate at the peak current of 18.7 A and should be able to handle the sum of the power dissipation caused by the average current of 15 A in the winding and the core loss.

The output ripple current is smaller than the inductor ripple current due to the two phases partially canceling. This can be calculated as follows:

$$I_{O\Delta} = \frac{2 \times V_{AVG}\,(V_{IN} - 2 \times V_{AVG})}{V_{IN} \times L \times f_{OSC}} = \frac{2 \times 1.780V \times (5V - 2 \times 1.780V)}{5V \times 1\,\mu H \times 400\,kHz} = 2.6\,A \quad (2)$$

**Designing an Inductor**

Once the inductance is known, the next step is either to design an inductor or find a standard inductor that comes as close as possible to meeting the overall design goals. The first decision in designing the inductor is to choose the core material. There are several possibilities for providing low core loss at high frequencies. Two examples are the powder cores (e.g., Kool-Mµ® from Magnetics) and the gapped soft ferrite cores (e.g., 3F3 or 3F4 from Philips). Low frequency powdered iron cores should be avoided due to their high core loss, especially when the inductor value is relatively low and the ripple current is high.

Two main core types can be used in this application. Open magnetic loop types, such as beads, beads on leads, and rods and slugs, provide lower cost but do not have a focused magnetic field in the core. The radiated EMI from the distributed magnetic field may create problems with noise interference in the circuitry surrounding the inductor. Closed-loop types, such as pot cores, PQ, U, and E cores, or toroids, cost more, but have much better EMI/RFI performance. A good compromise between price and performance are cores with a toroidal shape.

There are many useful references for quickly designing a power inductor. Table II gives some examples.

**Table II. Magnetics Design References**

| |
|---|
| Magnetic Designer Software<br>Intusoft (http://www.intusoft.com) |
| Designing Magnetic Components for High-Frequency DC-DC Converters<br>McLyman, Kg Magnetics<br>ISBN 1-883107-00-08 |

**Selecting a Standard Inductor**

The companies listed in Table III can provide design consultation and deliver power inductors optimized for high power applications upon request.

**Table III. Power Inductor Manufacturers**

| |
|---|
| Coilcraft<br>(847) 639-6400<br>http://www.coilcraft.com |
| Coiltronics<br>(561) 752-5000<br>http://www.coiltronics.com |
| Sumida Electric Company<br>(408) 982-9660<br>http://www.sumida.com |

**$C_{OUT}$ Selection—Determining the ESR**

The required equivalent series resistance (ESR) and capacitance drive the selection of the type and quantity of the output capacitors. The ESR must be small enough to contain the voltage deviation caused by a maximum allowable CPU transient current within the specified voltage limits, giving consideration also to the output ripple and the regulation tolerance. The capacitance must be large enough that the voltage across the capacitor, which is the sum of the resistive and capacitive voltage deviations, does not deviate beyond the initial resistive deviation while the inductor current ramps up or down to the value corresponding to the new load current. The maximum allowed ESR also represents the maximum allowed output resistance, $R_{OUT}$.

The cumulative errors in the output voltage regulations cut into the available regulation window, $V_{WIN}$. When considering dynamic load regulation this relates directly to the ESR. When considering dc load regulation, this relates directly to the programmed output resistance of the power converter.

Some error sources, such as initial voltage accuracy and ripple voltage, can be directly deducted from the available regulation window, while other error sources scale proportionally to the amount of voltage positioning used, which, for an optimal design, should utilize the maximum that the regulation window will allow. The error determination is a closed-loop calculation, but it can be closely approximated. To maintain a conservative design while avoiding an impractical design, various error sources should be considered and summed statistically.

The output ripple voltage can be factored into the calculation by summing the output ripple current with the maximum output current to determine an effective maximum dynamic current change. The remaining errors are summed separately according to the formula:

$$V_{WIN} = (V_{\Delta} - (V_{VID} \times 2\,k_{VID})) \times \left(1 - \frac{I_O}{I_O + I_{O\Delta}} \sqrt{k_{RCS}{}^2 + \left(\frac{k_{CSF}}{2}\right)^2 + k_{RT}{}^2 + k_{EA}{}^2}\right) = 83.5\,mV \quad (3)$$

where $k_{VID}$ = 0.7% is the initial programmed voltage tolerance from the graph of TPC 4, $k_{RCS}$ = 2% is the tolerance of the current sense resistor, $k_{CSF}$ = 20% is the summed tolerance of the current sense filter components, $k_{RT}$ = 2% is the tolerance of the two termination resistors added at the COMP pin, and $k_{EA}$ = 8% accounts for the IC current loop gain tolerance including the $g_m$ tolerance.

The remaining window is then divided by the maximum output current plus the ripple to determine the maximum allowed ESR and output resistance:

$$R_{E(MAX)} = R_{OUT(MAX)} = \frac{V_{WIN}}{I_O + I_{O\Delta}} = \frac{83.5\,mV}{26\,A + 2.6\,A} = 2.9\,m\Omega \quad (4)$$

The output filter capacitor bank must have an ESR of less than 2.9 mΩ. One can, for example, use four SP-Type OS-CON capacitors from Sanyo, with 1.2 mF capacitance, a 2.5 V voltage rating, and 11 mΩ ESR. The four capacitors have a maximum total ESR of 2.75 mΩ when connected in parallel. Another possibility is the ZA series from Rubycon. The trade-off is size versus cost. Nine 1 mF capacitors would give an ESR of 2.67 mΩ. These capacitors take up more space than four OS-CON capacitors, but are significantly less expensive.

**$C_{OUT}$—Checking the Capacitance**

As long as the capacitance of the output capacitor is above a critical value and the regulating loop is compensated with ADOPT, the actual value has no influence on the peak-to-peak deviation of the output voltage to a full step change in the load current. The critical capacitance can be calculated as follows:

$$C_{OUT(CRIT)} = \frac{I_O}{R_E \times V_{OUT}} \times \frac{L}{2} = \frac{26\,A}{2.75\,m\Omega \times 1.8} \times \frac{1\,\mu H}{2} = 2.6\,mF \quad (5)$$

The critical capacitance for the four OS-CON capacitors with an equivalent ESR of 2.75 mΩ is 2.6 mF, while the equivalent capacitance of those capacitors is 4.8 mF. The critical capacitance for the nine ZA series Rubycon capacitors is 2.8 mF while the equivalent capacitance is 9 mF. With both choices, the capacitance is safely above the critical value.

**$R_{SENSE}$**

The value of $R_{SENSE}$ is based on the maximum required output current. The current comparator of the ADP3161 has a minimum current limit threshold of 69 mV. Note that the 69 mV value cannot be used for the maximum specified nominal current, as headroom is needed for ripple current and tolerances.

The current comparator threshold sets the peak of the inductor current yielding a maximum output current, $I_O$, which equals twice the peak inductor current value less half of the peak-to-peak inductor ripple current. From this the maximum value of $R_{SENSE}$ is calculated as:

$$R_{SENSE} \le \frac{V_{CS(CL)(MIN)}}{\frac{I_O}{2} + \frac{I_{L(RIPPLE)}}{2}} = \frac{69\,mV}{13\,A + 2.85\,A} = 4.4\,m\Omega \quad (6)$$

In this case, 4 mΩ was chosen as the closest standard value.

Once $R_{SENSE}$ has been chosen, the output current at the point where current limit is reached, $I_{OUT(CL)}$, can be calculated using the maximum current sense threshold of 89 mV:

$$I_{OUT(CL)} = 2 \times \frac{V_{CS(CL)(MAX)}}{R_{SENSE}} - I_{L(RIPPLE)} = 2 \times \frac{89\,mV}{4\,m\Omega} - 5.7\,A = 38.8\,A \quad (7)$$

At output voltages below 425 mV, the current sense threshold is reduced to 58 mV, and the ripple current is negligible. Therefore, at dead short the output current is reduced to:

$$I_{OUT(SC)} = 2 \times \frac{58\,mV}{4\,mV} = 29.0\,A \quad (8)$$

To safely carry the current under maximum load conditions, the sense resistor must have a power rating of at least:

$$P_{R_{SENSE}} = I_{SENSE(RMS)}{}^2 \times R_{SENSE} \quad (9)$$

where:

$$I_{SENSE(RMS)}{}^2 = \frac{I_O{}^2}{n} \times \frac{V_{OUT}}{\eta \times V_{IN}} \quad (10)$$

In this formula, $n$ is the number of phases, and η is the converter efficiency, in this case assumed to be 85%. Combining Equations 9 and 10 yields:

$$P_{R_{SENSE}} = \frac{26A^2}{2} \times \frac{1.8\,V}{0.85 \times 5\,V} = 573\,mW$$

**Power MOSFETs**

In the standard two-phase application, two pairs of N-channel power MOSFETs must be used with the ADP3161 and ADP3412, one pair as the main (control) switches, and the other pair as the synchronous rectifier switches. The main selection parameters

for the power MOSFETs are $V_{GS(TH)}$ and $R_{DS(ON)}$. The minimum gate drive voltage (the supply voltage to the ADP3412) dictates whether standard threshold or logic-level threshold MOSFETs must be used. Since $V_{GATE}$ < 8 V, logic-level threshold MOSFETs ($V_{GS(TH)}$ < 2.5 V) are strongly recommended.

The maximum output current $I_O$ determines the $R_{DS(ON)}$ requirement for the power MOSFETs. When the ADP3161 is operating in continuous mode, the simplifying assumption can be made that in each phase one of the two MOSFETs is always conducting the average inductor current. For $V_{IN}$ = 5 V and $V_{OUT}$ = 1.8 V, the duty ratio of the high-side MOSFET is:

$$D_{HSF} = \frac{V_{OUT}}{V_{IN}} = 36\% \quad (11)$$

The duty ratio of the low-side (synchronous rectifier) MOSFET is:

$$D_{LSF} = 1 - D_{HSF} = 64\% \quad (12)$$

The maximum rms current of the high-side MOSFET during normal operation is:

$$I_{HSF(MAX)} = \frac{I_O}{2}\sqrt{D_{HSF} \times \left(1 + \frac{I^2{}_{L(RIPPLE)}}{3 \times I_O{}^2}\right)} = 7.9\ A \quad (13)$$

The maximum rms current of the low-side MOSFET during normal operation is:

$$I_{LSF(MAX)} = I_{HSF(MAX)}\sqrt{\frac{D_{LSF}}{D_{HSF}}} = 10.5\ A \quad (14)$$

The $R_{DS(ON)}$ for each MOSFET can be derived from the allowable dissipation. If 10% of the maximum output power is allowed for MOSFET dissipation, the total dissipation in the four MOSFETs of the two-phase converter will be:

$$P_{MOSFET(TOTAL)} = 0.1 \times V_{OUT} \times I_O = 0.1 \times 1.8\ V \times 26\ A = 4.7\ W \quad (15)$$

Allocating half of the total dissipation for the pair of high-side MOSFETs and half for the pair of low-side MOSFETs, and assuming that the resistive and switching losses of the high-side MOSFET are equal, the required maximum MOSFET resistances will be:

$$R_{DS(ON)HS(MAX)} = \frac{P_{MOSFET(TOTAL)}}{8 \times I^2{}_{HSF(MAX)}} = \frac{4.7\ W}{8 \times (7.9\ A)^2} = 9.4\ m\Omega \quad (16)$$

$$R_{DS(ON)LS(MAX)} = \frac{P_{MOSFET(TOTAL)}}{4 \times I^2{}_{LSF(MAX)}} = \frac{4.7\ W}{4 \times (10.5\ A)^2} = 10.6\ m\Omega \quad (17)$$

An IRL3803 MOSFET from International Rectifier ($R_{DS(ON)}$ = 6 mΩ nominal, 9 mΩ worst case) is a good choice for both the high-side and low-side. The high-side MOSFET dissipation is:

$$P_{HSF} = \left(R_{DS(ON)HS} \times I^2{}_{HFS(MAX)}\right) + \frac{V_{IN} \times I_{L(PK)} \times Q_G \times f_{SW}}{2 \times I_G} + \left(V_{IN} \times Q_{RR} \times f_{SW}\right) \quad (18)$$

where the second term represents the turn-off loss of the MOSFET and the third term represents the turn-on loss due to the stored charge in the body diode of the low-side MOSFET. (In the second term, $Q_G$ is the gate charge to be removed from the gate for turn-off and $I_G$ is the gate turn-off current. From the data sheet, for the IRL3803 the value of $Q_G$ is about 140 nC and the peak gate drive current provided by the ADP3412 is about 1 A. In the third term, $Q_{RR}$ is the charge stored in the body diode of the low-side MOSFET at the valley of the inductor current. The data sheet of the IRL3803 gives 450 nC for the stored charge at 71 A. That value corresponds to a stored charge of 80 nC at the valley of the inductor current. In both terms $f_{SW}$ is the actual switching frequency of the MOSFETs, or 200 kHz. $I_{L(PK)}$ is the peak current in the inductor, or 15.85 A.)

Substituting the above data in Equation 18, and using the worst-case value for the MOSFET resistance, yields a conduction loss of 0.56 W, a turn-off loss of 1.1 W, and a turn-on loss of 0.08 W. Thus the worst-case total loss in a high-side MOSFET is 1.74 W.

The worst-case low-side MOSFET dissipation is:

$$P_{LSF} = R_{DS(ON)LS} \times I^2{}_{LSF(MAX)} = 9\ m\Omega \times (10.5\ A)^2 = 1\ W \quad (19)$$

(Note that there are no switching losses in the low-side MOSFET.)

**$C_{IN}$ Selection and Input Current di/dt Reduction**

In continuous inductor-current mode, the source current of the high-side MOSFET is approximately a square wave with a duty ratio equal to $V_{OUT}/V_{IN}$ and an amplitude of one-half of the maximum output current. To prevent large voltage transients, a low ESR input capacitor sized for the maximum rms current must be used. The maximum rms capacitor current is given by:

$$I_{C(RMS)} = \frac{I_O}{2}\sqrt{2 \times D_{HSF} - (2 \times D_{HSF})^2} = \frac{26\ A}{2}\sqrt{2 \times 0.36 - (2 \times 0.36)^2} = 5.8\ A \quad (20)$$

Note that the capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be placed in parallel to meet size or height requirements in the design. In this example, the input capacitor bank is formed by three 1000 µF, 16 V Rubycon capacitors.

The ripple voltage across the three paralleled capacitors is:

$$V_{C(RIPPLE)} = \frac{I_O}{n} \times \left(\frac{ESR_C}{n_C} + \frac{D_{HSF}}{n_C \times C_{IN} \times f_{SW}}\right) = \frac{26\ A}{2} \times \left(\frac{24\ m\Omega}{3} + \frac{0.36}{3 \times 1000\ \mu F \times 200\ kHz}\right) = 112\ mV \quad (21)$$

To reduce the input-current di/dt to below the recommended maximum of 0.1 A/µs, an additional small inductor (L > 1 µH @ 15 A) should be inserted between the converter and the supply bus. That inductor also acts as a filter between the converter and the primary power source.

**Feedback Loop Compensation Design for ADOPT**

Optimized compensation of the ADP3161 allows the best possible containment of the peak-to-peak output voltage deviation. Any practical switching power converter is inherently limited by the inductor in its output current slew rate to a value much less than the slew rate of the load. Therefore, any sudden change of load current will initially flow through the output capacitors, and assuming that the capacitance of the output capacitor is larger than the critical value defined by Equation 5, this will produce a peak output voltage deviation equal to the ESR of the output capacitor times the load current change.

The optimal implementation of voltage positioning, ADOPT, will create an output impedance of the power converter that is entirely resistive over the widest possible frequency range, including dc, and equal to the maximum acceptable ESR of the output capacitor array. With the resistive output impedance, the output voltage will droop in proportion with the load current at any load current slew rate; this ensures the optimal positioning and allows the minimization of the output capacitor.

With an ideal current-mode-controlled converter, where the average inductor current would respond without delay to the command signal, the resistive output impedance could be achieved by having a single-pole roll-off of the voltage gain of the voltage-error amplifier. The pole frequency must coincide with the ESR zero of the output capacitor. The ADP3161 uses constant frequency current-mode control, which is known to have a nonideal, frequency dependent command signal to inductor current transfer function. The frequency dependence manifests in the form of a pair of complex conjugate poles at one-half of the switching frequency. A purely resistive output impedance could be achieved by canceling the complex conjugate poles with zeros at the same complex frequencies and adding a third pole equal to the ESR zero of the output capacitor. Such a compensating network would be quite complicated. Fortunately, in practice it is sufficient to cancel the pair of complex conjugate poles with a single real zero placed at one-half of the switching frequency. Although the end result is not a perfectly resistive output impedance, the remaining frequency dependence causes only a few percentage of deviation from the ideal resistive response. The single-pole and single-zero compensation can be easily implemented by terminating the $g_m$ error amplifier with the parallel combination of a resistor and a series RC network.

The first step in the design of the feedback loop compensation is to determine the targeted output resistance, $R_{E(MAX)}$ of the power converter using Equation 4. The compensation can then be tailored to create that output impedance for the power converter, and the quantity of output capacitors can be chosen to create a net ESR that is less than or equal to $R_{E(MAX)}$.

The next step is to determine the total termination resistance of the $g_m$ amplifier that will yield the correct output resistance:

$$R_T = \frac{n_I \times R_{SENSE}}{g_m \times R_{E(MAX)} \times 2} = \frac{25 \times 4\ m\Omega}{2.2\ mmho \times 2.9\ m\Omega \times 2} = 7.84\ k\Omega \quad (22)$$

where $n_I$ is the division ratio from the output voltage signal of the $g_m$ amplifier to the PWM comparator (CMP1), $g_m$ is the transconductance of the $g_m$ amplifier itself, and the factor of 2 is the result of the two-phase configuration.

Once $R_T$ is known, the two resistors that make up the divider from the REF pin to output of the $g_m$ amplifier (COMP pin) must be calculated. The resistive divider introduces an offset to the output of the $g_m$ amplifier that, when reflected back through the gain of the $g_m$ stage, accurately positions the output voltage near its allowed maximum at light load. Furthermore, the output of the $g_m$ amplifier sets the current sense threshold voltage. At no load, the current sense threshold is increased by the peak of the ripple current in the inductor and reduced by the delay between sensing when the current threshold has been reached and when the high-side MOSFET actually turns off. These two factors are combined with the inherent voltage at the output of $g_m$ amplifier that commands a current sense threshold of 0 mV ($V_{GNL0}$):

$$\begin{aligned} V_{GNL} &= V_{GNL0} + \frac{I_{L(RIPPLE)} \times R_{CS} \times n_I}{2} - \frac{V_{IN} - V_{AVG}}{L}\left(2 \times t_D \times R_{CS} \times n_I\right) \\ V_{GNL} &= 1\,V + \frac{5.7\,A \times 4\,m\Omega \times 25}{2} \\ &- \frac{5\,V - 1.78\,V}{1\,\mu H} \times 2 \times 60\,ns \times 4\,m\Omega \times 25 = 1.25\,V \end{aligned} \quad (23)$$

The output voltage at no load ($V_{ONL}$) can be calculated by starting with the VID setting, adding in the positive offset (V+), subtracting half the ripple voltage, and then subtracting the dominant error terms:

$$\begin{aligned} V_{ONL} &= V_{VID} + V^+ - \frac{R_E \times \Delta I_O}{2} - V_{VID} \times \sqrt{2\,k_{VID}{}^2 + \left(k_{RT} \times \frac{V_{WIN}}{V_{VID}}\right)^2} \\ V_{ONL} &= 1.8\,V + 40\,mV - \frac{2.9\,m\Omega \times 2.6\,A}{2} \\ &-1.8\,V \times \sqrt{(0.007)^2 + \left(0.02 \times \frac{83.5\,mV}{1.8\,V}\right)^2} = 1.824\,V \end{aligned} \quad (24)$$

With these two terms calculated, the divider resistors ($R_A$ for the upper, and $R_B$ for the lower) can be calculated. Assuming that the internal resistance of the $g_m$ amplifier ($R_{OGM}$) is 200 kΩ:

$$\begin{aligned} R_B &= \frac{V_{REF}}{\frac{V_{REF} - V_{GNL}}{R_T} - g_m(V_{ONL} - V_{VID})} \\ R_B &= \frac{3\,V}{\frac{3\,V - 1.25\,V}{7.84\,k\Omega} - 2.2\,mmho \times (1.824\,V - 1.8\,V)} \\ &= 17.6\,k\Omega \end{aligned} \quad (25)$$

Choosing the nearest 1% resistor value gives $R_B$ = 17.8 kΩ. Finally, $R_A$ is calculated:

$$R_A = \frac{1}{\frac{1}{R_T} - \frac{1}{R_{OGM}} - \frac{1}{R_B}} = \frac{1}{\frac{1}{7.84\,k\Omega} - \frac{1}{200\,k\Omega} - \frac{1}{17.8\,k\Omega}} = 15.1\,k\Omega \quad (26)$$

Again, choosing the nearest 1% resistor value gives $R_A$ = 15.0 kΩ. The compensating capacitor can be calculated from the equation

$$\begin{aligned} C_{OC} &= \frac{C_{OUT} \times R_E}{R_T} - \frac{2}{\pi \times f_{OSC} \times R_T} \\ C_{OC} &= \frac{9\,mF \times 2.67\,m\Omega}{7.84\,k\Omega} - \frac{2}{\pi \times 400\,kHz \times 7.84\,k\Omega} = 2.86\,nF \end{aligned} \quad (27)$$

Choosing the nearest standard value yields 2.7 nF.

The resistance of the zero-setting resistor in series with the compensating capacitor is

$$R_Z = \frac{2}{C_{OC} \times \pi \times f_{OSC}} = \frac{2}{2.7\,nF \times \pi \times 400\,kHz} = 590\,k\Omega \quad (28)$$

The nearest 2.7 standard 5% resistor value is 560 Ω.

## LAYOUT AND COMPONENT PLACEMENT GUIDELINES

The following guidelines are recommended for optimal performance of a switching regulator in a PC system.

### General Recommendations

1. For good results, at least a four-layer PCB is recommended. This should allow the needed versatility for control circuitry interconnections with optimal placement, a signal ground plane, power planes for both power ground and the input power (e.g., 5 V), and wide interconnection traces in the rest of the power delivery current paths. Keep in mind that each square unit of 1 ounce copper trace has a resistance of ~ 0.53 mΩ at room temperature.
2. Whenever high currents must be routed between PCB layers, vias should be used liberally to create several parallel current paths so that the resistance and inductance introduced by these current paths is minimized and the via current rating is not exceeded.
3. If critical signal lines (including the voltage and current sense lines of the ADP3161) must cross through power circuitry, it is best if a signal ground plane can be interposed between those signal lines and the traces of the power circuitry. This serves as a shield to minimize noise injection into the signals at the expense of making signal ground a bit noisier.
4. The power ground plane should not extend under signal components, including the ADP3161 itself. If necessary, follow the preceding guideline to use the signal ground plane as a shield between the power ground plane and the signal circuitry.
5. The GND pin of the ADP3161 should be connected first to the timing capacitor (on the CT pin), and then into the signal ground plane. In cases where no signal ground plane can be used, short interconnections to other signal ground circuitry in the power converter should be used.
6. The output capacitors of the power converter should be connected to the signal ground plane even though power current flows in the ground of these capacitors. For this reason, it is advised to avoid critical ground connections (e.g., the signal circuitry of the power converter) in the signal ground plane between the input and output capacitors. It is also advised to keep the planar interconnection path short (i.e., have input and output capacitors close together).
7. The output capacitors should also be connected as closely as possible to the load (or connector) that receives the power (e.g., a microprocessor core). If the load is distributed, the capacitors should also be distributed, and generally in proportion to where the load tends to be more dynamic.
8. Absolutely avoid crossing any signal lines over the switching power path loop, described below.

### Power Circuitry

9. The switching power path should be routed on the PCB to encompass the smallest possible area in order to minimize radiated switching noise energy (i.e., EMI). Failure to take proper precautions often results in EMI problems for the entire PC system as well as noise-related operational problems in the power converter control circuitry. The switching power path is the loop formed by the current path through the input capacitors, the power MOSFETs, and the power Schottky diode, if used (see next), including all interconnecting PCB traces and planes. The use of short and wide interconnection traces is especially critical in this path for two reasons: it minimizes the inductance in the switching loop, which can cause high-energy ringing, and it accommodates the high current demand with minimal voltage loss.
10. An optional power Schottky diode (3 A–5 A dc rating) from each lower MOSFET's source (anode) to drain (cathode) will help to minimize switching power dissipation in the upper MOSFETs. In the absence of an effective Schottky diode, this dissipation occurs through the following sequence of switching events. The lower MOSFET turns off in advance of the upper MOSFET turning on (necessary to prevent cross-conduction). The circulating current in the power converter, no longer finding a path for current through the channel of the lower MOSFET, draws current through the inherent body diode of the MOSFET. The upper MOSFET turns on, and the reverse recovery characteristic of the lower MOSFET's body diode prevents the drain voltage from being pulled high quickly. The upper MOSFET then conducts very large current while it momentarily has a high voltage forced across it, which translates into added power dissipation in the upper MOSFET. The Schottky diode minimizes this problem by carrying a majority of the circulating current when the lower MOSFET is turned off, and by virtue of its essentially nonexistent reverse recovery time. The Schottky diode has to be connected with very short copper traces to the MOSFET to be effective.
11. A small ferrite bead inductor placed in series with the drain of the lower MOSFET can also help to reduce this previously described source of switching power loss.
12. Whenever a power dissipating component (e.g., a power MOSFET) is soldered to a PCB, the liberal use of vias, both directly on the mounting pad and immediately surrounding it, is recommended. Two important reasons for this are: improved current rating through the vias, and improved thermal performance from vias extended to the opposite side of the PCB where a plane can more readily transfer the heat to the air.
13. The output power path, though not as critical as the switching power path, should also be routed to encompass a small area. The output power path is formed by the current path through the inductor, the current sensing resistor, the output capacitors, and back to the input capacitors.
14. For best EMI containment, the power ground plane should extend fully under all the power components except the output capacitors. These components are: the input capacitors, the power MOSFETs and Schottky diodes, the inductors, the current sense resistor, and any snubbing element that might be added to dampen ringing. Avoid extending the power ground under any other circuitry or signal lines, including the voltage and current sense lines.

**Signal Circuitry**

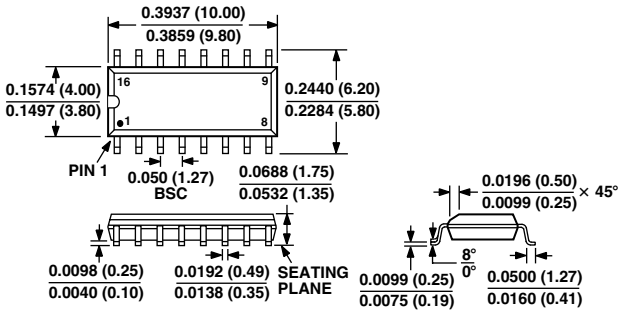
15. The output voltage is sensed and regulated between the FB pin and the GND pin (which connects to the signal ground plane). The output current is sensed (as a voltage) by the CS+ and CS– pins. In order to avoid differential mode noise pickup in the sensed signal, the loop area should be small. Thus the FB trace should be routed atop the signal ground plane, and the CS+ and CS– pins should be routed as a closely coupled pair (the CS+ pin should be over the signal ground plane as well).
16. The CS+ and CS– traces should be Kelvin-connected to the current sense resistor, so that the additional voltage drop due to current flow on the PCB at the current sense resistor connections, does not affect the sensed voltage.

C01033–2.5–1/01 (rev. 0)

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 16-Lead SOIC
### (R-16A/SO-16)

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