16-Channel, 16-Bit Analog-to-Digital Converter

FEATURES

- 16 Bits, No Missing Codes
- Fixed-Channel or Automatic Channel Scan
- Fixed-Channel Data Rate: 125kSPS
- Auto-Scan Data Rate: 23.7kSPS/Channel
- Single-Conversion Settled Data
- 16 Single-Ended or 8 Differential Inputs
- Unipolar (+5V) or Bipolar (±2.5V) Operation
- 0.3LSB (INL)
- DC Stability:
  0.02μV/°C Offset Drift, 0.4ppm/°C Gain Drift
- Open-Sensor Detection
- Conversion Control Pin
- Multiplexer Output for External Signal Conditioning
- On-Chip Temperature, Reference, Offset, Gain, and Supply Voltage Readback
- 42mW Power Dissipation
- Standby, Sleep, and Power-Down Modes
- Eight General-Purpose Inputs/Outputs (GPIO)
- 32.768kHz Crystal Oscillator or External Clock

APPLICATIONS

- Medical, Avionics, and Process Control
- Machine and System Monitoring
- Fast Scan Multi-Channel Instrumentation
- Industrial Systems
- Test and Measurement Systems

DESCRIPTION

The ADS1158 is a 16-channel (multiplexed), low-noise, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC) that provides single-cycle settled data at channel scan rates from 1.8k to 23.7k samples per second (SPS) per channel. A flexible input multiplexer accepts combinations of eight differential or 16 single-ended inputs with a full-scale differential range of 5V or true bipolar range of ±2.5V when operating with a 5V reference. The fourth-order delta-sigma modulator is followed by a fifth-order sinc digital filter optimized for low-noise performance.

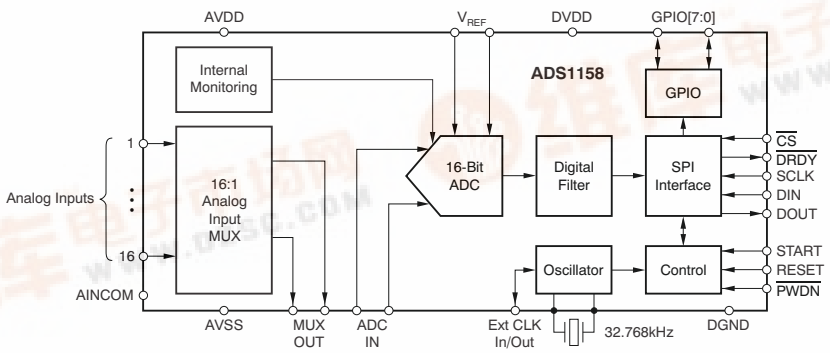
The differential output of the multiplexer is accessible to allow signal conditioning before the input of the ADC. Internal system monitor registers provide supply voltage, temperature, reference voltage, gain, and offset data.

An onboard PLL generates the system clock from a 32.768kHz crystal, or can be overridden by an external clock source. A buffered system clock output (15.7MHz) is provided to drive a microcontroller or additional converters.

Serial digital communication is handled via an SPI™-compatible interface. A simple command word structure controls channel configuration, data rates, digital I/O, monitor functions, etc.

Programmable sensor bias current sources can be used to bias sensors or verify sensor integrity.

The ADS1158 operates from a unipolar +5V or bipolar ±2.5V analog supply and a digital supply compatible with interfaces ranging from 2.7V to 5.25V. The ADS1158 is available in a QFN-48 package.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range, unless otherwise noted.(1)

	ADS1158	UNIT
AVDD to AVSS	–0.3 to +5.5	V
AVSS to DGND	–2.8 to +0.3	V
DVDD to DGND	–0.3 to +5.5	V
Input current	100, momentary	mA
Input current	10, continuous	mA
Analog input voltage	AVSS – 0.3 to AVDD + 0.3	V
Digital input voltage to DGND	–0.3 to DVDD + 0.3	V
Maximum junction temperature	+150	°C
Operating temperature range	–40 to +105	°C
Storage temperature range	–60 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = –40°C to +105°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = +3.3V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), OPA227 buffer between MUX outputs and ADC inputs, V_{REF} = +4.096V, and VREFN = –2.5V, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1158			UNIT
			MIN	TYP	MAX	
Analog Multiplexer Inputs						
Absolute input voltage	AIN0–AIN15, AINCOM with respect to DGND		AVSS – 100mV		AVDD + 100mV	V
On-channel resistance				80		Ω
Crosstalk		f_{IN} = 1kHz		–110		dB
Sensor bias (current source)		SBCS[1:0] = 01		1.5		µA
		SBCS[1:0] = 11		24		
1.5µA:24µA ratio error				1		%
ADC Input						
Full-scale input voltage	(V_{IN} = ADCINP – ADCINN)			±1.06$\overline{6}$ V_{REF}		V
Absolute input voltage	(ADCINP, ADCINN)		AVSS – 100mV		AVDD + 100mV	V
Differential input impedance				65		kΩ
System Performance						
Resolution		No missing codes	16			Bits
Data rate, fixed-channel mode			1.953		125	kSPS
Data rate, auto-scan mode			1.805		23.739	kSPS
Integral nonlinearity (INL)(1)		Differential input		0.3	1	LSB(2)
Offset error	Chopping on	Shorted inputs	–1	–0.5(3)	0	LSB
Offset drift		Shorted inputs		1		µV/°C
Gain error				0.1	0.5	%
Gain drift				2		ppm/°C
Noise				0.6		LSB ($_{PP}$)
Common-mode rejection		f_{CM} = 60Hz		100		dB
Power-supply rejection	AVDD, AVSS	f_{PS} = 60Hz		85		dB
	DVDD			95		
Voltage Reference Input						
Reference input voltage	(V_{REF} = VREFP – VREFN)		0.5	4.096	AVDD – AVSS	V
Negative reference input (VREFN)			AVSS – 0.1V		VREFP – 0.5	V
Positive reference input (VREFP)			VREFN + 0.5		AVDD + 0.1V	V
Reference input impedance				40		kΩ
System Parameters						
External reference reading error				1	3	%
Analog supply reading error				1	5	%
Temperature sensor reading	Voltage	T_A = +25°C		168		mV
	Coefficient			394		µV/°C

(1) Best straight line fit method.
(2) FSR = Full-scale range = 2.13$\overline{3}$ V_{REF}.
(3) Systematic –0.5LSB in reading code.

ELECTRICAL CHARACTERISTICS (continued)

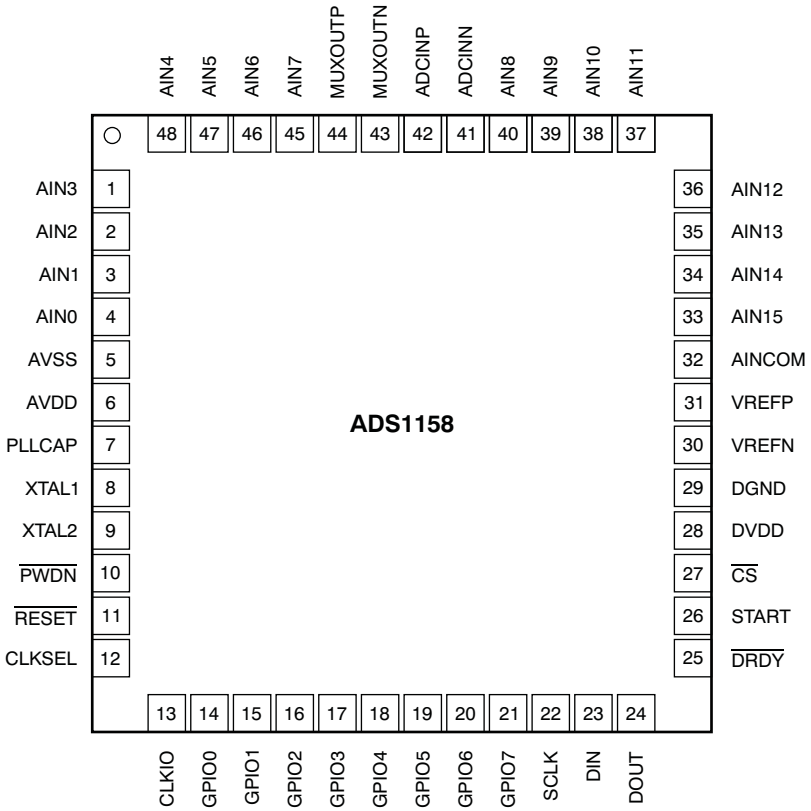
All specifications at T_A = –40°C to +105°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = +3.3V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), OPA227 buffer between MUX outputs and ADC inputs, V_{REF} = +4.096V, and VREFN = –2.5V, unless otherwise noted.

PARAMETER		CONDITIONS	ADS1158			UNIT
			MIN	TYP	MAX	
Digital Input/Output						
Logic levels	V_{IH}		0.7DVDD		DVDD	V
	V_{IL}		DGND		0.3DVDD	V
	V_{OH}	I_{OH} = 2mA	0.8DVDD		DVDD	V
	V_{OL}	I_{OL} = 2mA	DGND		0.2DVDD	V
Input leakage		V_{IN} = DVDD, GND			10	µA
Master clock input (CLKIO)	Frequency		0.1		16	MHz
	Duty cycle		40		60	%
Crystal oscillator (see *Crystal Oscillator* section)	Crystal frequency			32.768		kHz
	Clock output frequency			15.729		MHz
	Start-up time (clock output valid)			150		ms
	Clock output duty cycle		40		60	%
Power Supply						
DVDD			2.7		5.25	V
AVSS			–2.6		0	V
AVDD			AVSS + 4.75		AVSS + 5.25	V
DVDD supply current		External clock operation		0.25	0.6	mA
		Internal oscillator operation, clock output disabled		0.04		mA
		Internal oscillator operation, clock output enabled(4)		1.4		mA
		Power-down(5)		1	25	µA
AVDD, AVSS supply current		Converting		8.2	12	mA
		Standby		5.6		mA
		Sleep		2.1		mA
		Power-down		2	200	µA
Power dissipation		Converting		42	62	mW
		Standby		29		mW
		Sleep		11		mW
		Power-down		14		µW

(4) CLKIO load = 20pF.
(5) No clock applied to CLKIO.

PIN CONFIGURATION

QFN PACKAGE
(TOP VIEW)



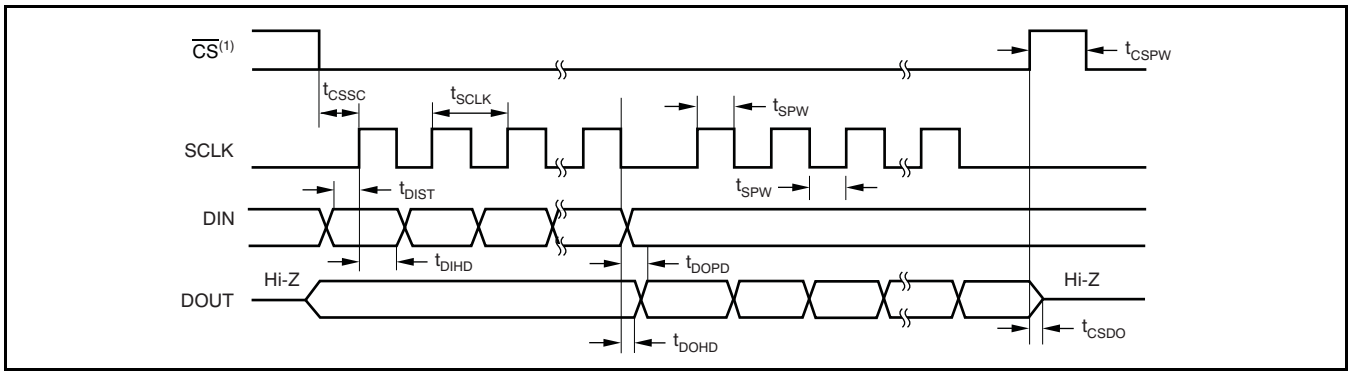
PIN ASSIGNMENTS

PIN #	NAME	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
1	AIN3	Analog input	Analog input 3: single-ended channel 3, differential channel 1 (–)
2	AIN2	Analog input	Analog input 2: single-ended channel 2, differential channel 1 (+)
3	AIN1	Analog input	Analog input 1: single-ended channel 1, differential channel 0 (–)
4	AIN0	Analog input	Analog input 0: single-ended channel 0, differential channel 0 (+)
5	AVSS	Analog	Negative analog power supply: 0V for unipolar operation, –2.5V for bipolar operation. (Internally connected to exposed thermal pad of QFN package.)
6	AVDD	Analog	Positive analog power supply: +5V for unipolar operation, +2.5V for bipolar operation.
7	PLLCAP	Analog	PLL bypass capacitor: connect 22nF capacitor to AVSS when using crystal oscillator.
8	XTAL1	Analog	32.768kHz crystal oscillator input 1; see *Crystal Oscillator* section.
9	XTAL2	Analog	32.768kHz crystal oscillator input 2; see *Crystal Oscillator* section.
10	$\overline{\text{PWDN}}$	Digital input	Power-down input: hold low for minimum of two f_{CLK} cycles to engage low-power mode.
11	$\overline{\text{RESET}}$	Digital input	Reset input: hold low for minimum of two f_{CLK} cycles to reset the device.
12	CLKSEL	Digital input	Clock select input: Low = activates crystal oscillator, f_{CLK} output on CLKIO. High = disables crystal oscillator, apply f_{CLK} to CLKIO.
13	CLKIO	Digital I/O	System clock input/output (see CLKSEL pin)
14	GPIO0	Digital I/O	General-purpose digital input/output 0
15	GPIO1	Digital I/O	General-purpose digital input/output 1
16	GPIO2	Digital I/O	General-purpose digital input/output 2
17	GPIO3	Digital I/O	General-purpose digital input/output 3
18	GPIO4	Digital I/O	General-purpose digital input/output 4
19	GPIO5	Digital I/O	General-purpose digital input/output 5
20	GPIO6	Digital I/O	General-purpose digital input/output 6

PIN ASSIGNMENTS (continued)

PIN #	NAME	ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
21	GPIO7	Digital I/O	General-purpose digital input/output 7
22	SCLK	Digital input	SPI interface clock input: data clocked in on rising edge, clocked out on falling edge.
23	DIN	Digital input	SPI interface data input: data are input to the device.
24	DOUT	Digital output	SPI interface data output: data are output from the device.
25	$\overline{\text{DRDY}}$	Digital output	Data ready output: active low.
26	START	Digital input	Start conversion input: active high.
27	$\overline{\text{CS}}$	Digital input	SPI interface chip select input: active low.
28	DVDD	Digital	Digital power supply: 2.7V to 5.25V
29	DGND	Digital	Digital ground
30	VREFN	Analog input	Reference input negative
31	VREFP	Analog input	Reference input positive
32	AINCOM	Analog input	Analog input common: common input pin to all single-ended inputs.
33	AIN15	Analog input	Analog input 15: single-ended channel 15, differential channel 7 (–)
34	AIN14	Analog input	Analog input 14: single-ended channel 14, differential channel 7 (+)
35	AIN13	Analog input	Analog input 13: single-ended channel 13, differential channel 6 (–)
36	AIN12	Analog input	Analog input 12: single-ended channel 12, differential channel 6 (+)
37	AIN11	Analog input	Analog input 11: single-ended channel 11, differential channel 5 (–)
38	AIN10	Analog input	Analog input 10: single-ended channel 10, differential channel 5 (+)
39	AIN9	Analog input	Analog input 9: single-ended channel 9, differential channel 4 (–)
40	AIN8	Analog input	Analog input 8: single-ended channel 8, differential channel 4 (+)
41	ADCINN	Analog input	ADC differential input (–)
42	ADCINP	Analog input	ADC differential input (+)
43	MUXOUTN	Analog output	Multiplexer differential output (–)
44	MUXOUTP	Analog output	Multiplexer differential output (+)
45	AIN7	Analog input	Analog input 7: single-ended channel 7, differential channel 3 (–)
46	AIN6	Analog input	Analog input 6 : single-ended channel 6, differential channel 3 (+)
47	AIN5	Analog input	Analog input 5: single-ended channel 5, differential channel 2 (–)
48	AIN4	Analog input	Analog input 4: single-ended channel 4, differential channel 2 (+)

PARAMETER MEASUREMENT INFORMATION



(1) $\overline{CS}$ can be tied low.

Figure 1. Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

At T_A= –40°C to +105°C and DVDD = 2.7V to 5.25V, unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{SCLK}	SCLK period	2		τ_{CLK} (1)
t_{SPW}	SCLK high or low pulse width (exceeding max resets SPI interface)	0.8	4096 (2)	τ_{CLK}
t_{CSSC}	$\overline{CS}$ low to first SCLK: setup time (3)	2.5		τ_{CLK}
t_{DIST}	Valid DIN to SCLK rising edge: setup time	10		ns
t_{DIHD}	Valid DIN to SCLK rising edge: hold time	5		ns
t_{DOPD}	SCLK falling edge to valid new DOUT: propagation delay (4)		20	ns
t_{DOHD}	SCLK falling edge to old DOUT invalid: hold time	0		ns
t_{CSDO}	$\overline{CS}$ high to DOUT invalid (3-state)		5	τ_{CLK}
t_{CSPW}	$\overline{CS}$ pulse width high	2		τ_{CLK}

(1) τ_{CLK} = master clock period = $1/f_{CLK}$.
(2) Programmable to 256 τ_{CLK}.
(3) $\overline{CS}$ can be tied low.
(4) DOUT load = 20pF || 100kΩ to DGND.

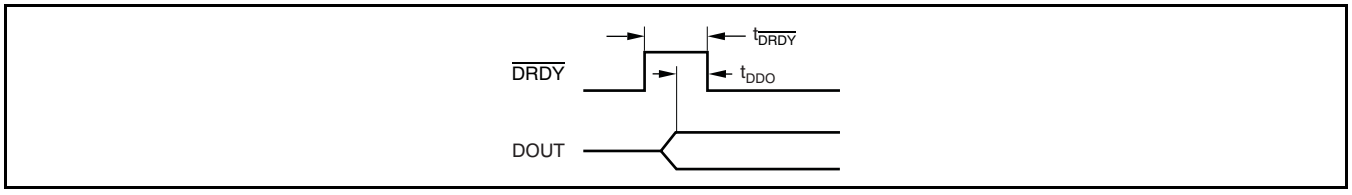


Figure 2. $\overline{DRDY}$ Update Timing

$\overline{DRDY}$ UPDATE TIMING CHARACTERISTICS

SYMBOL	DESCRIPTION	TYP	UNITS
$t_{\overline{DRDY}}$	$\overline{DRDY}$ high pulse width without data read	1	τ_{CLK}
t_{DDO}	Valid DOUT to $\overline{DRDY}$ falling edge ($\overline{CS}$ = 0)	0.5	τ_{CLK}

TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = +3.3V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), OPA227 buffer between MUX outputs and ADC inputs, VREFP = +2.048V, and VREFN = –2.048V, unless otherwise noted.

OFFSET WITH 0.5V REFERENCE, CHOPPING ON

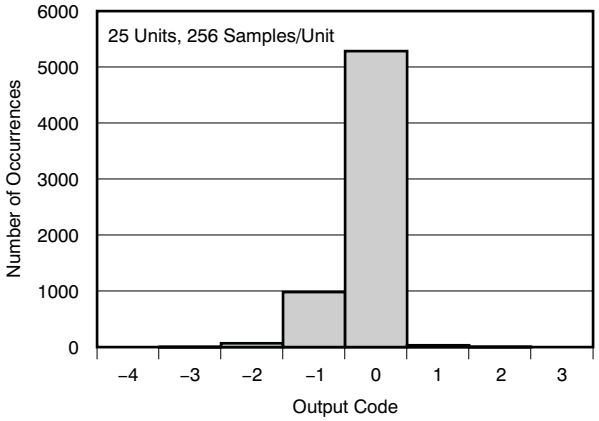


Figure 3.

OFFSET WITH 4.096V REFERENCE, CHOPPING ON

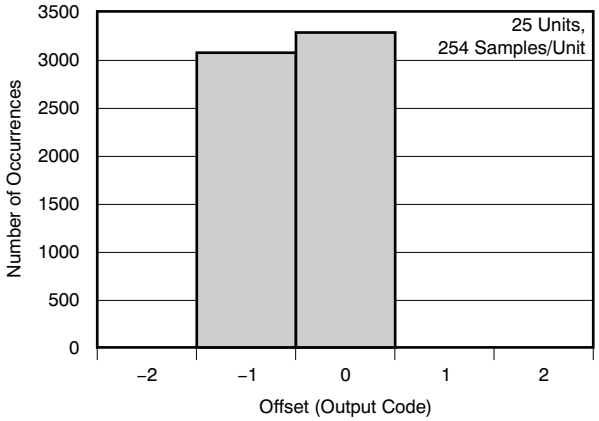


Figure 4.

OFFSET vs TEMPERATURE

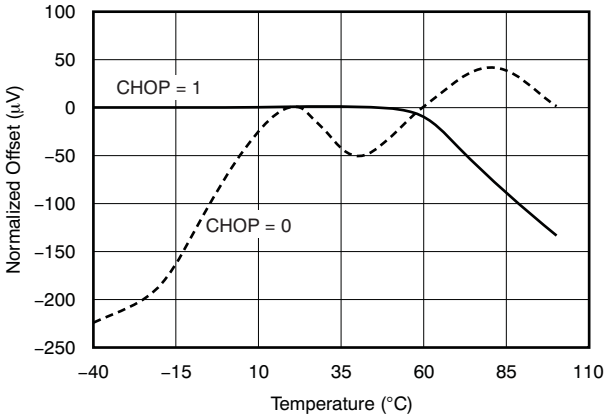


Figure 5.

GAIN ERROR HISTOGRAM

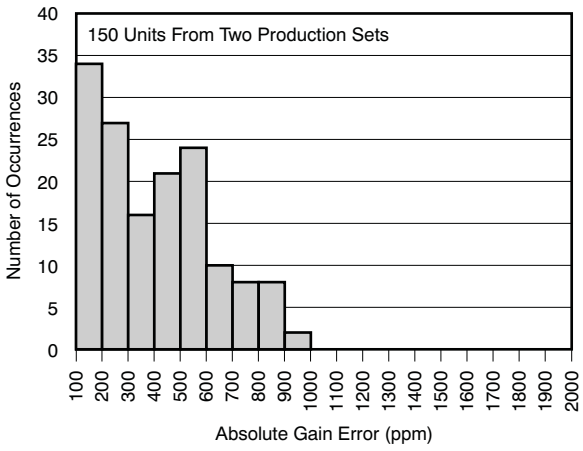


Figure 6.

GAIN DRIFT HISTOGRAM

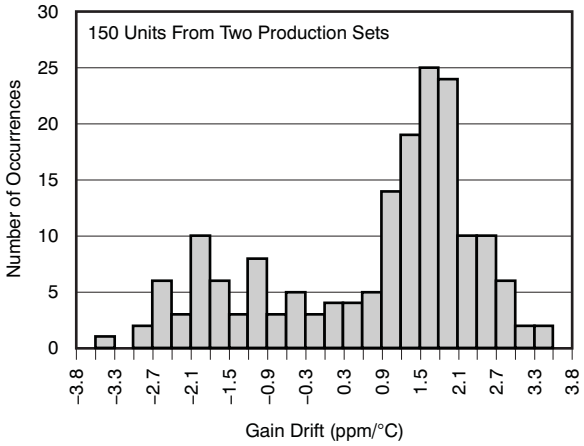


Figure 7.

GAIN ERROR vs TEMPERATURE

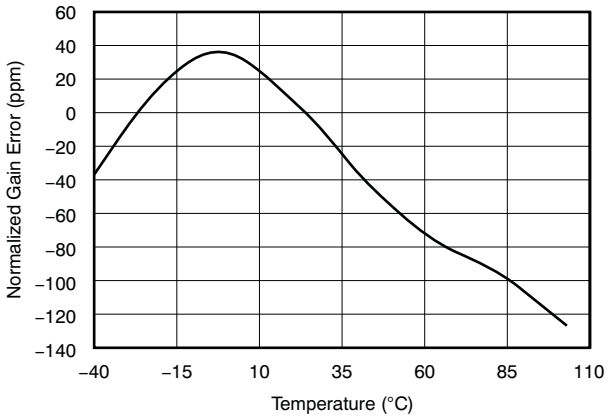


Figure 8.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = +3.3V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), OPA227 buffer between MUX outputs and ADC inputs, VREFP = +2.048V, and VREFN = –2.048V, unless otherwise noted.

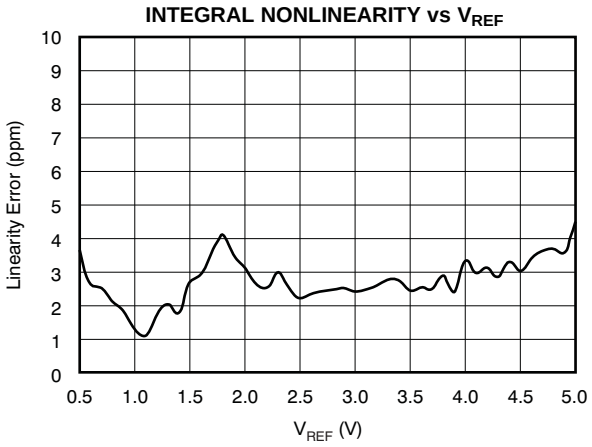


Figure 9.

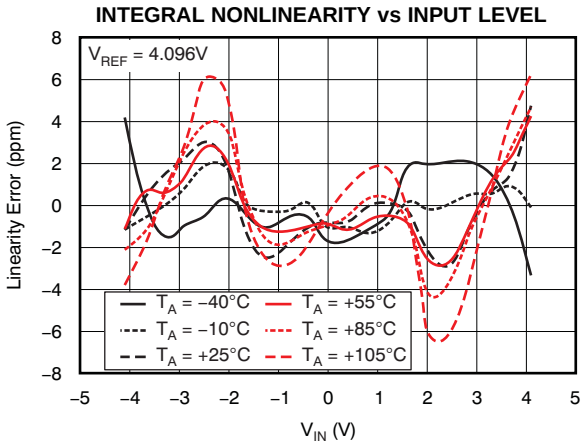


Figure 10.

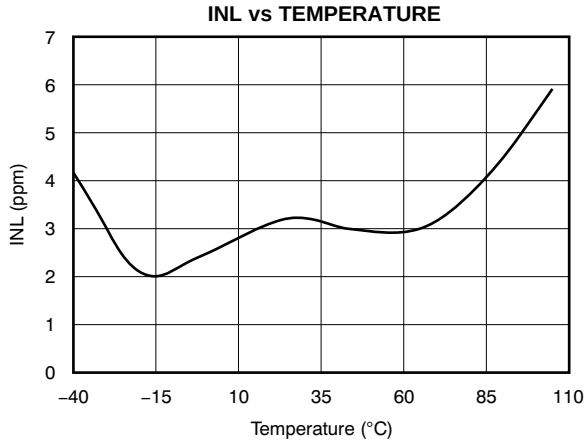


Figure 11.

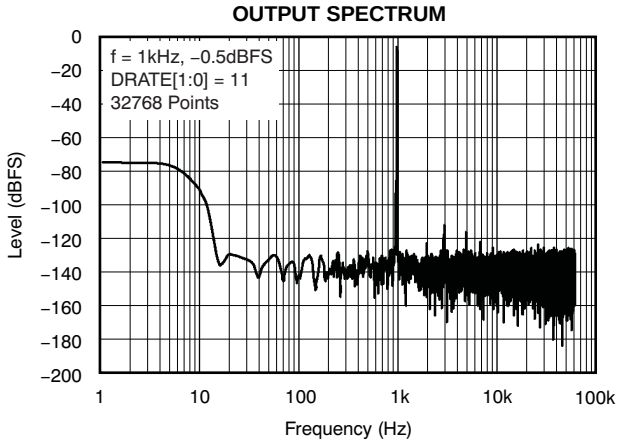


Figure 12.

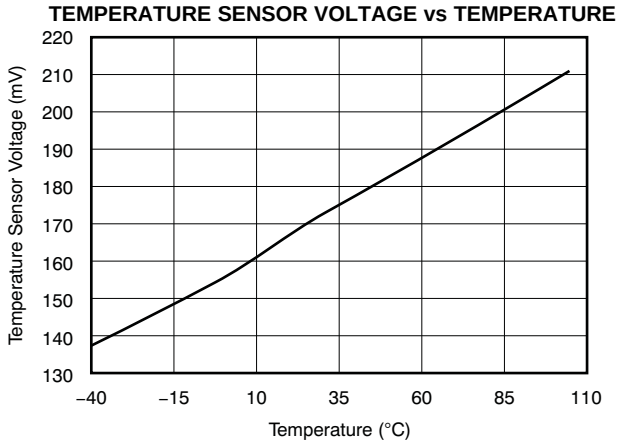


Figure 13.

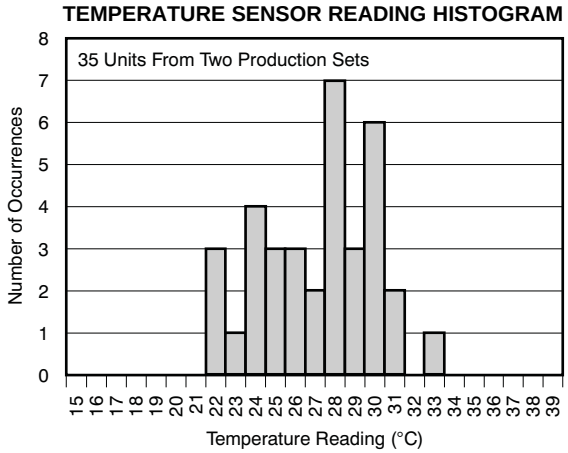


Figure 14.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, AVDD = +2.5V, AVSS = –2.5V, DVDD = +3.3V, f_{CLK} = 16MHz (external clock) or f_{CLK} = 15.729MHz (internal clock), OPA227 buffer between MUX outputs and ADC inputs, VREFP = +2.048V, and VREFN = –2.048V, unless otherwise noted.

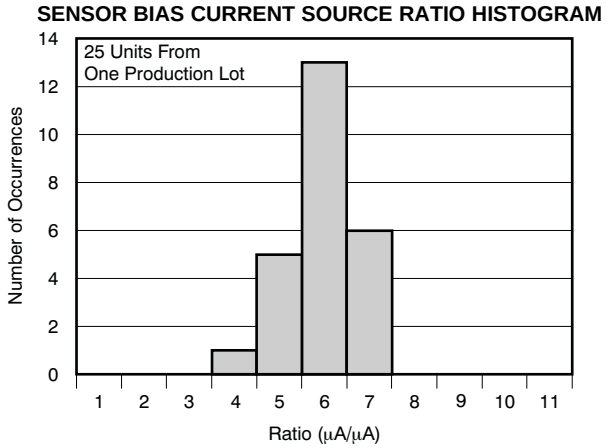


Figure 15.

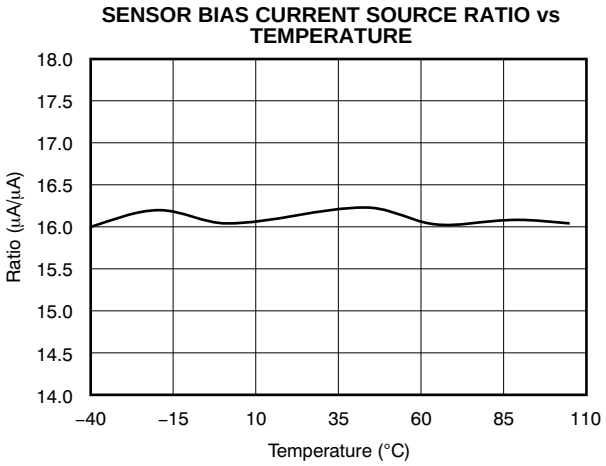


Figure 16.

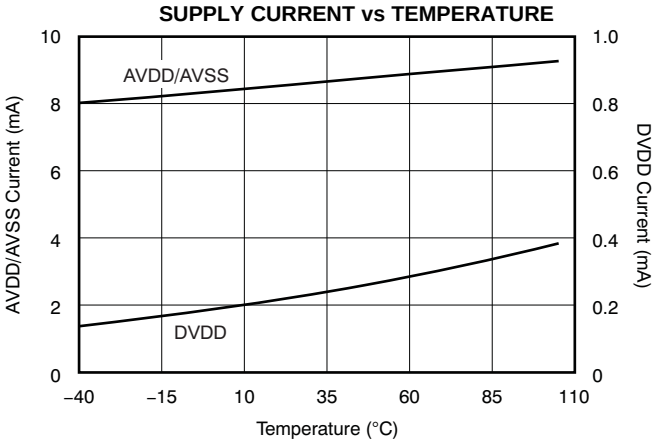


Figure 17.

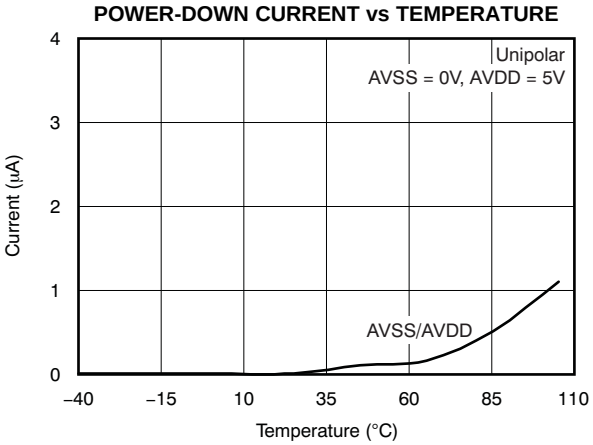


Figure 18.

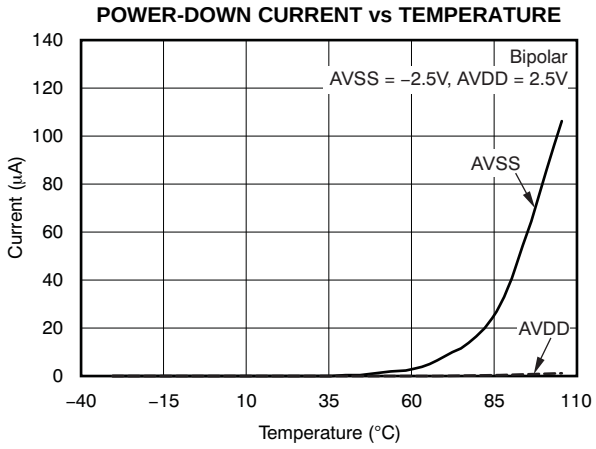


Figure 19.

OVERVIEW

The ADS1158 is a flexible, 16-bit, low-noise ADC optimized for fast multi-channel, high-resolution measurement systems. The converter provides a maximum channel scan rate of 23.7kSPS, giving a complete 16-channel scan in less than 700µs.

Figure 20 shows the block diagram of the ADS1158. The input multiplexer selects which analog input pins connect to the multiplexer output pins (MUXOUTP/MUXOUTN). External signal conditioning can be used between the multiplexer output pins and the ADC input pins (ADCINP/ADCINN) or the multiplexer output can be routed internally to the ADC inputs without external circuitry. Selectable current sources within the input multiplexer can be used to bias sensors or detect for a failed sensor. On-chip system function readings provide readback of temperature, supply voltage, gain, offset, and external reference.

The ADS1158 converter consists of a fourth-order, delta-sigma modulator followed by a programmable digital filter. The modulator measures the differential input signal, V_{IN} = (ADCINP – ADCINN), against the differential reference input, V_{REF} = (VREFP – VREFN). The digital filter receives the modulator signal and provides a low-noise digital output. The ADC channel block controls the multiplexer Auto-Scan feature. Channel Auto-Scan occurs at a maximum rate of 23.7kSPS. Slower scan rates can be used with corresponding increases in resolution.

Communication is handled over an SPI-compatible serial interface with a set of simple commands to control the ADS1158. Onboard registers store the various settings for the input multiplexer, sensor detect bias, data rate selection, etc. Either an external 32.768kHz crystal, connected to pins XTAL1 and XTAL2, or an external clock applied to pin CLKIO can be used as the clock source. When using the external crystal oscillator, the system clock is available as an output for driving other devices or controllers. General-purpose digital I/Os (GPIO) provide input and output control of eight pins.

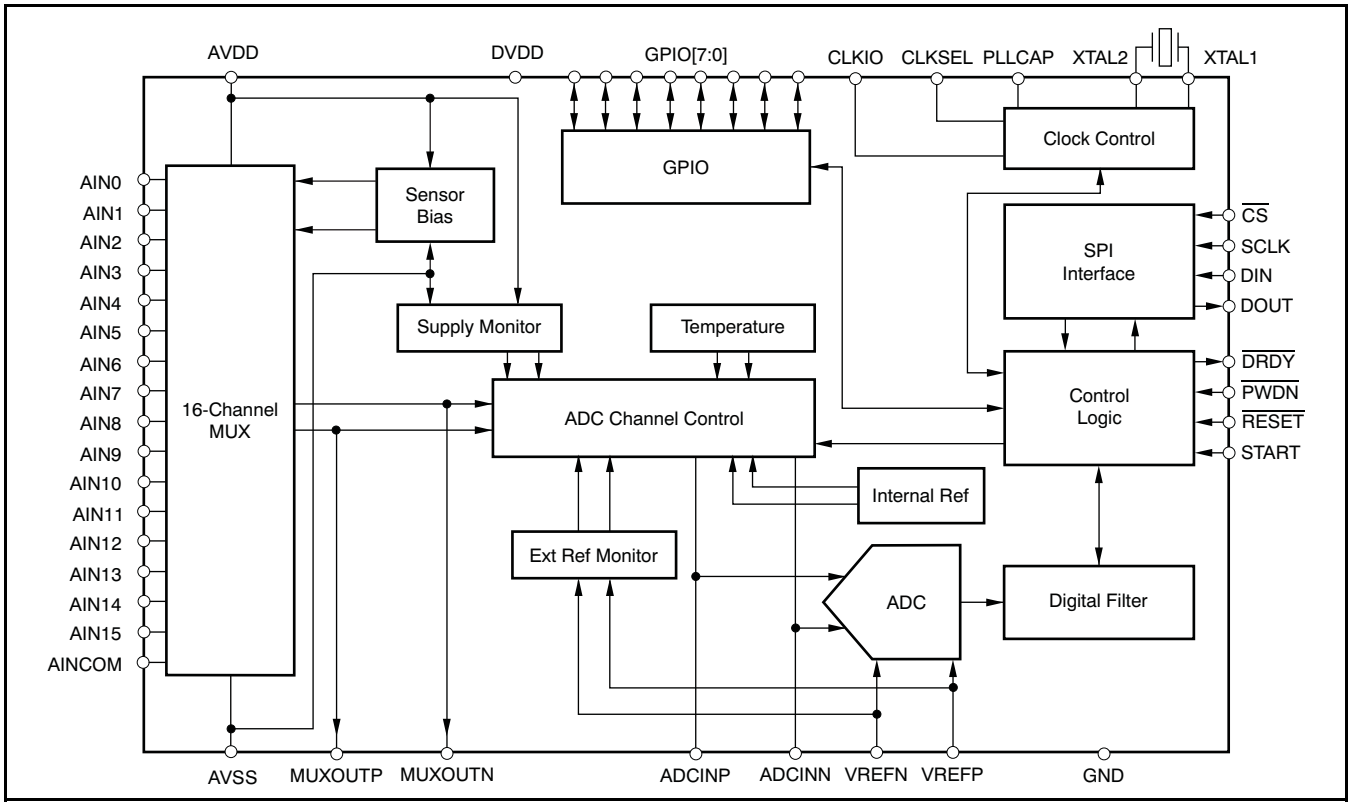


Figure 20. ADS1158 Block Diagram

MULTIPLEXER INPUTS

A simplified diagram of the input multiplexer is illustrated in Figure 22. The multiplexer connects one of 16 single-ended external inputs, one of eight differential external inputs, or one of the on-chip internal variables to the ADC inputs. The output of the channel multiplexer can be routed to external pins and then to the input of the ADC. This flexibility allows for use of external signal conditioning. See the *External Multiplexer Loop* section.

Electrostatic discharge (ESD) diodes protect the analog inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 100mV, and likewise do not exceed AVDD by more than 100mV:

AVSS – 100mV < (Analog Inputs) < AVDD + 100mV.

Overdriving the multiplexer inputs may affect the conversions of other channels. See the *Input Overload Protection* description in the *Hardware Considerations* segment of the *Applications* section.

The converter supports two modes of channel access through the multiplexer: the Auto-Scan mode and the Fixed-Channel mode. These modes are selected by the MUXMOD bit of register CONFIG0. The Auto-Scan mode scans through the selected channels automatically, with break-before-make switching. The Fixed-Channel mode requires the user to set the channel address for each channel measured.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference for the ADS1158 ADC is the differential voltage between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs with the circuitry on the reference inputs shown in Figure 21.

The load presented by the switched capacitor can be modeled with an effective resistance (R_{eff}) of 40kΩ for f_{CLK} = 16MHz. Note that the effective impedance of the reference inputs loads an external reference with a non-zero source impedance.

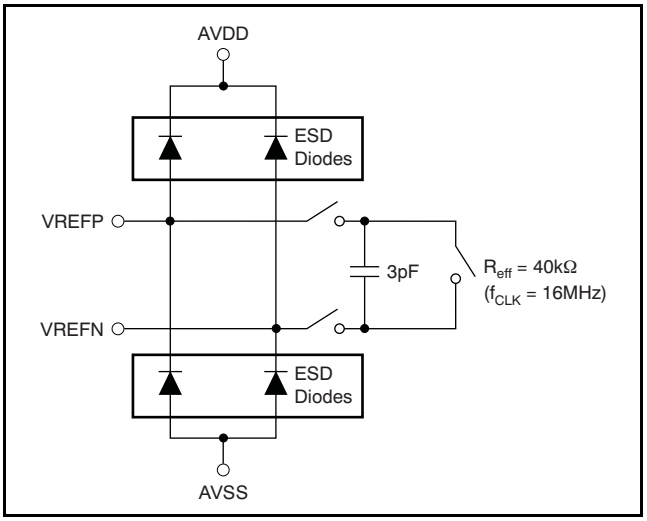


Figure 21. Simplified Reference Input Circuit

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AVSS by more than 100mV, and likewise do not exceed AVDD by 100mV:

AVSS – 100mV < (VREFP or VREFN) < AVDD + 100mV

A high-quality reference voltage is essential to achieve the best performance from the ADS1158. Noise and drift on the reference degrade overall system performance. It is especially critical that special care be given to the circuitry that generates the reference voltages and the layout when operating in the low-noise settings (that is, with low data rates) to prevent the voltage reference from limiting performance. See the *Reference Inputs* description in the *Hardware Considerations* segment of the *Applications* section.

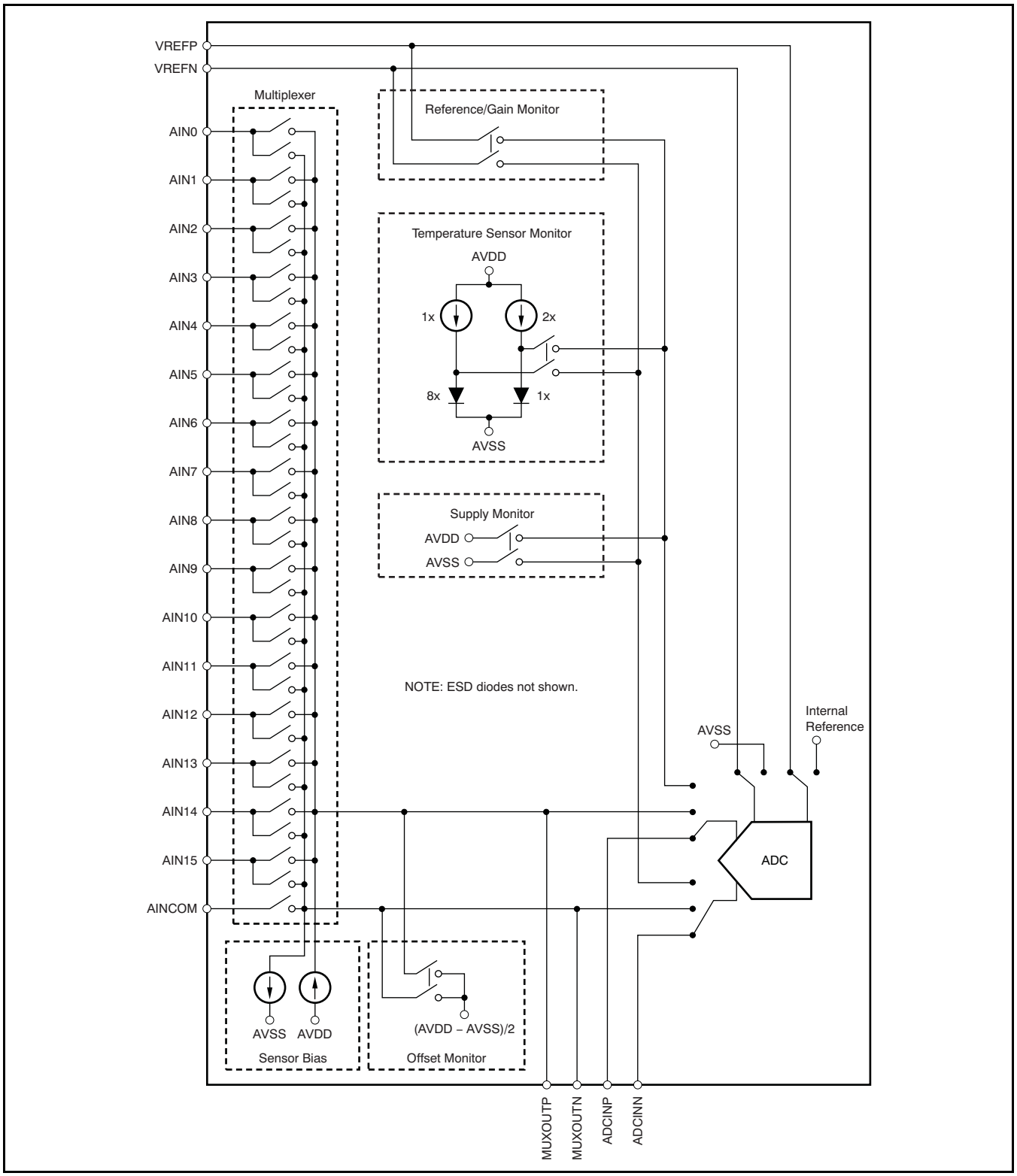


Figure 22. Input Multiplexer

ADC INPUTS

The ADS1158 ADC inputs (ADCINP, ADCINN) measure the input signal using internal capacitors that are continuously charged and discharged. The left side of Figure 24 shows a simplified schematic of the ADC input circuitry; the right side of Figure 24 shows the input circuitry with the capacitors and switches replaced by an equivalent circuit. Figure 23 shows the ON/OFF timings of the switches shown in Figure 24. S_1 switches close during the input sampling phase. With S_1 closed, C_{A1} charges to ADCINP, C_{A2} charges to ADCINN, and C_B charges to (ADCINP – ADCINN). For the discharge phase, S_1 opens first and then S_2 closes. C_{A1} and C_{A2} discharge to approximately AVSS + 1.3V and C_B discharges to 0V. This two-phase sample/discharge cycle repeats with a period of $t_{SAMPLE} = 2/f_{CLK}$.

The charging of the input capacitors draws a transient current from the source driving the ADS1158 ADC inputs. The average value of this current can be used to calculate an effective impedance (R_{eff}) where $R_{eff} = V_{IN}/I_{AVERAGE}$. These impedances scale inversely with f_{CLK}. For example, if f_{CLK} is reduced by a factor of two, the impedances will double.

As with the multiplexer and reference inputs, ESD diodes protect the ADC inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 100mV, and likewise do not exceed AVDD by more than 100mV.

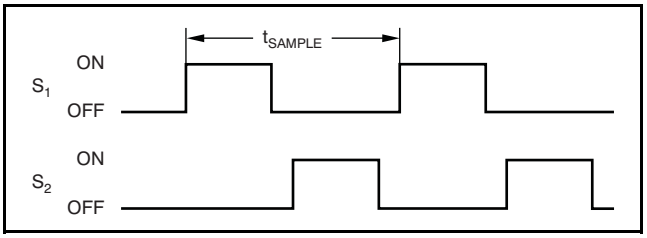


Figure 23. S_1 and S_2 Switch Timing for Figure 24

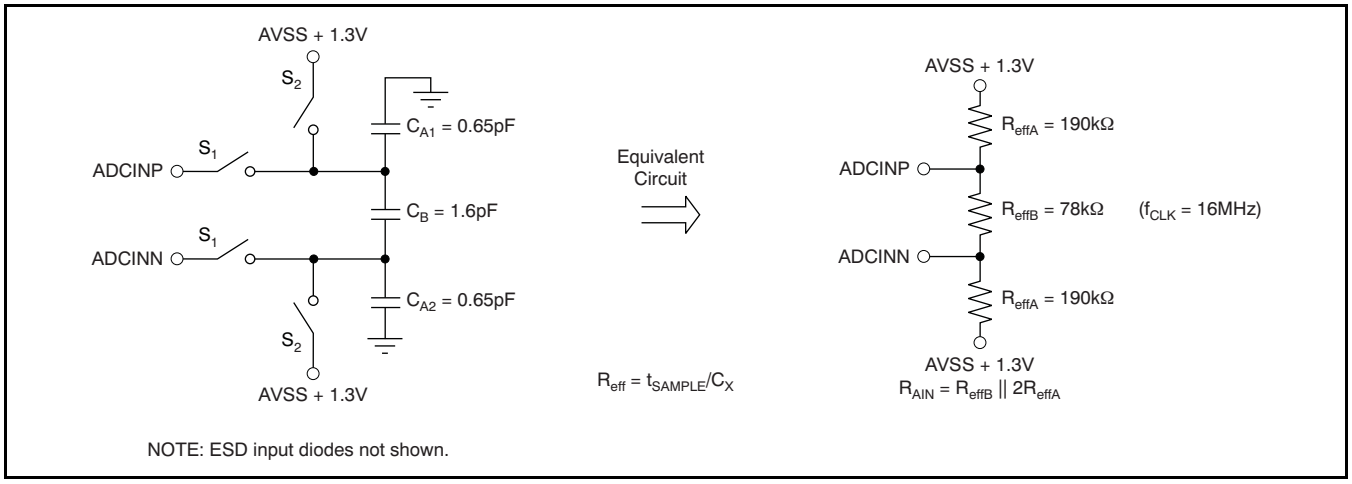


Figure 24. Simplified ADC Input Structure

MASTER CLOCK (f_{CLK})

The ADS1158 oversamples the analog input at a high rate. This oversampling requires a high-frequency master clock to be supplied to the converter. As shown in Figure 25, the clock comes from either an internal oscillator (with external crystal), or an external clock source.

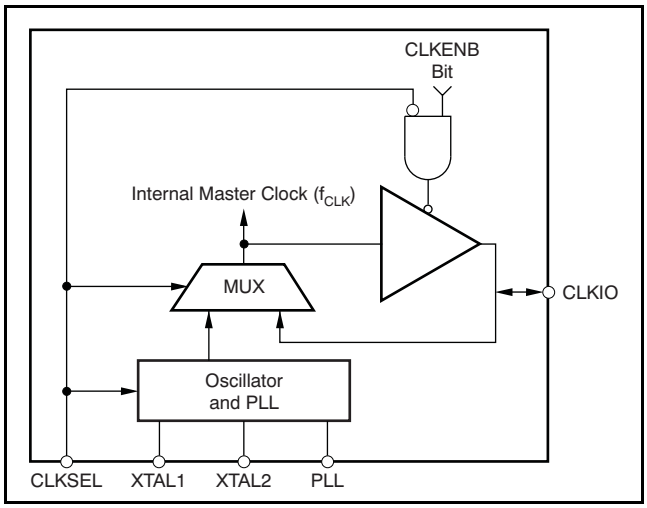
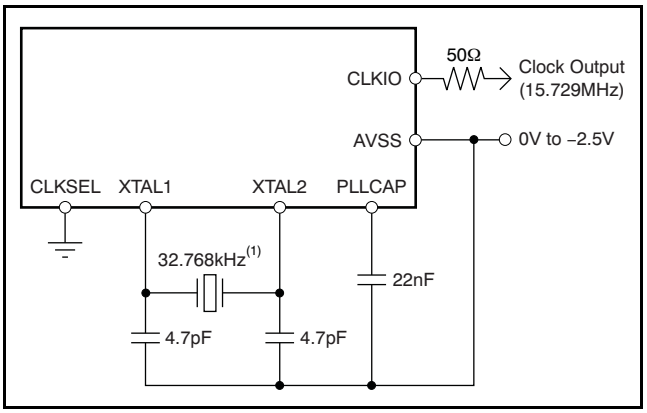


Figure 25. Clock Generation Block Diagram

The CLKSEL pin determines the source of the system clock, as shown in Table 1. The CLKIO pin functions as an input or as an output. When the CLKSEL pin is set to '1', CLKIO is configured as an input to receive the master clock. When the CLKSEL pin is set to '0', the crystal oscillator generates the clock. The CLKIO pin can then be configured to output the master clock. When the clock output is not needed, it can be disabled to reduce device power consumption.

Crystal Oscillator

An on-chip oscillator and phase-locked loop (PLL) together with an external crystal can be used to generate the system clock. For this mode, tie the CLKSEL pin low. A 22nF PLL filter capacitor, connected from the PLLCAP pin to the AVSS pin, is required. The internal clock of the PLL can be output to the CLKIO to drive other converters or controllers. If not used, disable the clock output to reduce device power consumption; see Table 1 for settings. The clock output is enabled by a register bit setting (default is ON). Figure 26 shows the oscillator connections. Place these components as close to the pins as possible to avoid interference and coupling. Do not connect XTAL1 or XTAL2 to any other logic. The oscillator start-up time may vary, depending on the crystal and ambient temperature. The user should verify the oscillator start-up time.



(1) Parallel resonant type. C_L = 12.5pF, ESR = 35kΩ (max). Place the crystal and load capacitors as close as possible to the device pins.

Figure 26. Crystal Oscillator Connection

Table 1. System Clock Source

CLKSEL PIN	CLOCK SOURCE	CLKENB BIT	CLKIO FUNCTION
0	32.768kHz crystal oscillator	0	Disabled (internally grounded)
0	32.768kHz crystal oscillator	1	Output (15.729MHz)
1	External clock input	X	Input (16MHz)

Table 2. Approved Crystal Vendors

VENDOR	CRYSTAL PRODUCT
Epson	C-001R

External Clock Input

When using an external clock to operate the device, apply the master clock to the CLKIO pin. For this mode, the CLKSEL pin is tied high. CLKIO then becomes an input, as shown in Figure 27.

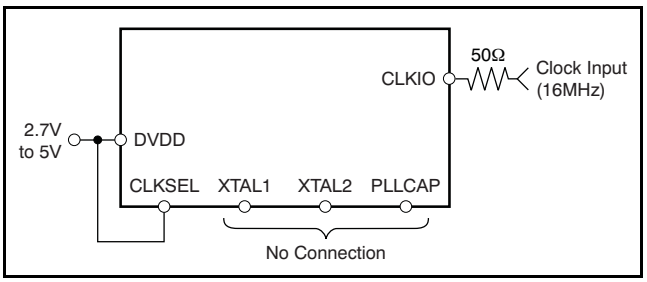


Figure 27. External Clock Connection

Make sure to use a clock source clean from jitter or interference. Ringing or under/overshoot should be avoided. A 50Ω resistor in series with the CLKIO pin (placed close to the source) can often help.

ADC

The ADC block of the ADS1158 is composed of two blocks: a modulator and a digital filter.

Modulator

The modulator converts the analog input voltage into a pulse code modulated (PCM) data stream. When the level of differential analog input (ADCINP – ADCINN) is near the level of the reference voltage, the '1' density of the PCM data stream is at its highest. When the level of the differential analog input is near zero, the PCM '0' and '1' densities are nearly equal. The fourth-order modulator shifts the quantization noise to a high frequency (out of the passband) where the digital filter can easily remove it.

The modulator continuously chops the input, resulting in excellent offset and offset drift performance. It is important to note that offset or offset drift that originates from the external circuitry is not removed by the modulator chopping. These errors can be effectively removed by using the external chopping feature of the ADS1158 (see the *External Chopping* section).

Digital Filter

The programmable low-pass digital filter receives the modulator output and produces a high-resolution digital output. By adjusting the amount of filtering, tradeoffs can be made between resolution and data rate—filter more for higher resolution, filter less for higher data rate. The filter consists of two sections, a fixed filter followed by a programmable filter.

Figure 28 shows the block diagram of the filter. Data are supplied to the filter from the analog modulator at a rate of $f_{CLK}/2$. The fixed filter is a fifth-order sinc filter with a decimation value of 64 that outputs data at a rate of $f_{CLK}/128$. The second stage of the filter is a programmable averager (first-order sinc filter) with the number of averages set by the DRATE[1:0] bits.

The data rate depends upon the system clock frequency (f_{CLK}) and the converter configuration. The data rate can be computed by Equation 1 or Equation 2:

Data rate (Auto-Scan):

$$\frac{f_{CLK}}{128(4^{11b - DR} + 4.26525 + TD) \times 2^{CHOP}} \quad (1)$$

Data rate (Fixed-Channel mode):

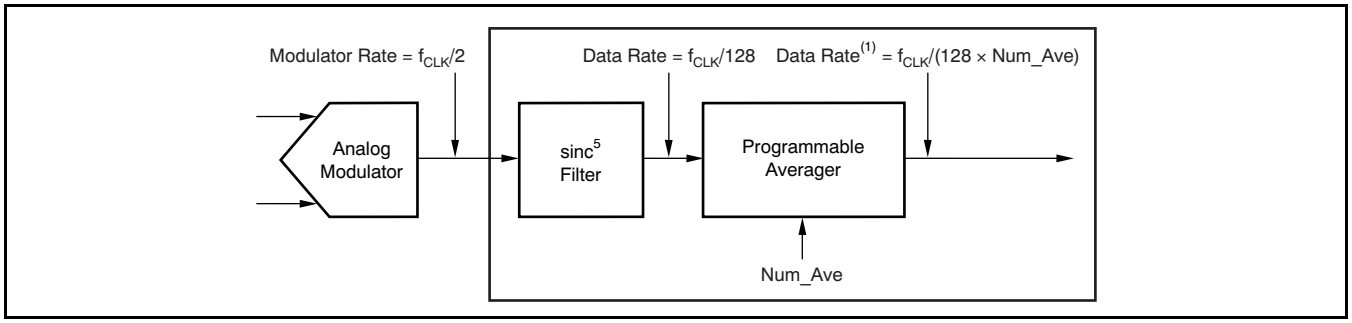
$$\frac{f_{CLK}}{128[4^{11b - DR} + CHOP(4.26525 + TD)] \times 2^{CHOP}} \quad (2)$$

Where:

DR = DRATE[1:0] register bits (binary).

CHOP = Chop register bit.

TD = time delay value given in Table 4 from the DLY[2:0] register bits ($128/f_{CLK}$ periods).



(1) Data rate for Fixed-Channel mode, Chop = 0, Delay = 0.

Figure 28. Block Diagram of Digital Filter

Table 3 shows a listing of the averaging and data rates for each of the four DRATE[1:0] register settings for the Auto-Scan and Fixed-Channel modes, with CHOP, DLY = 0. Note that the data rate scales directly with f_{CLK}. For example, reducing f_{CLK} by 2x reduces the maximum data rate by 2x.

FREQUENCY RESPONSE

The low-pass digital filter sets the overall frequency response for the ADS1158. The filter response is the product of the responses of the fixed and programmable filter sections and is given by Equation 3:

$$\left|H_{(f)}\right| = \left|H_{sinc}{}^{5}(f)\right| \times \left|H_{Averager}(f)\right| =$$

$$\left| \frac{\sin\left(\frac{128\pi \times f}{f_{CLK}}\right)}{64 \times \sin\left(\frac{2\pi \times f}{f_{CLK}}\right)} \right|^{5} \times \left| \frac{\sin\left(\frac{128\pi \times Num\_Ave \times f}{f_{CLK}}\right)}{Num\_Ave \times \sin\left(\frac{128\pi \times f}{f_{CLK}}\right)} \right| \quad (3)$$

The digital filter attenuates noise on the modulator output, including noise from within the ADS1158 and external noise present within the ADS1158 input signal. Adjusting the filtering by changing the number of averages used in the programmable filter changes the filter bandwidth. With a higher number of averages, the bandwidth is reduced and more noise is attenuated.

The low-pass filter has notches (or *zeros*) at the data output rate and multiples thereof. The sinc^5 part of the filter produces wide notches at f_{CLK}/128 and multiples thereof. At these frequencies, the filter has zero gain. Figure 29 shows the response with no post averaging. Note that in Auto-Scan mode, the data rate is reduced while retaining the same frequency response as in Fixed-Channel mode.

With programmable averaging, the wide notches produced by the sinc^5 filter remain, but a number of narrow notches are superimposed in the response. The number of the superimposed notches is determined by the number of readings averaged (minus one).

Figure 30 shows the response with averaging set to 4 (DRATE[1:0] = 10). 4-reading, post-averaging produces three equally-spaced notches between each main notch of the sinc^5 filter. The frequency response of DRATE[1:0] = 01 and 00 follows a similar pattern, but with 15 and 63 equally-spaced notches between the main sinc^5 notches, respectively.

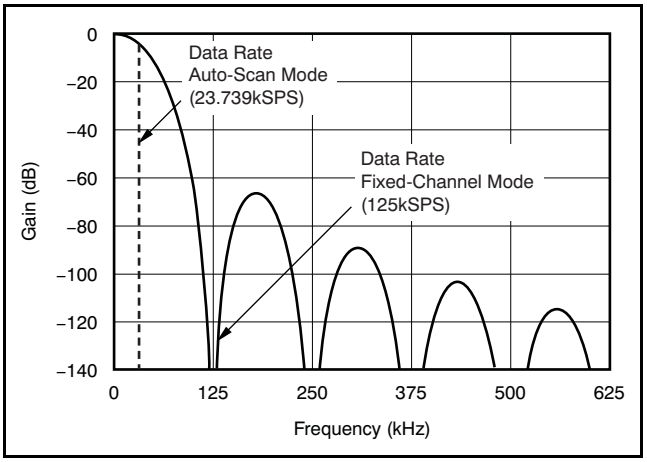


Figure 29. Frequency Response, DRATE[1:0] = 11

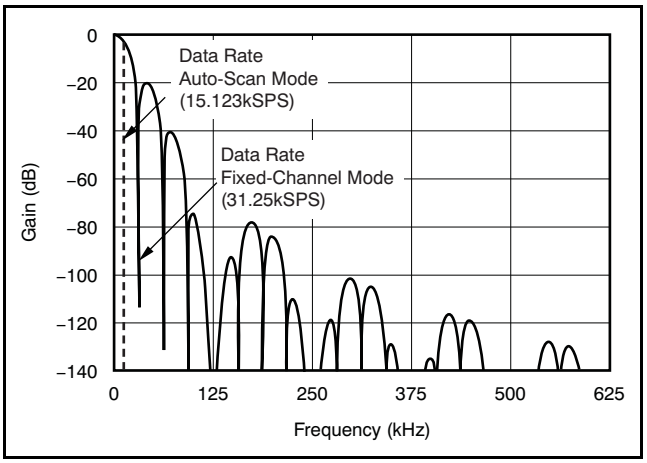


Figure 30. Frequency Response, DRATE[1:0] = 10

Table 3. Data Rates(1)

DRATE[1:0]	Num_Ave(2)	DATA RATE AUTO-SCAN MODE (SPS)(3)	DATA RATE FIXED-CHANNEL MODE (SPS)	–3dB BANDWIDTH (Hz)
11	1	23739	125000	25390
10	4	15123	31250	12402
01	16	6168	7813	3418
00	64	1831	1953	869

(1) f_{CLK} = 16MHz, Chop = 0, and Delay = 0.
(2) Num_Ave is the number of averages performed by the digital filter second stage.
(3) In Auto-Scan mode, the data rate listed is for a single channel; the effective data rate for multiple channels (on a per-channel basis) is the value shown in Figure 29 and Figure 30 divided by the number of active channels in a scan loop.

ALIASING

The digital filter low-pass characteristic repeats at multiples of the modulator rate of $f_{CLK}/2$. Figure 31 shows the response plotted out to 16MHz at the data rate of 125kSPS (Fixed-Channel mode). Notice how the responses near dc, 8MHz, and 16MHz are the same. The digital filter attenuates high-frequency noise on the ADS1158 inputs up to the frequency where the response repeats. However, noise or frequency components present on the analog input where the response repeats alias into the passband. For most applications, an anti-alias filter is recommended to remove this noise. A simple first-order input filter with a pole at 200kHz provides –34dB rejection at the first image frequency.

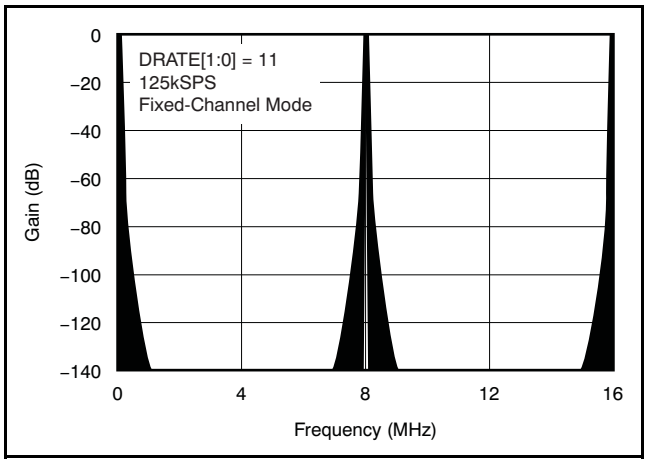


Figure 31. Frequency Response Out to 16MHz

Referring to Figure 29 and Figure 30, frequencies present on the analog input above the Nyquist rate (sample rate/2) are first attenuated by the digital filter and then aliased into the passband.

SETTLING TIME

The design of the ADS1158 provides fully-settled data when scanning through the input channels in Auto-Scan mode. The $\overline{\text{DRDY}}$ flag asserts low when the data for each channel are ready. It may be necessary to use the automatic switch time delay feature to provide time for settling of the external buffer and associated components after channel switching. When the converter is started (START pin transitions high or Start Command) with stable inputs, the first converter output is fully settled. When applying asynchronous step inputs, the settling time is somewhat different. The step-input settling time diagrams (Figure 32 and Figure 33) show the converter step response with an asynchronous step input. For most modes of operation, the analog input must be stable for one complete conversion cycle to provide settled data. In Fixed-Channel mode (DRATE[1:0] = 11), the input must be stable for five complete conversion cycles.

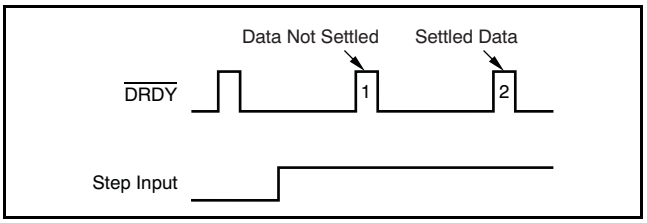


Figure 32. Asynchronous Step-Input Settling Time (DRATE[1:0] = 10, 01, 00)

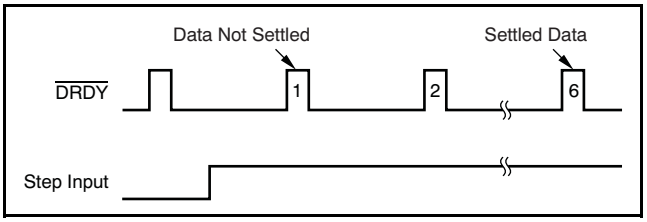


Figure 33. Asynchronous Step-Input Settling Time (Fixed-Channel Mode, DRATE[1:0] = 11)

Table 4. Effective Data Rates with Switch-Time Delay (Auto-Scan Mode)(1)

DLY [2:0]	TIME DELAY (128/f_{CLK} periods)	TIME DELAY (μS)	DRATE [1:0] = 11	DRATE [1:0] = 10	DRATE [1:0] = 01	DRATE [1:0] = 00
000	0	0	23739	15123	6168	1831
001	1	8	19950	13491	5878	1805
010	2	16	17204	12177	5614	1779
011	4	32	13491	10191	5151	1730
100	8	64	9423	7685	4422	1639
101	16	128	5878	5151	3447	1483
110	32	256	3354	3104	2392	1247
111	48	384	2347	2222	1831	1075

(1) Time delay and data rates scale with f_{CLK}. If Chop = 1, the data rates are half those shown. f_{CLK} = 16MHz, Auto-Scan mode.

EXTERNAL MULTIPLEXER LOOP

The external multiplexer loop consists of two differential multiplexer output pins and two differential ADC input pins. The user may use external components (buffering/filtering, single-ended to differential conversion, etc.) to form a signal conditioning loop. For best performance, the ADC input should be buffered and driven differentially.

To bypass the external multiplexer loop, connect the ADC input pins directly to the multiplexer output pins, or select internal bypass connection (BYPASS = 0 of CONFIG0). Note that the multiplexer output pins are active regardless of the bypass setting.

SWITCH TIME DELAY

When using the ADS1158 in the Auto-Scan mode, where the converter automatically switches from one channel to the next, the settling time of the external signal conditioning circuit becomes important. If the channel does not fully settle after the multiplexer channel is switched, the data may not be correct. The ADS1158 provides a switch time delay feature which automatically provides a delay after channel switching to allow the channel to settle before taking a reading. The amount of time delay required depends primarily on the settling time of the external signal conditioning. Additional consideration may be needed to account for the settling of the input source arising from the transient generated from channel switching.

Use of the switch time delay register reduces the effective channel data rate. Table 4 shows the actual data rates derived from Equation 1, when using the switch time delay feature.

When pulse converting, where one channel is converted with each START pin pulse or each pulse command, the application software may provide the required time delay between pulses. However, with Chop = 1, the switch time delay feature may continue to be necessary to allow for settling.

In estimating the time delay that may be required, Table 5 lists the time delay-to-time constant ratio (t/τ) and the corresponding final settled data in % and number of bits.

Table 5. Settling Time

t/τ (1)	FINAL SETTLING (%)	FINAL SETTLING (Bits)
1	63	2
3	95	5
5	99.3	7
7	99.9	10
10	99.995	14
15	99.998	16

(1) Multiple time constants can be approximated by: $(\tau_1^2 + \tau_2^2 + \ldots)^{=}$.

SENSOR BIAS

An integrated current source provides a means to bias an external sensor (for example, a diode junction); or, it verifies the integrity of a sensor or sensor connection. When the sensor fails to an open condition, the current sources drive the inputs of the converter to positive full-scale. The biasing is in the form of differential currents (programmable 1.5µA or 24µA), connected to the output of the multiplexer.

Figure 34 shows a simplified diagram of ADS1158 input structure with the external sensor modeled as a resistance R_S between two input pins. The two 80Ω series resistors, R_{MUX}, model the ADS1158 internal resistances. R_L represents the effective input resistance of the ADC input or external buffer. When the sensor bias is enabled, they source I_{SDC} to one selected input pin (connected to the MUXOUTP channel) and sink I_{SDC} from the other selected input pin (connected to the MUXOUTN channel). The signal measured with the biasing enabled equals the total IR drop: $I_{SDC}[(2R_{MUX} + R_S) \parallel R_L]$. Note that when the sensor is a direct short (that is, $R_S = 0$), there continues to be a small signal measured by the ADS1158 when the biasing is enabled: $I_{SDC}[2R_{MUX} \parallel R_L]$.

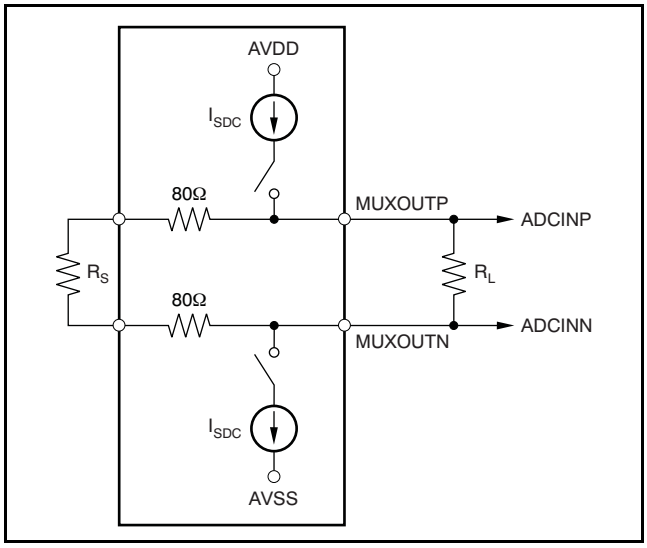


Figure 34. Sensor Bias Structure

The current source is connected to the output of the multiplexer. For unselected channels, the current source is not connected. This configuration means that when a new channel is selected, the current source charges stray sensor capacitance, which may slow the rise of the sensor voltage. The automatic switch time delay feature can be used to apply an appropriate time delay before a conversion is started to provide fully settled data (see the *Switch Time Delay* section).

The time to charge the external capacitance is given in Equation 4:

$$\frac{dV}{dt} = \frac{I_{SDC}}{C} \quad (4)$$

It is also important to note that the low impedance (65kΩ) of the direct ADC inputs or the impedance of the external signal conditioning loads the current sources. This low impedance limits the ability of the current source to pull the inputs to positive full-scale for open-channel detection.

OPEN-SENSOR DETECTION

For open-sensor detection, set the biasing to either 1.5µA or 24µA. Then select the channel and read the output code. When a sensor opens, the positive input is pulled to AVDD and the negative input is pulled to AVSS. Because of this configuration, the output code trends toward positive full-scale. Note that the interaction of the multiplexer resistance with the current source may lead to degradation in converter linearity. It is recommended to enable the current source only periodically to check for open inputs and discard the associated data.

EXTERNAL DIODE BIASING

The current source can be used to bias external diodes for temperature sensing. Scan the appropriate channels with the current source set to 24µA. Re-scan the same channels with the current source set to 1.5µA. The difference in diode voltage readings resulting from the two bias currents is directly proportional to temperature.

Note that errors in current ratio, diode and cable resistance, or the non-ideality factor of the diode can lead to errors in temperature readings. These effects can be compensated by characterization or by calibrating the diode at known temperatures.

EXTERNAL CHOPPING

The modulator of the ADS1158 incorporates a chopping front-end that removes offset errors to provide excellent offset and offset drift performance. However, offset and offset drift that originate from external signal conditioning are not removed by the modulator. The ADS1158 has an additional chopping feature that removes external offset errors (CHOP = 1).

With external chopping enabled, the converter takes two readings in succession on the same channel. The first reading is taken with one polarity and the second reading is taken with the opposite polarity. The converter averages the two readings and cancels the offset, as shown in Figure 35. With chopping enabled, the effective reading reduces to half of the nominal reading rate.

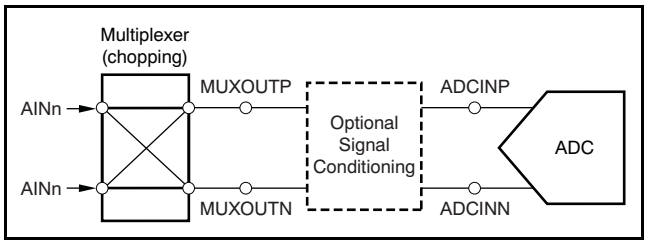


Figure 35. External Chopping

Note that because the inputs are reversed under control of the ADS1158, a delay time may be necessary to provide time for external signal conditioning to fully settle before the second phase of the reading sequence starts (see the *Switch Time Delay* section).

External chopping can be used to reduce total offset errors and offset drift over temperature. Note that chopping must be disabled (CHOP = 0) in order to take the internal monitor readings.

GPIO DIGITAL PORT (GPIOx)

The ADS1158 has eight dedicated general-purpose digital input/output (GPIO) pins. The digital I/O pins are individually configurable as either inputs or as outputs through the GPIOC (GPIO-Configure) register. The GPIOD (GPIO-Data) register controls the level of the pins. When reading the GPIOD register, the data returned are the level of the pins, whether they are programmed as inputs or outputs. As inputs, a write to the GPIOD has no effect. As outputs, a write to the GPIOD sets the output value.

During Standby and Power-Down modes, the GPIO remains active. If configured as inputs, these pins must be driven (do not float). If configured as outputs, the pins are driven. The GPIO pins are set as inputs after power-on or after a reset. Figure 36 shows the GPIO port structure.

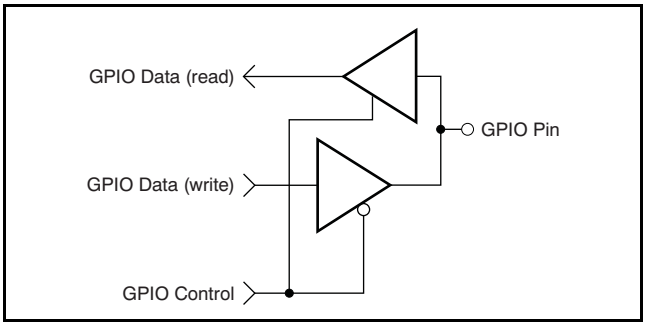


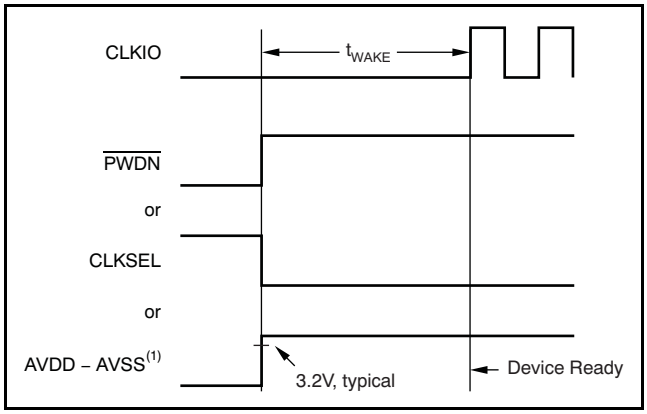
Figure 36. GPIO Port Pin

POWER-DOWN INPUT ($\overline{\text{PWDN}}$)

The $\overline{\text{PWDN}}$ pin controls the power-down mode of the converter. In power-down mode, all internal circuitry is deactivated including the oscillator and the clock output. Hold $\overline{\text{PWDN}}$ low for at least two f_{CLK} cycles to engage power-down. The register settings are retained during power-down. When the pin is returned high, the converter requires a wake-up time before readings can be taken, as shown in the *Power-Up Timing* section. Note that in power-down mode, the inputs of the ADS1158 must continue to be driven and the device continues to drive the outputs.

POWER-UP TIMING

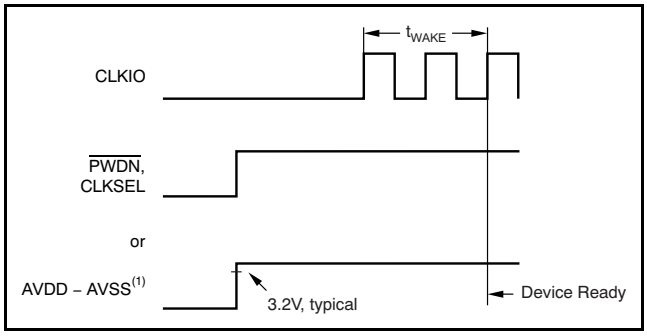
When powering up the device or taking the $\overline{\text{PWDN}}$ pin high to wake the device, a wake-up time is required before readings can be taken. When using the internal oscillator, the wake-up time is composed of the oscillator start-up time and the PLL lock time, and if the supplies are also being powered, there is a reset interval time of 2^{18} f_{CLK} cycles. Note that CLKIO is not valid during the wake-up period, as shown in Figure 37.



(1) Shown with DVDD stable.

Figure 37. Device Wake Time with Internal Oscillator

When using the device with an external clock, the wake-up time is $2/f_{CLK}$ periods when waking up with the $\overline{\text{PWDN}}$ pin and $2^{18}/f_{CLK}$ periods when powering the supplies, all after a valid CLKIO is applied, as shown in Figure 38.



(1) Shown with DVDD stable.

Figure 38. Device Wake Time with External Clock

Table 6 summarizes the wake-up times using the internal oscillator and the external clock operations.

Table 6. Wake-Up Times

CONDITION	t_{WAKE} INTERNAL OSCILLATOR(1)	t_{WAKE} EXTERNAL CLOCK
PWDN or CLKSEL	t_{OSC}	$2/f_{CLK}$
AVDD – AVSS	$t_{OSC} + 2^{18}/f_{CLK}$	$2^{18}/f_{CLK}$

(1) Wake-up times for the internal oscillator operation are typical and may vary depending on crystal characteristics and layout capacitance. The user should verify the oscillator start-up times (t_{OSC} = oscillator start-up time).

POWER-UP SEQUENCE

The analog and digital supplies should be applied before any analog or digital input is driven. The power supplies may be sequenced in any order. The internal master reset signal is generated from the analog power supply (AVDD – AVSS), when the level reaches approximately 3.2V. The power-up master reset signal is functionally the same as the Reset Command and the RESET input pin.

Reset Input ($\overline{\text{RESET}}$)

When $\overline{\text{RESET}}$ is held low for at least two f_{CLK} cycles, all registers are reset to their default values and the digital filter is cleared. When $\overline{\text{RESET}}$ is released high, the device is ready to convert data.

Clock Select Input (CLKSEL)

This pin selects the source of the system clock: the crystal oscillator or an external clock. Tie CLKSEL low to select the crystal oscillator. When using an external clock (applied to the CLKIO pin), tie CLKSEL high.

Clock Input/Output (CLKIO)

This pin serves either as a clock output or clock input, depending on the state of the CLKSEL pin. When using an external clock, apply the clock to this pin and set the CLKSEL pin high. When using the internal oscillator, this pin has the option of providing a clock output. The CLKENB bit of register CONFIG0 enables the clock output (default is enabled).

Start Input (START)

The START pin is an input that controls the ADC process. When the START pin is taken high, the converter starts converting the selected input channels. When the START pin is taken low, the conversion in progress runs to completion and the converter is stopped. The device then enters one of the two idle modes (see the *Idle Modes* section for more details). See the *Conversion Control* section for details of using the START pin.

Data Ready Output ($\overline{\text{DRDY}}$)

The $\overline{\text{DRDY}}$ pin is an output that asserts low to indicate when new channel data are available to read (the previous conversion data are lost). $\overline{\text{DRDY}}$ returns high after the first falling edge of SCLK during a data read operation. If the data are not read (no SCLK pulses), $\overline{\text{DRDY}}$ remains low until new channel data are available once again. $\overline{\text{DRDY}}$ then pulses high, then low to indicate new data are available; see Figure 39.

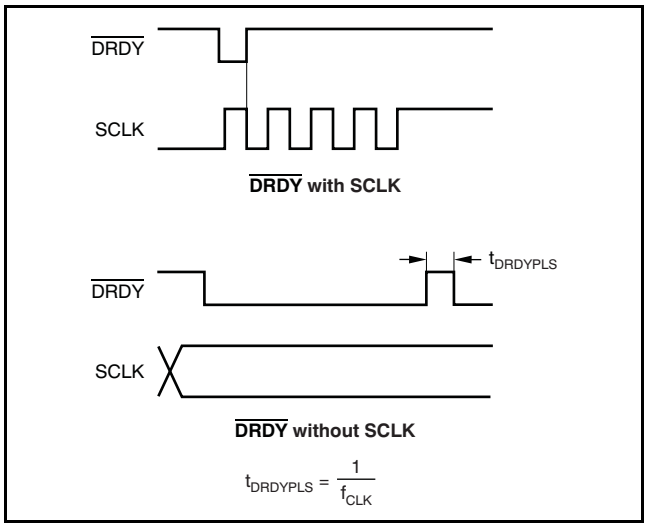


Figure 39. $\overline{\text{DRDY}}$ Timing (See Figure 2 for the $\overline{\text{DRDY}}$ Pulse)

$\overline{\text{DRDY}}$ is usually connected to an interrupt of a controller, DSP, or connected to a controller port pin for polling in a software loop. Channel data can be read without the use of $\overline{\text{DRDY}}$. Read the data using the register format read and check the Status Byte when the NEW bit = 1, which indicates new channel data.

Output Data Scaling and Over-Range

The ADS1158 is scaled such that the output data code resulting from an input voltage equal to $\pm V_{REF}$ has a margin of 6.6% before clipping. This architecture allows operation of applied input signals at or near full-scale without overloading the converter.

Specifically, the device is calibrated so that:

$1LSB = V_{REF}/7800h$,

and the output clips when:

$|V_{IN}| \geq 1.06 \times V_{REF}$.

Table 7 summarizes the ideal output codes versus input signals.

Table 7. Ideal Output Code versus Input Signal

INPUT SIGNAL V_{IN} (ADCINP – ADCINN)	IDEAL OUTPUT CODE(1)	DESCRIPTION
$\geq +1.06 \times V_{REF}$	7FFFh	Maximum positive full-scale before output clipping
$+V_{REF}$	7800h	$V_{IN} = +V_{REF}$
$+1.06 \times V_{REF}/(2^{15} - 1)$	0001h	+1LSB
0	0000h	Bipolar Zero
$-1.06 \times V_{REF}/(2^{15} - 1)$	FFFFh	–1LSB
$-V_{REF}$	87FFh	$V_{IN} = -V_{REF}$
$\leq -1.06 \times V_{REF} \times (2^{15}/2^{15} - 1)$	8000h	Maximum negative full-scale before output clipping

(1) Ideal output code –0.5LSB excludes effects of noise, linearity, offset, and gain errors.

INTERNAL SYSTEM READINGS

Analog Power-Supply Reading (VCC)

The analog power-supply voltage of the ADS1158 can be monitored by reading the VCC register. The supply voltage is routed internal to the ADS1158 and is measured and scaled using an internal reference. The supply readback channel outputs the difference between AVDD and AVSS (AVDD – AVSS), for both single and dual configurations. Note that it is required to disable chopping (CHOP = 0) before taking this reading.

The scale factor of Equation 5 converts the code value to volts:

$$\text{Total Analog Supply Voltage (V)} = \frac{\text{Code}}{\text{12 (0Ch)}} \quad (5)$$

When the power supply falls below the minimum specified operating voltage, the full operation of the ADS1158 cannot be ensured. Note that when the total analog supply voltage falls to below approximately 4.3V, the returned data are set to zero. The SUPPLY bit in the status byte is then set. The bit clears when the total supply voltage rises approximately 50mV higher than the lower trip point.

The digital supply (DVDD) may be monitored by looping-back the supply voltage to an input channel. A resistor divider may be required for bipolar supply operation to reduce the DVDD level to within the range of the analog supply.

Gain Reading (GAIN)

In this configuration, the external reference is connected both to the analog input and to the reference input of the ADC. The data from this register indicate the gain of the device.

The following scale factor (Equation 6) converts the code value to device gain:

$$\text{Device Gain (V/V)} = \frac{\text{Code}}{\text{120 (78h)}} \quad (6)$$

To correct the device gain error, the user software can divide each converter data value by the device gain. Note that this corrects only for gain errors originating within the ADC; system gain errors that occur because of an external gain stage error or because of reference errors are not compensated. Note that it is also required to disable chopping (CHOP = 0) before taking this reading.

Reference Reading (REF)

In this configuration, the external reference is connected to the analog input and an internal reference is connected to the reference of the ADC. The data from this register indicate the magnitude of the external reference voltage.

The scale factor of Equation 7 converts the code value to external reference voltage:

$$\text{External Reference (V)} = \frac{\text{Code}}{\text{12 (0Ch)}} \quad (7)$$

This readback function can be used to check for missing or an out-of-range reference. If the reference input pins are floating (not connected), internal biasing pulls them to the AVSS supply. This pull causes the output code to tend toward '0'. Bypass capacitors connected to the external reference pins may slow the response of the pins when open. When reading this register immediately after power-on, verify that the reference has settled to ensure an accurate reading. Note that it is required to disable chopping (CHOP = 0) before taking this reading.

Temperature Reading (TEMP)

The ADS1158 contains an on-chip temperature sensor. This sensor uses two internal diodes with one diode having a current density of 16x of the other. The difference in current densities of the diodes yields a difference voltage that is proportional to absolute temperature.

As a result of the low thermal resistance of the package to the printed circuit board (PCB), the internal device temperature tracks the PCB temperature closely. Note also that self-heating of the ADS1158 causes a higher reading than the temperature of the surrounding PCB. Note that it is required to disable chopping (CHOP = 0) before taking this reading.

The scale factor of Equation 8 converts the temperature reading to °C. Before using the equation, the temperature reading code must first be scaled to microvolts.

$$\text{Temperature (°C)} = \left(\frac{\text{Temp Reading}(\mu\text{V}) - 168{,}000\mu\text{V}}{394\mu\text{V/°C}} \right) \quad (8)$$

Offset Reading (OFFSET)

The differential output of the multiplexer is shorted together and set to a common-mode voltage of (AVDD – AVSS)/2. Ideally, the code from this register function is 0h, but varies because of the noise of the ADC and offsets stemming from the ADC and external signal conditioning. This register can be used to calibrate or track the offset of the ADS1158 and external signal conditioning. The chop feature of the ADC can automatically remove offset and offset drift from the external signal conditioning; see the *External Chopping* section.

CONVERSION CONTROL

The conversions of the ADS1158 are controlled by the START pin. Conversions begin when the START pin is taken high and conversions are stopped when the START pin is taken low. For continuous conversions, tie the START pin high. The START pin can also be tied low and the conversions controlled by the PULSE convert command. The PULSE convert command converts one channel (only) for each command sent. In this way, channel conversions can be stepped without the need to toggle the START pin.

START Pin

As shown in Figure 40, when the START pin is taken high, conversions start beginning with the current channel. The device continues to convert all of the programmed channels, in a continuous loop, until the START pin is taken low. When this occurs, the conversion in process completes, and the device enters the standby or sleep mode and waits for a new start condition. When $\overline{\text{DRDY}}$ asserts low, the conversion data are ready. Figure 42 shows the START pin to $\overline{\text{DRDY}}$ timing. The order in which channel data are converted is described in Table 9. When the last selected channel in the program list has been converted, the device continues conversions starting with the highest priority channel. If there is only one channel selected in the Auto-Scan mode, the converter remains fixed on one channel. A write operation to any of the multiplexer channel select registers sets the channel pointer to the highest priority channel (see Table 10). In Fixed-Channel mode, the channel pointer remains fixed.

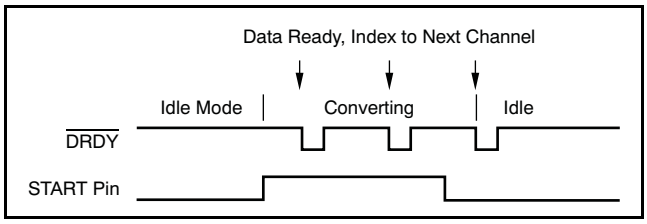


Figure 40. Conversion Control, Auto-Scan Mode

Pulse Convert Command

Figure 41 also shows the start of conversions with the rising edge of the START pin. If the START pin is taken high, and then low before completion of the conversion cycle (8 τ_{CLK} before $\overline{\text{DRDY}}$ asserts low), only the current channel is converted and the device enters the standby or sleep modes and waits for a new start condition. Figure 42 shows the START pin to $\overline{\text{DRDY}}$ timing. The same function of conversion control is possible using the Pulse Convert command (with the START pin low). In this operation, the data from one channel are converted with each Pulse Convert command. The Pulse convert command takes effect when the command byte is completely shifted in (eighth falling edge of SCLK). After conversion, if more than one channel is enabled (Auto-Scan mode), the converter indexes to the next selected channel after completing the conversion.

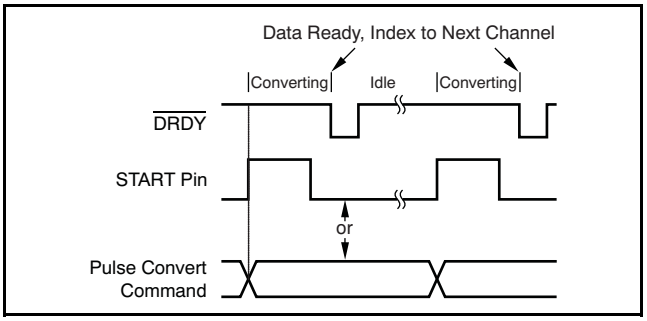
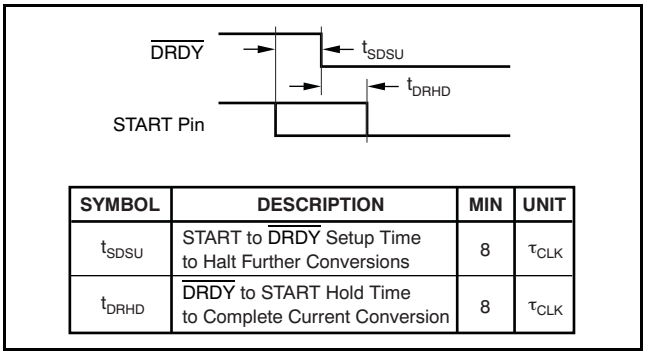


Figure 41. Pulse Conversion, Auto-Scan Mode



SYMBOL	DESCRIPTION	MIN	UNIT
t_{SDSU}	START to $\overline{\text{DRDY}}$ Setup Time to Halt Further Conversions	8	τ_{CLK}
t_{DRHD}	$\overline{\text{DRDY}}$ to START Hold Time to Complete Current Conversion	8	τ_{CLK}

Figure 42. START Pin and $\overline{\text{DRDY}}$ Timing

GPIO Linked START Pin Control

The START pin can be controlled directly by software by connecting externally a GPIO port pin to the START pin. (Note that an external pull-down resistor is recommended to keep the GPIO from floating until the GPIO is configured as an output). For this mode of control, the START pin is effectively controlled by writing to the GPIO Data Register (GPIOD), with the write operation setting or resetting the appropriate bit. The data takes effect on the eighth falling edge of the data byte write. The START pin can then be controlled by the serial interface.

Initial Delay

As seen in Figure 43, when a start convert condition occurs, the first reading from ADS1158 is delayed for a number of clock cycles. This delay allows fully settled data to occur at the first data read. Data reads thereafter are available at the full data rate. The number of clock cycles delayed before the first reading is valid depends on the data rate setting, and whether exiting the Standby or Sleep mode. Table 8 lists the delayed clock cycles versus data rate.

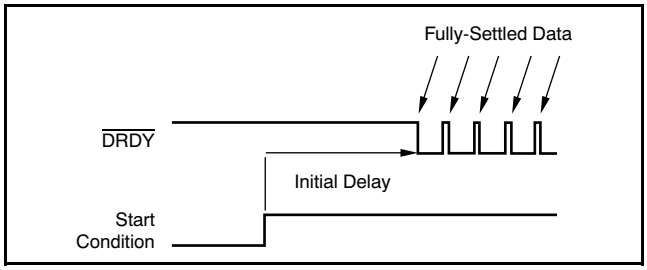


Figure 43. Start Condition to First Data

OPERATING MODES

The operating modes of the ADS1158 are defined in three basic states: Converting mode, Idle mode, and Power-Down mode. In Converting mode, the device is actively converting channel data. The device power dissipation is the highest in this mode. This mode is divided into two sub-modes: Auto-Scan and Fixed-Channel.

The next mode is the Idle mode. In this mode, the device is not converting channel data. The device remains active, waiting for input to start conversions. The power consumption is reduced from that of the Converting mode. This mode also has two sub-modes: Standby and Sleep.

The last mode is Power-Down mode. In this mode, all functions of the converter are disabled to reduce power consumption to a minimum.

CONVERTING MODES

The ADS1158 has two converting modes: Auto-Scan and Fixed-Channel. In Auto-Scan mode, the channels to be measured are pre-selected in the address register settings. When a convert condition is present, the converter automatically measures and sequences through the channels either in a continuous loop or pulse-step fashion, depending on the trigger condition.

In Fixed-Channel mode, the channel address is selected in the address register settings before acquiring channel data. When a convert condition is present, the device converts a single channel, either continuously or in pulse-step fashion, depending on the trigger condition. The data rate in this mode is higher than in Auto-Scan mode because the input channels are not indexed for each reading.

The selection of converting modes is set with bit MUXMOD of register CONFIG0.

Table 8. Start Condition to $\overline{\text{DRDY}}$ Delay, Chop = 0, DLY[2:0] = 000

DRATE[1:0]	INITIAL DELAY (Standby Mode) (f_{CLK} cycles)		INITIAL DELAY (Sleep Mode) (f_{CLK} cycles)	
	Fixed-Channel	Auto-Scan	Fixed-Channel	Auto-Scan
11	802	708	866	772
10	1186	1092	1250	1156
01	2722	2628	2786	2692
00	8866	8772	8930	8836

Auto-Scan Mode

The ADS1158 provides 16 analog inputs that can be configured in combinations of eight differential inputs or 16 single-ended inputs. The device also provides an additional five internal system measurements. Taken together, the device allows a total of 29 possible channel measurements. The converter automatically scans and measures the selected channels, either in a continuous loop or pulse-step fashion, under the control of the START pin or Start command software. The channels are selected for measurement in registers MUXDIF, MUXSG0, MUXSG1, and SYSRED. When any of these registers are written, the internal channel pointer is set to the channel address with the highest priority (see Table 10).

$\overline{\text{DRDY}}$ asserts low when the channel data are ready; see Figure 41 and Figure 40. At the same time, the converter indexes to the next selected channel and, if the START pin is high, starts a new channel conversion. Otherwise, if pulse converting, the device enters the Idle mode.

For example, if channels 3, 4, 7, and 8 are selected for measurement in the list, the ADS1158 converts the channels in that order, skipping all other channels. After channel 8 is converted, the device starts over, beginning at the top of the channel list, channel 3.

The following guidelines can be used when selecting input channels for Auto-Scan measurement:

1. For differential measurements, adjacent input pins (AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, etc.) are pre-set as differential pairs. Even number channels from each pair represent the positive input to the ADC and odd number channels within a pair represent the negative input (for example, AIN0/AIN1: AIN0 is the positive channel, AIN1 is the negative channel.)
2. For single-ended measurements, use AIN0 through AIN15 as single-ended inputs; AINCOM is the shared common input among them. Note: AINCOM does not need to be at ground potential. For example, AINCOM can be tied to VREFP or VREFN; or any potential between (AVSS – 100mV) and (AVDD + 100mV).
3. Combinations of differential, single-ended inputs, and internal system registers can be used in a scan.

Fixed-Channel Mode

In this mode, any of the 16 analog input channels (AIN0–AIN15) can be selected for the positive ADC input and any analog input channels can be selected for the negative ADC input. New channel configurations must be selected by the MUXSCH register before converting a different channel. Note that the AINCOM input and the internal system registers cannot be referenced in this mode.

Idle Modes

When the START pin is taken low, the device completes the conversion of the current channel and then enters one of the Idle modes, Standby or Sleep. In the Standby mode, the internal biasing of the converter is reduced. This state provides the fastest wake-up response when re-entering the run state. In Sleep mode, the internal biasing is reduced further to provide lower power consumption than the Standby mode. This mode has a slower wake-up response when re-entering the Converting mode (see Table 8). Selection of these modes is set under bit IDLMOD of register CONFIG1.

POWER-DOWN MODE

In power-down mode, both the analog and digital circuitry are completely disabled.

SERIAL INTERFACE

The ADS1158 is operated via an SPI-compatible serial interface by writing data to the configuration registers, using commands to control the converter and finally reading back the channel data. The interface consists of four signals: $\overline{\text{CS}}$, SCLK, DIN, and DOUT.

Chip Select ($\overline{\text{CS}}$)

$\overline{\text{CS}}$ is an input that selects the device for serial communication. $\overline{\text{CS}}$ is active low. When $\overline{\text{CS}}$ is high, read or write commands in progress are aborted and the serial interface is reset. Additionally, DOUT goes to a 3-state condition and inputs on DIN are ignored. $\overline{\text{DRDY}}$ indicates when data are ready, independent of $\overline{\text{CS}}$.

The converter may be operated using $\overline{\text{CS}}$ to actively select and deselect the device, or with $\overline{\text{CS}}$ tied low (always selected). $\overline{\text{CS}}$ must stay low for the entire read or write operation. When operating with $\overline{\text{CS}}$ tied low, the number of SCLK pulses must be carefully controlled to avoid false command transmission.

Serial Clock (SCLK) Operation

The serial clock (SCLK) is an input that is used to clock data into (DIN) and out of (DOUT) the ADS1158. This input is a Schmitt-trigger input that has a high degree of noise immunity. However, it is recommended to keep SCLK as clean as possible to prevent glitches from inadvertently shifting the data. Data are shifted into DIN on the rising edge of SCLK and data are shifted out of DOUT on the falling edge of SCLK. If SCLK is held inactive for 4096 or 256 f_{CLK}

cycles (SPIRST bit of register CONFIG0), read or write operations in progress terminate and the SPI interface resets. This timeout feature can be used to recover lost communication when a serial interface transmission is interrupted or inadvertently glitched.

Data Input (DIN) and Data Output (DOUT) Operation

The data input pin (DIN) is used to input data to the ADS1158. The data output pin (DOUT) is used to output data from the ADS1158. Data on DIN is shifted into the converter on the rising edge of SCLK while data are shifted out on DOUT on the falling edge of SCLK. DOUT 3-states when $\overline{CS}$ is high to allow multiple devices to share the line.

SPI Bus Sharing

The ADS1158 can be connected to a shared SPI bus. DOUT 3-states when $\overline{CS}$ is deselected (high). When the ADS1158 is connected to a shared bus, data can be read only by the Channel Data Read command format.

COMMUNICATION PROTOCOL

Communicating with the ADS1158 involves shifting data into the device (via the DIN pin) or shifting data out of the device (via the DOUT pin) under control of the SCLK input.

Reading DATA

$\overline{DRDY}$ goes low to indicate that new conversion data are ready. The data may be read via a direct data read (Channel Data Read Direct) or in a register format (Channel Data Read Register). A direct data read requires the data to be read before the next occurrence of $\overline{DRDY}$ or the data are corrupted. This type of data read requires synchronization with $\overline{DRDY}$ to avoid this conflict. When reading data in the register format, the data may be read at any time without concern to $\overline{DRDY}$. The NEW bit of the STATUS byte indicates that the data register has been refreshed with new converter data since the last read operation. The data are shifted out MSB first after the STATUS byte.

It should be noted that on system power-up, if the ADS1158 interface signals are floating or undefined, the interface could wake in an unknown state. This condition is remedied by resetting the interface in three ways: toggle the $\overline{RESET}$ pin low then high; toggle the $\overline{CS}$ pin high then low; or hold SCLK inactive for $2^{18} + 4096\ f_{CLK}$ cycles.

Channel Data Read Direct

Channel data can be accessed from the ADS1158 in two ways: Direct data read or data read with register format. With Direct read, the DIN input pin is held inactive (high or low) for at least the first three SCLK transitions. When the first three bits are *000* or *111*, the device detects a direct data read and channel data are output. After the device detects this read format, commands are ignored until either $\overline{CS}$ is toggled, an SPI timeout occurs or the device is reset. The Channel Data Read command does not have this requirement.

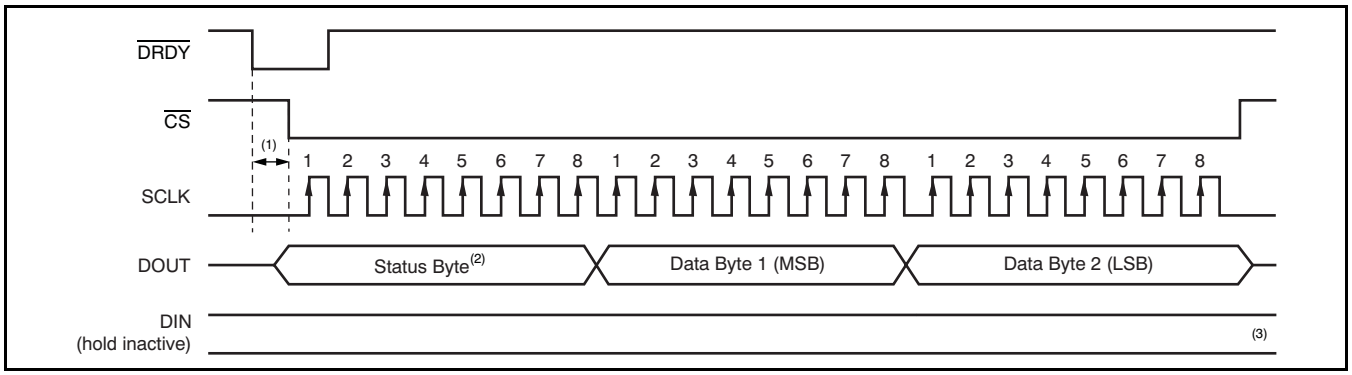
Concurrent with the first SCLK transition, channel data are output on the DOUT output pin. A total of 16 or 24 SCLK transitions complete the data read operation. The number of shifts depend on whether the status byte is enabled. The data must be completely shifted out before the next occurrence of DRDY or the remaining data are corrupted. It is recommended to monitor DRDY to synchronize the start of the read operation to avoid data corruption. Before DRDY asserts low, the MSB of the Status byte or the MSB of the data are output on DOUT (CS = '0'), as shown in Figure 44. In this format, reading the data a second time within the same DRDY frame returns data = 0.

COMMAND DESCRIPTION

Commands may be sent to the ADS1158 with CS tied low. However, after the Channel Data Read Direct operation, it is necessary to toggle CS or an SPI timeout must occur to reset the interface before sending a command.

Channel Data Read Command

To read channel data in this mode (register format), the first three bits of the command byte to be shifted into the device are *001*. The MUL bit must be set because this command is a multiple byte read. The remaining bits are *don't care* but must be clocked to the device. During this time, ignore any data that appear on DOUT until the command completes. These data should be ignored. Beginning with the eighth SCLK falling edge (command byte completed), the MSB of the channel data are restarted on DOUT. The user clocks the data on the following rising edge of SCLK. A total of 32 SCLK transitions complete the data read operation. Unlike the direct read mode, the channel data can be read during a DRDY transition without data corruption. This mode is recommended when DRDY is not used and the data are polled to detect for the occurrence of new data or when CS is tied low to avoid the necessity for an SPI timeout that otherwise occurs when reading data directly. This option avoids conflicts with DRDY, as shown in Figure 45.

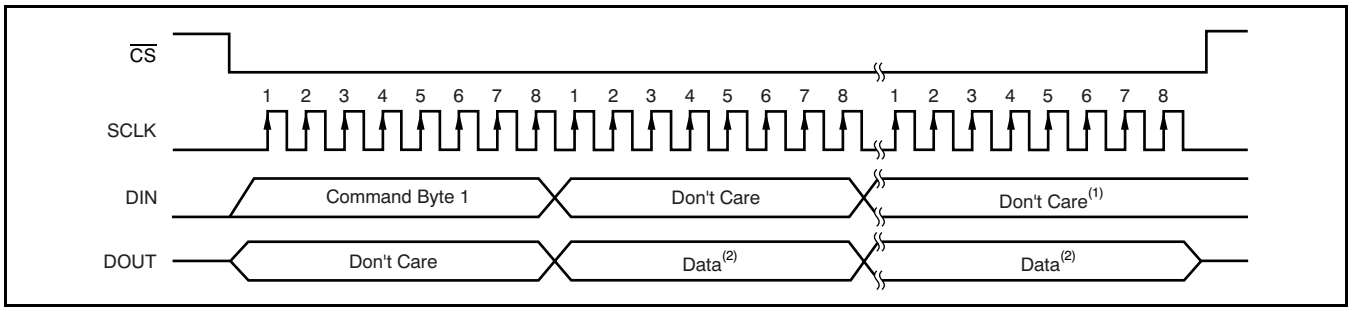


(1) No SCLK activity.

(2) Optional for Auto-Scan mode, disabled for Fixed-Channel mode. See Table 12, Status Byte.

(3) After the channel data read operation, CS must be toggled or an SPI timeout must occur before sending commands.

Figure 44. Channel Data Read Direct (No Command)



(1) After the prescribed number of registers are read, then one or more additional commands can be issued in succession.

(2) Four bytes for channel data register read. See Table 12, Status Byte. One or more bytes for register read, depending on MUL bit.

Figure 45. Register and Channel Data (Register Format) Read

Register Read Command

To read register data, the first three bits of the command byte to be shifted into the device are *010*. These bits are followed by the multiple register read bit (MUL). If MUL = '1', then multiple registers can be read in sequence beyond the desired register. If MUL = '0', only data from the addressed register can be read. The last four bits of the command word are the beginning register address bits. During this time, the invalid data may appear on DOUT until the command is completed. These data should be ignored. Beginning with the eighth falling edge of SCLK (command byte completed), the MSB of the register data are output on DOUT. The remaining eight SCLK transitions complete the read of a single register. If MUL = '1', the data from the next register can be read in sequence by supplying additional SCLKs. The operation terminates when the last register is accessed (address = 09h); see Figure 45.

Register Write Command

To write register data, the first three bits of the command byte to be shifted into the device are *011*. These bits are followed by the multiple register read bit (MUL). If MUL = '1', then multiple registers can be written in sequence beyond the desired register. If MUL = '0', only data to the addressed register can be written. The remaining four bits of the command word are the beginning register address bits. During this time, the invalid data may appear on DOUT until the command is completed. These data should be ignored.

Beginning with the eighth SCLK rising edge (command byte completed), the MSB of the data are shifted in. The remaining seven SCLK rising edges complete the write to a single register. If MUL = '1', the data to the next register can be written by supplying additional SCLKs. The operation terminates when the last register is accessed (address = 09h), as shown in Figure 46.

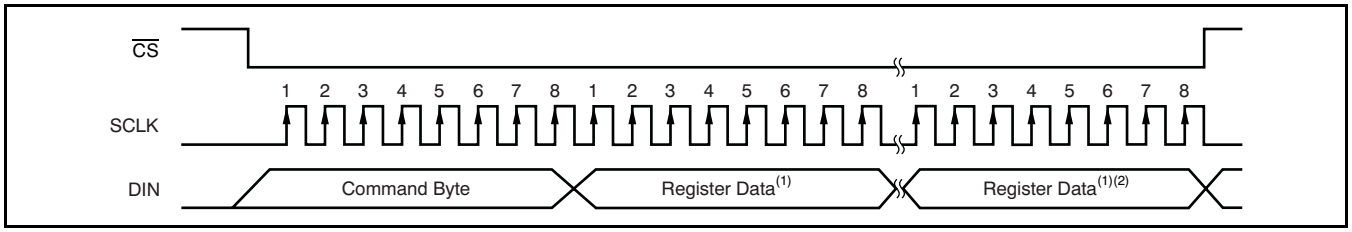
CONTROL COMMANDS

Pulse Convert Command

See *Conversion Control* section.

Reset Command

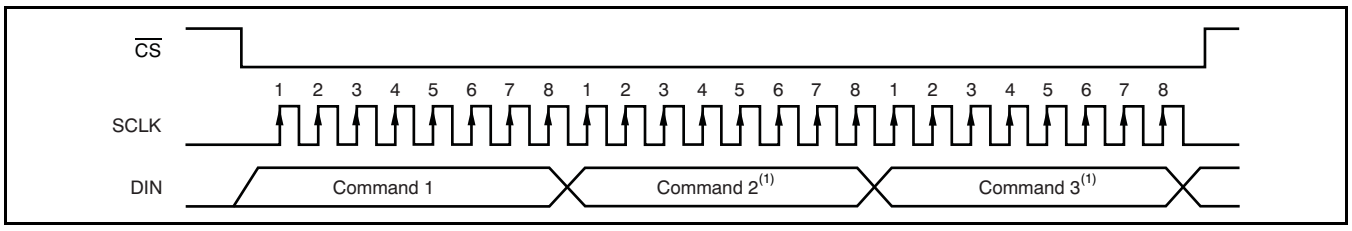
The Reset command resets the ADC. All registers are reset to their default values. A conversion in process continues but will be invalid when completed ($\overline{DRDY}$ low). This conversion data should be discarded. Note that the SPI interface may require reset for this command, or any command, to function. To ensure device reset under a possible locked SPI interface condition, do one of the following: 1) toggle $\overline{CS}$ high then low and send the reset command; or 2) hold SCLK inactive for $256/f_{CLK}$ or $4096/f_{CLK}$ and send the reset command. The control commands are illustrated in Figure 47.



(1) One or more bytes, depending on MUL bit.

(2) After the prescribed number of registers are read, then one or more additional commands can be issued in succession.

Figure 46. Register Write Operation



(1) One or more additional commands can be issued in succession.

Figure 47. Control Command Operation

CHANNEL DATA

The data read operation outputs either three bytes (one byte for status and two bytes for data), or two bytes for data only. The selection of the 3-byte or 2-byte data read is set by the bit STAT in register CONFIG0 (see Table 12, *Status Byte*, for options). In the 3-byte read, the first byte is the status byte and the following two bytes are the data bytes. The MSB (Data15) of the data are shifted out first.

Table 9. CHANNEL DATA FORMAT

BYTE		BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
1	STATUS	NEW	OVF	SUPPLY	CHID4	CHID3	CHID2	CHID1	CHID0
2	MSB	Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8
3	LSB	Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

STATUS BYTE

BIT STATUS.7, NEW

The NEW bit is set when the results of a Channel Data Read Command returns new channel data. The bit remains set indefinitely until the channel data are read. When the channel data are read again before the converter updates with new data, the previous data are output and the NEW bit is cleared. If the channel data are not read before the next conversion update, the data from the previous conversion is lost. As shown in Figure 48, the NEW bit emulates the operation of the $\overline{\text{DRDY}}$ output pin. To emulate the function of the $\overline{\text{DRDY}}$ output pin in software, the user reads data at a rate faster than the converter data rate. The user then polls the NEW bit to detect for new channel data.

0 = Channel data have not been updated since the last read operation.

1 = Channel data have been updated since the last read operation.

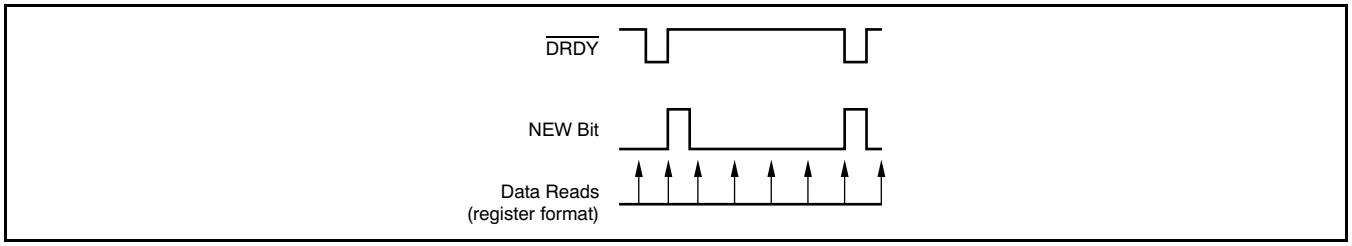


Figure 48. NEW Bit Operation

BIT STATUS.6, OVF

When this bit is set, it indicates that the differential voltage applied to the ADC inputs have exceeded the range of the converter $|V_{IN}| > 1.06\overline{6}V_{REF}$. During over-range, the output code of the converter clips to either positive FS ($V_{IN} \geq 1.06\overline{6} \times V_{REF}$) or negative FS ($V_{IN} \leq -1.06\overline{6} \times V_{REF}$). This bit, with the MSB of the data, can be used to detect positive or negative over-range conditions. Note that because of averaging incorporated within the digital filter, the absence of this bit does not assure that the modulator of the ADC has not saturated as a result of possible transient input overload conditions.

BIT STATUS.5, SUPPLY

This bit indicates that the analog power-supply voltage (AVDD – AVSS) is below a preset limit. The SUPPLY bit is set when the value falls below 4.3V (typically) and is reset when the value rises 50mV higher (typically) than the lower trip point. The output data of the ADC may not be valid under low power-supply conditions.

BITS CHID[4:0] CHANNEL ID BITS

The Channel ID bits indicate the measurement channel of the acquired data. Note that for Fixed-Channel mode, the Channel ID bits are undefined. See Table 10 for the channel ID, the measurement priority, and the channel description for Auto-Scan Mode.

BITS DATA[15:0] OF DATA BYTES

The ADC output data are 16 bits wide (DATA[15:0]). DATA15 is the most significant bit (MSB) and DATA0 is the least significant bit (LSB). The data are coded in binary twos complement (BTC) format.

Table 10. Channel ID and Measurement Order (Auto-Scan Mode)

BITS CHID[4:0]	PRIORITY	CHANNEL	DESCRIPTION
00h	1 (highest)	DIFF0 (AIN0–AIN1)	Differential 0
01h	2	DIFF1 (AIN2–AIN3)	Differential 1
02h	3	DIFF2 (AIN4–AIN5)	Differential 2
03h	4	DIFF3 (AIN6–AIN7)	Differential 3
04h	5	DIFF4 (AIN8– AIN9)	Differential 4
05h	6	DIFF5 (AIN10–AIN11)	Differential 5
06h	7	DIFF6 (AIN12–AIN13)	Differential 6
07h	8	DIFF7 (AIN14–AIN15)	Differential 7
08h	9	AIN0	Single-ended 0
09h	10	AIN1	Single-ended 1
0Ah	11	AIN2	Single-ended 2
0Bh	12	AIN3	Single-ended 3
0Ch	13	AIN4	Single-ended 4
0Dh	14	AIN5	Single-ended 5
0Eh	15	AIN6	Single-ended 6
0Fh	16	AIN7	Single-ended 7
10h	17	AIN8	Single-ended 8
11h	18	AIN9	Single-ended 9
12h	19	AIN10	Single-ended 10
13h	20	AIN11	Single-ended 11
14h	21	AIN12	Single-ended 12
15h	22	AIN13	Single-ended 13
16h	23	AIN14	Single-ended 14
17h	24	AIN15	Single-ended 15
18h	25	OFFSET	OFFSET
1Ah	26	VCC	AVDD – AVSS supplies
1Bh	27	TEMP	Temperature
1Ch	28	GAIN	Gain
1Dh	29 (lowest)	REF	External reference

COMMAND AND REGISTER DEFINITIONS

Commands are used to read channel data, access the configuration registers, and control the conversion process. If the command is a register read or write operation, one or more data bytes follow the command byte. If bit MUL = 1 in the command byte, then multiple registers can be read or written in one command operation (see the MUL bit). Commands can be sent back-to-back without toggling $\overline{CS}$; however, after a channel Data Read Direct operation, $\overline{CS}$ must be toggled or an SPI timeout must occur before sending a command. The data read by command does not require $\overline{CS}$ to be toggled.

The command byte consists of three fields: the Command Bits(C[2:0]), multiple register access bit (MUL), and the Register Address Bits (A[3:0]); see the Command Byte register.

Command Byte

7	6	5	4	3	2	1	0
C2	C1	C0	MUL	A3	A2	A1	A0

Bits C[2:0]—Command Bits

These bits code the command within the command byte.

C[2:0]	DESCRIPTION	COMMENTS
000	Channel data read direct (no command)	Toggle $\overline{CS}$ or allow SPI timeout before sending command
001	Channel data read command (register format)	Set MUL = 1; status byte always included in data
010	Register read command	
011	Register write command	
100	Pulse convert command	MUL, A[3:0] are don't care
101	Reserved	
110	Reset command	MUL, A[3:0] don't care
111	Channel data read direct (no command)	Toggle $\overline{CS}$ or allow SPI timeout before sending command

Bit 4 MUL: Multiple Register Access

0 = Disable Multiple Register Access

1 = Enable Multiple Register Access

This bit enables the multiple register access. This option allows writing or reading more than one register in a single command operation. If only one register is to be read or written, set MUL = '0'. For multiple register access, set MUL = '1'. The read or write operation begins at the addressed register. The ADS1158 automatically increments the register address for each register data byte subsequently read or written. The multiple register read or write operations complete after register address = 09h (device ID register) has been accessed.

The multiple register access is terminated in one of three ways:

1. The user takes $\overline{CS}$ high. This action resets the SPI interface.
2. The user holds SCLK inactive for 4096 f_{CLK} cycles. This action resets the SPI interface.
3. Register address = 09h has been accessed. This completes the command and the ADS1158 is then ready for a new command. Note for the Channel Data Read command, this bit must be set to read the three data bytes (one status byte and two data bytes).

A[3:0] Register Address Bits

These bits are the register addresses for a register read or write operation; see Table 11.

REGISTERS

Table 11. Register Map

ADDRESS Bits A[3:0]	REGISTER NAME	DEFAULT VALUE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
00h	CONFIG0	0Ah	0	SPIRST	MUXMOD	BYPAS	CLKENB	CHOP	STAT	0
01h	CONFIG1	83h	IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0
02h	MUXSCH	00h	AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0
03h	MUXDIF	00h	DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0
04h	MUXSG0	FFh	AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0
05h	MUXSG1	FFh	AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8
06h	SYSRED	00h	0	0	REF	GAIN	TEMP	VCC	0	OFFSET
07h	GPIOC	FFh	CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0
08h	GPIOD	00h	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
09h	ID	8Bh	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

CONFIG0: CONFIGURATION REGISTER 0 (Address = 00h)

7	6	5	4	3	2	1	0
0	SPIRST	MUXMOD	BYPAS	CLKENB	CHOP	STAT	0

Default = 0Ah.

Bit 7 **Must be 0** (default)

Bit 6 **SPIRST SPI Interface Reset Timer**

This bit sets the number of f_{CLK} cycles in which SCLK is inactive until the SPI interface resets. This bit places a lower limit on the frequency of SCLK in which to read or write data to the device. The SPI interface only is reset and not the device itself. When the SPI interface is reset, it is ready for a new command.

0 = Reset when SCLK inactive for $4096f_{CLK}$ cycles (256µs, f_{CLK} = 16MHz) (default).

1 = Reset when SCLK inactive for $256f_{CLK}$ cycles (16µs, f_{CLK} = 16MHz).

Bit 5 **MUXMOD**

This bit sets either the Auto-Scan or Fixed-Channel mode of operation.

0 = Auto-Scan mode (default)

In Auto-Scan mode, the input channel selections are eight differential channels (DIFF0–DIFF7) and 16 single-ended channels (AIN0–AIN15). Additionally, five internal monitor readings can be selected. These selections are made in registers MUXDIF, MUXSG0, MUXSG1, and SYSRED. In this mode, settings in register MUXSCH have no effect. See the *Auto-Scan Mode* section for more details.

1 = Fixed-Channel mode

In Fixed-Channel mode, any of the analog input channels may be selected for the positive measurement and the negative measurement channels. The inputs are selected in register MUXSCH. In this mode, registers MUXDIF, MUXSG0, MUXSG1, and SYSRED have no effect. Note that it is not possible to select the internal monitor readings in this mode.

Bit 4 **BYPAS**

This bit selects either the internal or external connection from the multiplexer output to the ADC input.

0 = ADC inputs use internal multiplexer connection (default).

1 = ADC inputs use external ADC inputs (ADCINP and ADCINN).

Note that the Temperature, V_{CC}, Gain, and Reference internal monitor readings automatically use the internal connection, regardless of the BYPAS setting. The Offset reading uses the setting of BYPAS.

Bit 3 **CLKENB**
This bit enables the clock output on pin CLKIO. The clock output originates from the device crystal oscillator and PLL circuit.
0 = Clock output on CLKIO disabled.
1 = Clock output on CLKIO enabled (default).
Note: If the CLKSEL pin is set to '1', the CLKIO pin is a clock input only. In this case, setting this bit has no effect.

Bit 2 **CHOP**
This bit enables the chopping feature on the external multiplexer loop.
0 = Chopping disabled (default)
1 = Chopping enabled
The chopping feature corrects for offset originating from components used in the external multiplexer loop; see the *External Chopping* section.
Note that for Internal System readings (Temperature, VCC, Gain, and Reference), the CHOP bit must be 0.

Bit 1 **STAT** Status Byte Enable
When reading channel data from the ADS1158, a status byte is normally included with the conversion data. However, in some ADS1158 operating modes, the status byte can be disabled. Table 12, Status Byte, shows the modes of operation and the data read formats in which the status byte can be disabled.
0 = Status byte disabled
1 = Status byte enabled (default)

Table 12. Status Byte

MODE	CHANNEL DATA READ COMMAND	CHANNEL DATA READ DIRECT
Auto-Scan	Always enabled	Enabled/disabled by STAT bit
Fixed-Channel	Always enabled (byte is undefined)	Always disabled

Bit 0 Must be 0

CONFIG1: CONFIGURATION REGISTER 1 (Address = 01h)

7	6	5	4	3	2	1	0
IDLMOD	DLY2	DLY1	DLY0	SBCS1	SBCS0	DRATE1	DRATE0

Default = 83h.

Bit 7 IDLMOD

This bit selects the Idle mode when the device is not converting, Standby or Sleep. The Sleep mode offers lower power consumption but has a longer wake-up time to re-enter the run mode; see the *Idle Modes* section.

0 = Select standby mode

1 = Select sleep mode (default)

Bits 6–4 DLY[2:0]

These bits set the amount of time the converter delays after indexing to a new channel but before starting a new conversion. This value should be set large enough to allow for the full settling of external filtering or buffering circuits used between the MUXOUTP, MUXOUTN, and ADCINP, ADCINN pins; see the *Switch Time Delay* section. (default = 000)

Bits 3–2 SBCS[1:0]

These bits set the sensor bias current source.

0 = Sensor bias current source off (default)

1 = 1.5µA source

3 = 24µA source

Bits 1–0 DRATE[1:0]

These bits set the data rate of the converter. Slower reading rates yield increased resolution. The actual data rates shown in the table can be slower, depending on the use of Switch Time Delay or the Chop feature. See the *Switch Time Delay* section. The reading rate scales with the master clock frequency.

DRATE[1:0]	DATA RATE AUTO-SCAN MODE (SPS)	DATA RATE FIXED-CHANNEL MODE (SPS)
11	23739	125000
10	15123	31250
01	6168	7813
00	1831	1953

f_{CLK} = 16MHz, Chop = 0, Delay = 0.

MUXSCH: MULTIPLEXER FIXED-CHANNEL REGISTER (Address = 02h)

7	6	5	4	3	2	1	0
AINP3	AINP2	AINP1	AINP0	AINN3	AINN2	AINN1	AINN0

Default = 00h.

This register selects the input channels of the multiplexer to be used for the Fixed-Channel mode. The MUXMOD bit in register CONFIG0 must be set to '1'. In this mode, bits AINN[3:0] select the analog input channel for the negative ADC input, and bits AINP[3:0] select the analog input channel for the positive ADC input. See the *Fixed-Channel Mode* section.

MUXDIF: MULTIPLEXER DIFFERENTIAL INPUT SELECT REGISTER (Address = 03h)

7	6	5	4	3	2	1	0
DIFF7	DIFF6	DIFF5	DIFF4	DIFF3	DIFF2	DIFF1	DIFF0

Default = 00h.

MUXSG0: MULTIPLEXER SINGLE-ENDED INPUT SELECT REGISTER 0 (Address = 04h)

7	6	5	4	3	2	1	0
AIN7	AIN6	AIN5	AIN4	AIN3	AIN2	AIN1	AIN0

Default = FFh.

MUXSG1: MULTIPLEXER SINGLE-ENDED INPUT SELECT REGISTER 1 (Address = 05h)

7	6	5	4	3	2	1	0
AIN15	AIN14	AIN13	AIN12	AIN11	AIN10	AIN9	AIN8

Default = FFh.

SYSRED: SYSTEM READING SELECT REGISTER (Address = 06h)

7	6	5	4	3	2	1	0
0	0	REF	GAIN	TEMP	VCC	0	OFFSET

Default = 00h.

These four registers select the input channels and the internal readings for measurement in Auto-Scan mode. For differential channel selections (DIFF0…DIFF7), adjacent input pins (AIN0/AIN1, AIN2/AIN3, etc.) are pre-set as differential inputs. All single-ended inputs are measured with respect to the AINCOM input. AINCOM may be set to any level within ±100mV of the analog supply range. Channels not selected are skipped in the measurement sequence. Writing to any of these four registers resets the internal channel pointer to the channel with the highest priority (see Table 10). Note that the bits indicated as '0' must be set to 0.

0 = Channel not selected within a reading sequence.

1 = Channel selected within a reading sequence.

GPIOC: GPIO CONFIGURATION REGISTER (Address = 07h)

7	6	5	4	3	2	1	0
CIO7	CIO6	CIO5	CIO4	CIO3	CIO2	CIO1	CIO0

Default = FFh.

This register configures the GPIO pins as inputs or as outputs. Note that the default configurations of the port pins are inputs and as such they should not be left floating. See the *GPIO Digital Port* section.
0 = GPIO is an output; 1 = GPIO is an input (default).

CIO[7:0] GPIO Configuration

bit 7 **CIO7**, digital I/O configuration bit for pin GPIO7
bit 6 **CIO6**, digital I/O configuration bit for pin GPIO6
bit 5 **CIO5**, digital I/O configuration bit for pin GPIO5
bit 4 **CIO4**, digital I/O configuration bit for pin GPIO4
bit 3 **CIO3**, digital I/O configuration bit for pin GPIO3
bit 2 **CIO2**, digital I/O configuration bit for pin GPIO2
bit 1 **CIO1**, digital I/O configuration bit for pin GPIO1
bit 0 **CIO0**, digital I/O configuration bit for pin GPIO0

GPIOD: GPIO DATA REGISTER (Address = 08h)

7	6	5	4	3	2	1	0
DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

Default = 00h.

This register is used to read and write data to the GPIO port pins. When reading this register, the data returned corresponds to the state of the GPIO external pins, whether they are programmed as inputs or as outputs. As outputs, a write to the GPIOD sets the output value. As inputs, a write to the GPIOD has no effect. See the *GPIO Digital Port* section.
0 = GPIO is logic low (default); 1 = GPIO is logic high.

DIO[7:0] GPIO Data

bit 7 **DIO7**, digital I/O data bit for pin GPIO7
bit 6 **DIO6**, digital I/O data bit for pin GPIO6
bit 5 **DIO5**, digital I/O data bit for pin GPIO5
bit 4 **DIO4**, digital I/O data bit for pin GPIO4
bit 3 **DIO3**, digital I/O data bit for pin GPIO3
bit 2 **DIO2**, digital I/O data bit for pin GPIO2
bit 1 **DIO1**, digital I/O data bit for pin GPIO1
bit 0 **DIO0**, digital I/O data bit for pin GPIO0

ID: DEVICE ID REGISTER (Address = 09h)

7	6	5	4	3	2	1	0
ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Default = 8Bh.

ID[7:0] ID bits

Factory-programmed ID bits. Read-only.

APPLICATION INFORMATION

HARDWARE CONSIDERATIONS

The following summarizes the design and layout considerations when using the ADS1158:

a. **Power Supplies**: The converter accepts a single +5V supply (AVDD = +5V and AVSS = AGND) or dual, bipolar supplies (typically AVDD = +2.5V, AVSS = –2.5V). Dual supply operation accommodates true bipolar input signals, within a ±2.5V range. Note that the maximum negative input voltage to the multiplexer is limited to AVSS – 100mV, and the maximum positive input voltage is limited to AVDD + 100mV. The range for the digital power supply (DVDD) is 2.7V to 5.25V. For all supplies, use a 10µF tantalum capacitor, bypassed with a 0.1µF ceramic capacitor, placed close to the device pins. Alternatively, a single 10µF ceramic capacitor can be used. The supplies should be relatively free from noise and should not be shared with devices that produce voltage spikes (such as relays, LED display drivers, etc.). If a switching power supply is used, the voltage ripple should be low (< 2mV). The analog and digital power supplies may be sequenced in any order.

b. **Analog (Multiplexer) Inputs**: The 16-channel analog input multiplexer can accommodate 16 single-ended inputs, eight differential input pairs, or combinations of either. These options permit freedom in choosing the input channels. The channels do not have to be used consecutively. Unassigned channels are skipped by the device. In the Fixed-Channel mode, any of the analog inputs (AIN0 to AIN15) can be addressed for the positive input and for the negative input. The full-scale range of the device is $2.1\overline{3}V_{REF}$, but the absolute analog input voltage is limited to 100mV beyond the analog supply rails. Input signals exceeding the analog supply rails (for example, ±10V) must be divided prior to the multiplexer inputs.

c. **Input Overload Protection**: Overdriving the multiplexer inputs may affect the conversions of other channels. In the case of input overload, external Schottky diode clamps and series resistor are recommended, as shown in Figure 49.

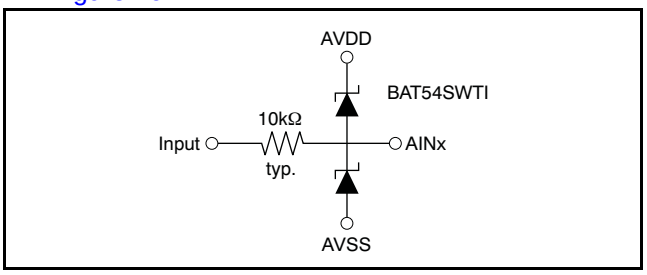


Figure 49. Input Overload Protection

d. **ADC Inputs**: The external multiplexer loop of the ADS1158 allows for the inclusion of signal conditioning between the output of the multiplexer and the input of the ADC. Typically, an amplifier provides gain, buffering, and/or filtering to the input signal. For best performance, the ADC inputs should be driven differentially. A differential in/differential out or a single-ended-to-differential driver is recommended. If the driver uses higher supply voltages than the device itself (for example, ±15V), attention should be paid to power-supply sequencing and potential over-voltage fault conditions. Protection resistors and/or external clamp diodes may be used to protect the ADC inputs. A 1nF or higher capacitor should be used directly across the ADC inputs.

e. **Reference Inputs**: It is recommended to use a 10µF tantalum capacitor with a 0.1µF ceramic capacitor directly across the reference pins, VREFP and VREFN. The reference inputs should be driven by a low-impedance source. For rated performance, the reference should have less than $3\mu V_{RMS}$ broadband noise. For references with higher noise, external filtering may be necessary. Note that when exiting the sleep mode, the device begins to draw a small current through the reference pins. Under this condition, the transient response of the reference driver should be fast enough to settle completely before the first reading is taken, or simply discard the first several readings.

f. **Clock Source**: The ADS1158 requires a clock signal for operation. The clock can originate from either the crystal oscillator or from an external clock source. The internal oscillator uses a PLL circuit and an external 32.768kHz crystal to generate a 15.7MHz master clock. The PLL requires a 22nF capacitor from the PLLCAP pin to AVSS. The crystal and load capacitors should be placed close to the pins as possible and kept away from other traces with ac components. A buffered output of the 15.7MHz clock can be used to drive other converters or controllers. An external clock source can be used up to 16MHz. For best performance, the clock of the SPI interface controller and the converter itself should be on the same *domain*. This configuration requires that the ratio of the SCLK to device clock must be limited to 1,1/2,1/4, 1/8, etc.

g. **Digital Inputs**: It is recommended to source terminate the digital inputs and outputs of the device with a 50Ω (typical) series resistor. The resistors should be placed close to the driving end of the source (output pins, oscillator, logic gates, DSP, etc). This placement helps to reduce the ringing and overshoot on the digital lines.

h. **Hardware Pins**: START, $\overline{\text{DRDY}}$, $\overline{\text{RESET}}$, and PWDN. These pins allow direct pin control of the ADS1158. The equivalent of the START and $\overline{\text{DRDY}}$ pins is provided via commands through the SPI interface; these pins may be left unused. The device also has a $\overline{\text{RESET}}$ command. The PWDN pin places the ADC into very low-power state where the device is inactive.

i. **SPI Interface**: The ADS1158 has an SPI-compatible interface. This interface consists of four signal lines: SCLK, DIN, DOUT, and $\overline{\text{CS}}$. When $\overline{\text{CS}}$ is high, the DIN input is ignored and the DOUT output 3-states. See *Chip Select ($\overline{CS}$)* for more details. The SPI interface can be operated in a minimum configuration without the use of $\overline{\text{CS}}$ (tie $\overline{\text{CS}}$ low; see the *Serial Interface* and *Communication Protocol* sections).

j. **GPIO**: The ADS1158 has eight, user-programmable digital I/O pins. These pins are controlled by register settings. The register setting is default to inputs. If these pins are not used, tie them high or low (do not float input pins) or configure them as outputs.

k. **QFN Package**: See Application Note SLUA271, *QFN/SON PCB Attachment for PCB layout recommendations*, available for download at www.ti.com. The exposed thermal pad of the ADS1158 should be connected electrically to AVSS.

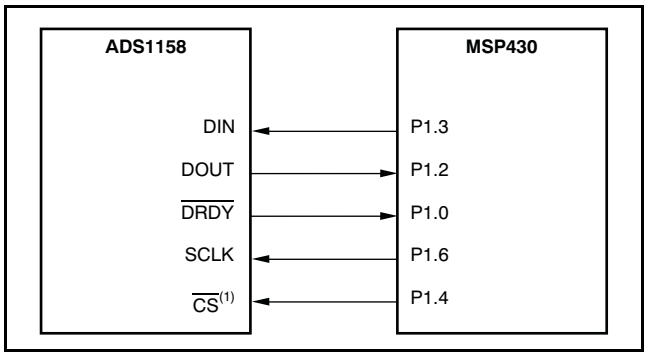
CONFIGURATION GUIDE

Configuration of the ADS1158 involves setting the configuration registers via the SPI interface. After the device is configured for operation, channel data are read from the device through the same SPI interface. The following procedure is recommended to configure the device:

1. **Reset the SPI Interface**: Before using the SPI interface, it may be necessary to recover the SPI interface. To reset the interface, set $\overline{\text{CS}}$ high or disable SCLK for 4096 (256) f_{CLK} cycles.
2. **Stop the Converter**: Set the START pin low to stop the converter. Although not necessary for configuration, this command stops the channel scanning sequence which then points to the first channel after configuration.
3. **Reset the Converter**: The reset pin can be pulsed low or a Reset command can be sent. Although not necessary for configuration, reset re-initializes the device into a known state.
4. **Configure the Registers**: The registers are configured by writing to them either sequentially or as a group. The user may configure the software in either mode. Any write to the Auto-Scan channel-select registers resets the channel pointer to the channel of highest priority.
5. **Verify Register Data**: The register data may be read back for verification of device communications.
6. **Start the Converter**: The converter can be started with the START pin or with a Pulse Convert command sent through the interface.
7. **Read Channel Data**: The $\overline{\text{DRDY}}$ asserts low when data are ready. The channel data can be read at that time. If $\overline{\text{DRDY}}$ is not used, the updated channel data can be checked by reading the NEW bit in the status byte. The status byte also indicates the origin of the channel data. If the data for a given channel is not read before $\overline{\text{DRDY}}$ asserts low again, the data for that channel is lost and replaced with new channel data.

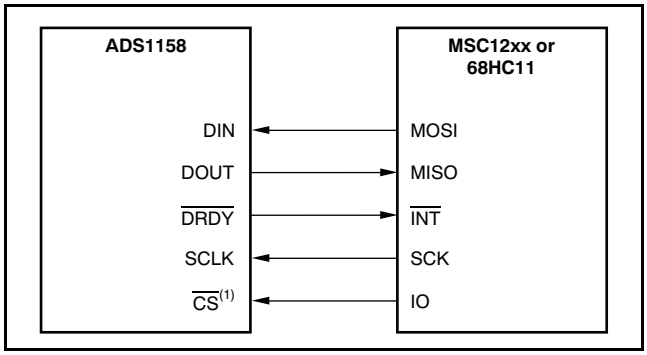
DIGITAL INTERFACE CONNECTIONS

The ADS1158 SPI-compatible interface easily connects to a wide variety of microcontrollers and DSPs. Figure 50 shows the basic connection to TI's MSP430 family of low-power microcontrollers. Figure 51 shows the connection to microcontrollers with an SPI interface such as the 68HC11 family, or TI's MSC12xx family. Note that the MSC12xx includes a high-resolution ADC; the ADS1158 can be used to provide additional channels of measurement or add higher-speed connections. Finally, Figure 52 shows how to connect the ADS1158 to a TMS320x DSP.



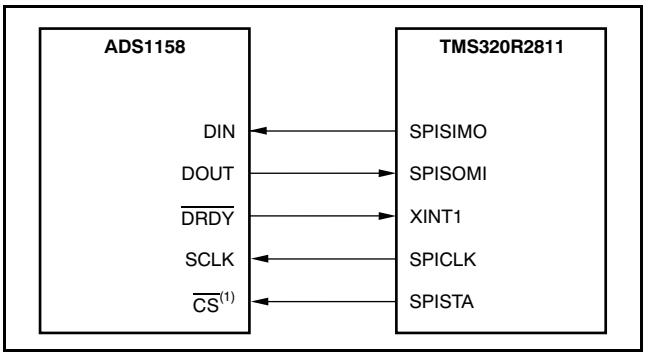
(1) $\overline{CS}$ may be tied low.

Figure 50. Connection to MSP430 Microcontroller



(1) $\overline{CS}$ may be tied low.

Figure 51. Connection to Microcontrollers with an SPI Interface



(1) $\overline{CS}$ may be tied low.

Figure 52. Connection to TMS320R2811 DSP

GPIO Connections

The ADS1158 has eight GPIO pins. Each pin can be configured as an input or an output. Note that pins configured as inputs should not float. The pins can be used to read key pads, drive LED indicator, etc., by reading and writing the GPIO data register (GPIOD). See Figure 53.

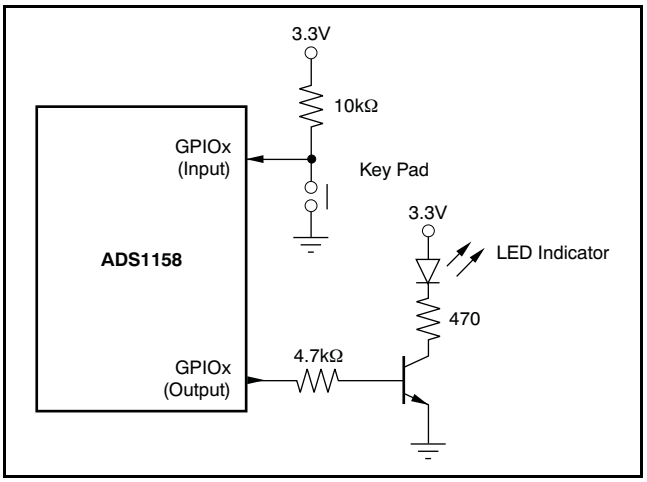


Figure 53. GPIO Connections

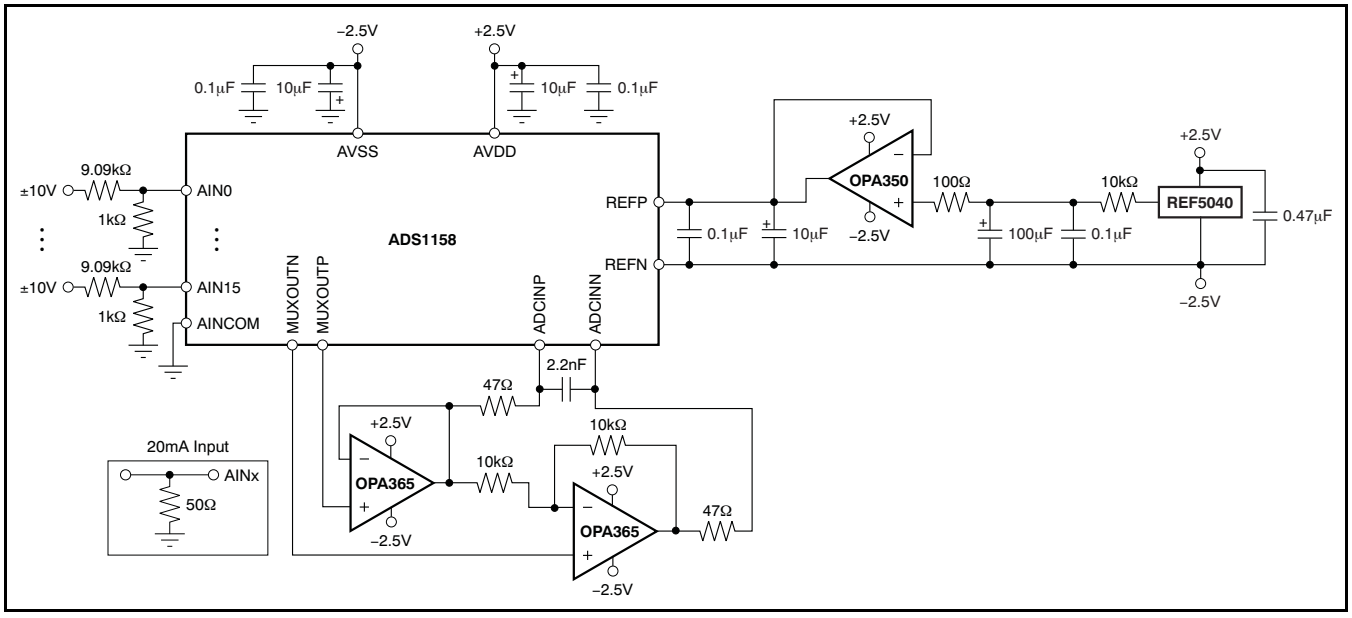
ANALOG INPUT CONNECTIONS

Figure 54 shows the ADS1158 interfacing to high-level ±10V inputs, commonly used in industrial environments. In this case, bipolar power supplies are used to avoid the need for input signal level-shifting that is otherwise required with a single supply. The input resistors serve both to reduce the level of the 10V input signal to within the ADC range and also protect the inputs from inadvertent signal over-voltage up to 30V. The external amplifiers convert the single-ended inputs to a fully differential output to drive the ADC inputs. Driving the inputs differentially maintains good linearity performance. The 2.2nF capacitor at the ADC inputs is required to bypass the ADC sampling currents. The 2.5V reference, REF3125, is filtered and buffered to provide a low-noise reference input to the ADC. The chop feature of the ADC can be used to reduce offset and offset drift of the amplifiers.

For ±1V input signals, the input resistor divider can be removed and replaced with a series protection resistor. For 20mA input signals, the input resistor divider is replaced by a 50Ω resistor, connected from each input to AINCOM.

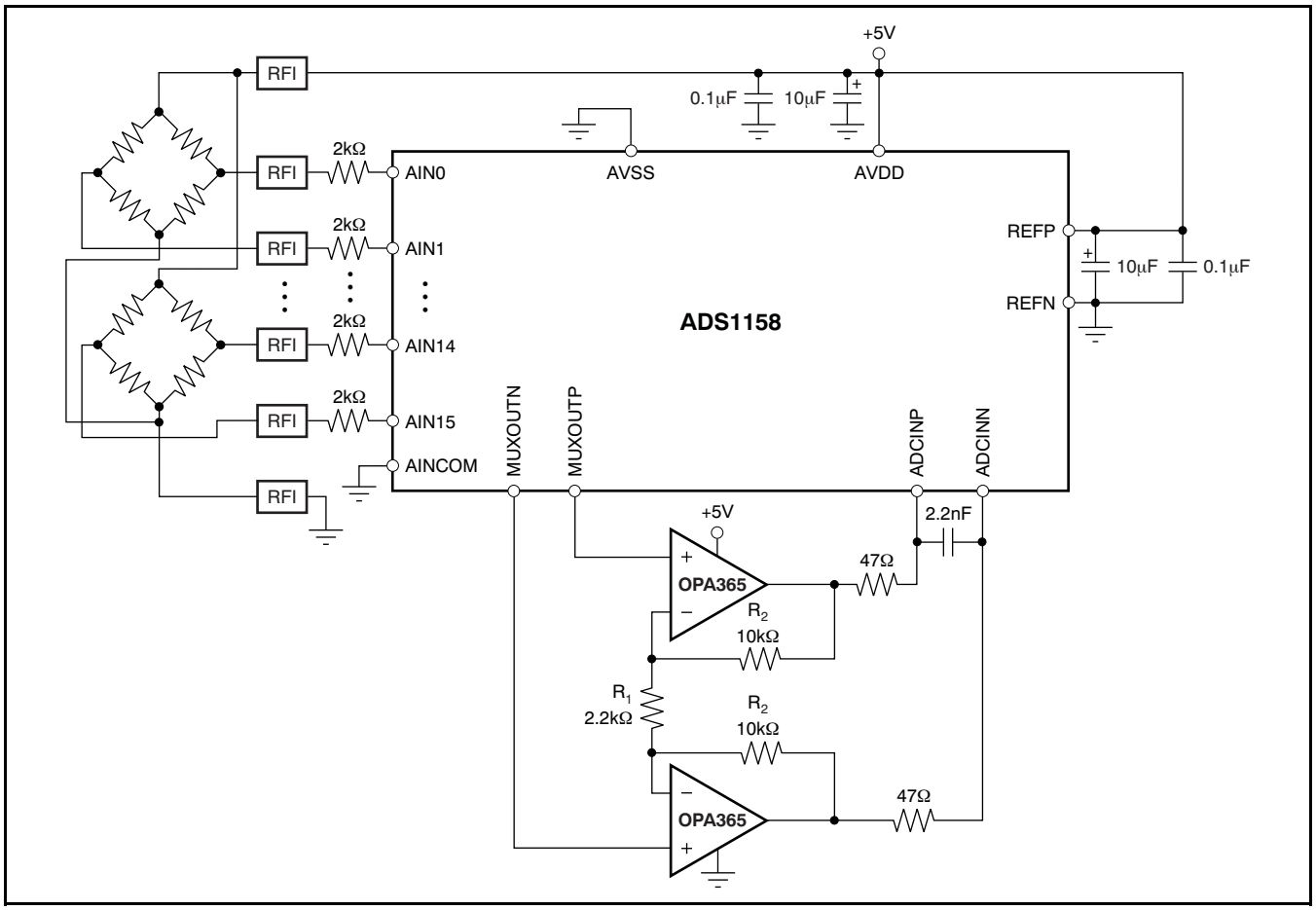
When using Auto-Scan mode to sequence through the channels, the switch time delay feature (programmable by registers) can be used to provide additional settling time of the external components.

Figure 55 illustrates the ADS1158 interfacing to multiple pressure sensors that have a resistor bridge output. Each sensor is excited by the +5V single supply that also powers the ADS1158, and likewise is used as the ADS1158 reference input; the 6% input overrange capability accommodates input levels at or above V_{REF}. The ratiometric connection provides cancellation of excitation voltage drift and noise. For best performance, the +5V supply should be free from glitches or transients. The 5V supply input amplifiers (two OPA365s) form a differential input/differential output buffer with the gain set to 10. The chop feature of the ADS1158 is used to reduce offset and offset drift to very low levels. The 2.2nF capacitor at the ADC inputs is required to bypass the ADC sampling currents. The 47Ω resistors isolate the operational amplifier outputs from the filter capacitor.



NOTE: 0.1µF capacitors not shown.

Figure 54. Multichannel, ±10V Single-Ended Input, Bipolar Supply Operation



NOTE: G = 1 + $2R_2/R_1$. 0.1μF supply bypass capacitor not shown.

Figure 55. Bridge Input, Single-Supply Operation

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June 2008) to Revision A **Page**

- Corrected typical specification value for offset error in Electrical Characteristics table from 0.5LSB to –0.5LSB 3
- Changed offset drift specification parameters in Electrical Characteristics table; combined *chopping on* and *chopping off* specifications. Changed typical value from 0.5µV/°C to 1µV/°C..... 3
- Corrected typical specification value for gain drift in Electrical Characteristics table from 0.4ppm/°C to 2ppm/°C 3
- Changed typical noise specification in Electrical Characteristics table from $0.4LSB_{(PP)}$ to $0.6LSB_{(PP)}$..... 3
- Corrected maximum value for AVDD, AVSS supply current under power-down conditions in Electrical Characteristics table from 85µA to 200µA..... 4
- Added Figure 18, *Power-Down Current vs Temperature (Unipolar)* 10
- Added Figure 19, *Power-Down Current vs Temperature (Bipolar)*..... 10

PACKAGE OPTION ADDENDUM

11-Jul-2008

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS1158IRTCR	ACTIVE	QFN	RTC	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1158IRTCRG4	ACTIVE	QFN	RTC	48	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1158IRTCT	ACTIVE	QFN	RTC	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS1158IRTCTG4	ACTIVE	QFN	RTC	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

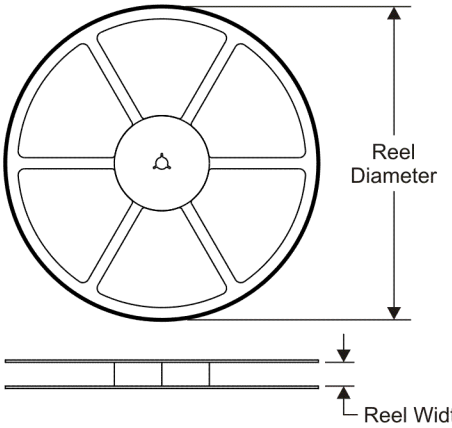
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

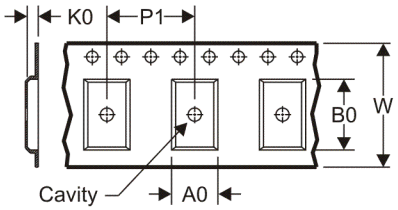
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

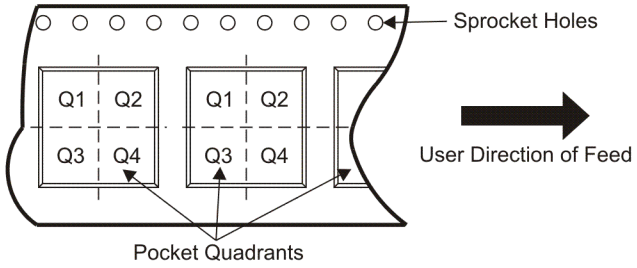


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

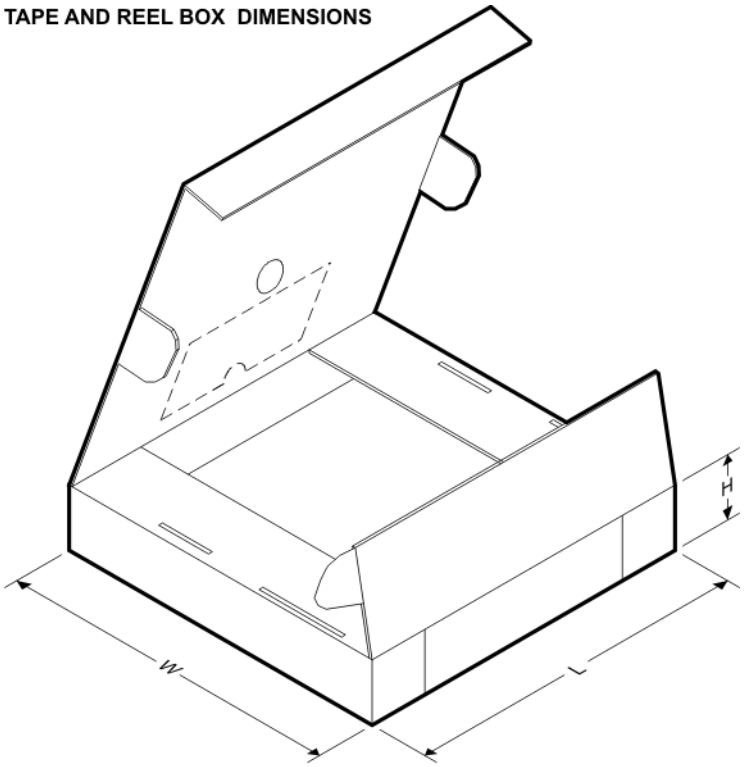
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1158IRTCR	QFN	RTC	48	2500	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2
ADS1158IRTCT	QFN	RTC	48	250	330.0	16.4	7.3	7.3	1.5	12.0	16.0	Q2

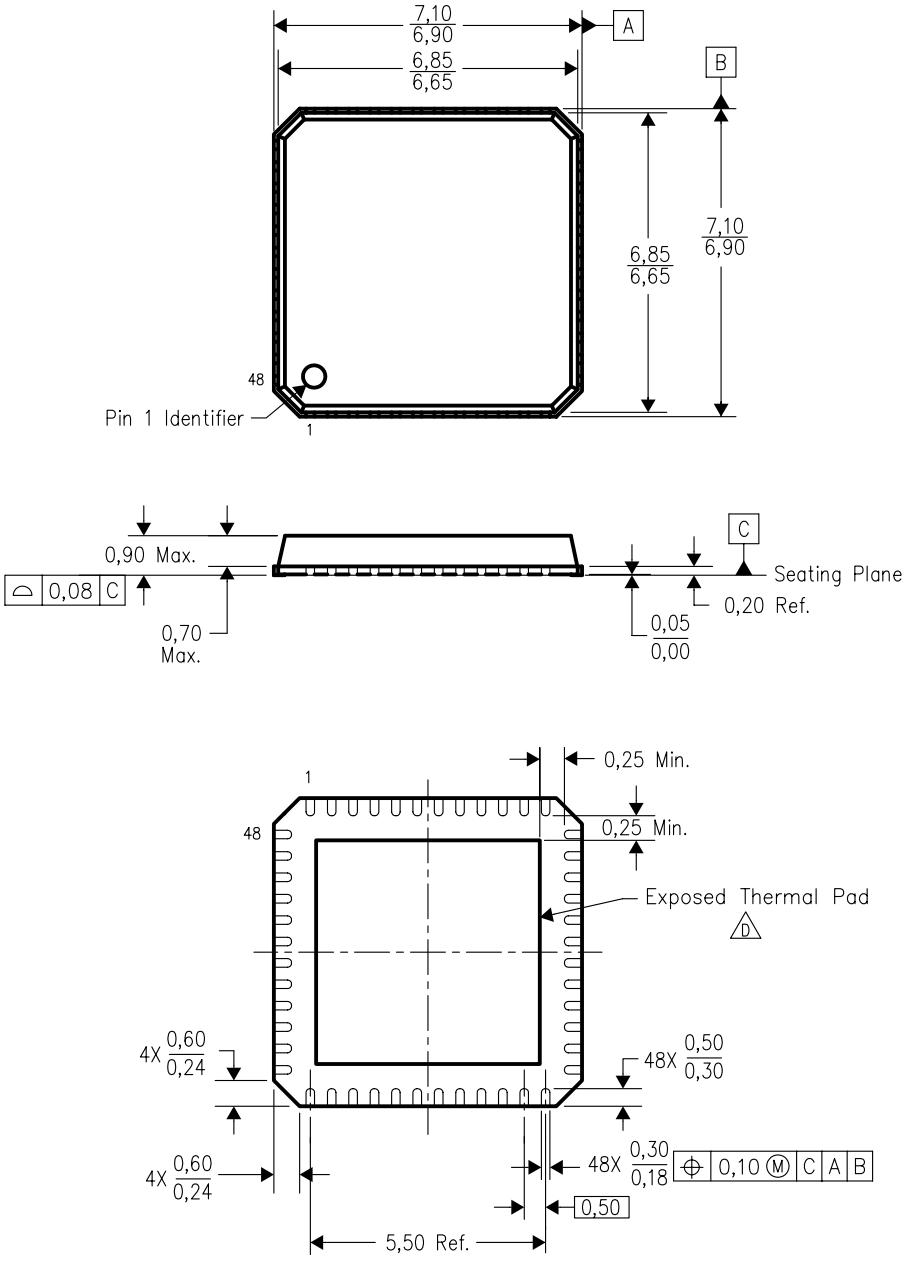
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1158IRTCR	QFN	RTC	48	2500	333.2	345.9	28.6
ADS1158IRTCT	QFN	RTC	48	250	333.2	345.9	28.6

RTC (S–PQFP–N48) PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

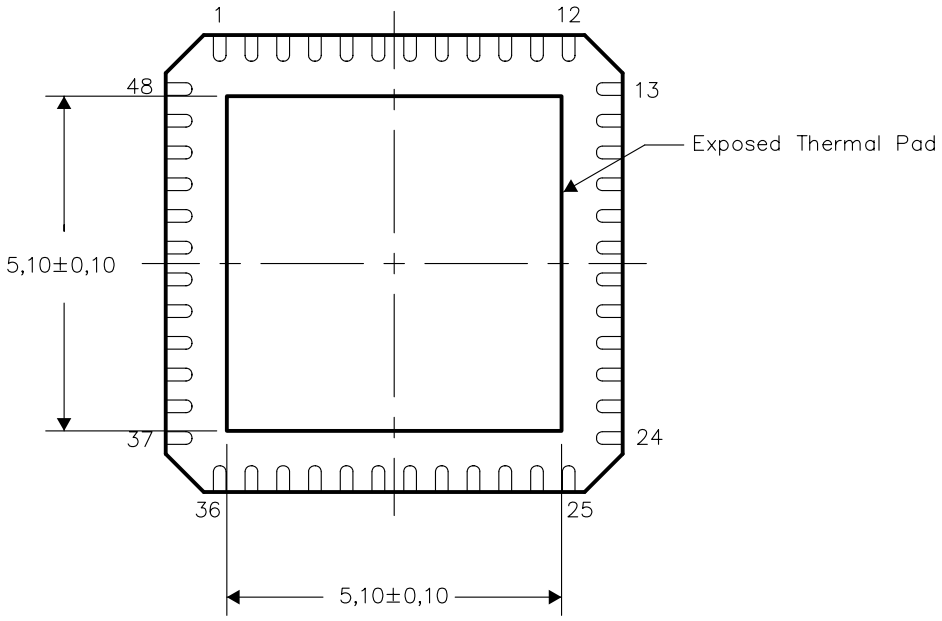
RTC (S–PQFP–N48)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

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