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PRODUCT PREVIEW

ADS62P45, ADS62P44
ADS62P43, ADS62P42

REV1P0 SEP 2007

Dual Channel 14-Bit, 125/105/80/65 MSPS ADC with Parallel CMOS/DDR LVDS outputs

FEATURES

- Maximum Sample Rate: 125 MSPS
- 14-bit Resolution with No Missing Codes
- 92 dB Crosstalk at 50MHz
- Parallel CMOS and DDR LVDS Output Options
- 3.5 dB Coarse Gain and Programmable Fine Gain up to 6 dB for SNR/SFDR trade-off
- Supports Sine, LVPECL, LVDS & CMOS clock inputs & amplitude down to 400 mV p-p
- Digital Processing Block with
  - Offset correction
  - Fine gain correction, (0.05 dB step)
  - Decimation by 2/4/8
  - Built-in & Custom programmable 24-tap Low / High / Band pass filters
- Clock duty cycle stabilizer
- Internal reference, supports external reference also
- 64-QFN Package (9mm x 9mm)
- Pin compatible 12-bit family (ADS62P2X)

Table 1 ADS62PXX Dual Channel Family

	125 MSPS	105 MSPS	80 MSPS	65 MSPS
14 bit	ADS62P45	ADS62P44	ADS62P43	ADS62P42
12 bit	ADS62P25	ADS62P24	ADS62P23	ADS62P22
11 bit	ADS62P15	-	-	-

Table 2 Performance Summary

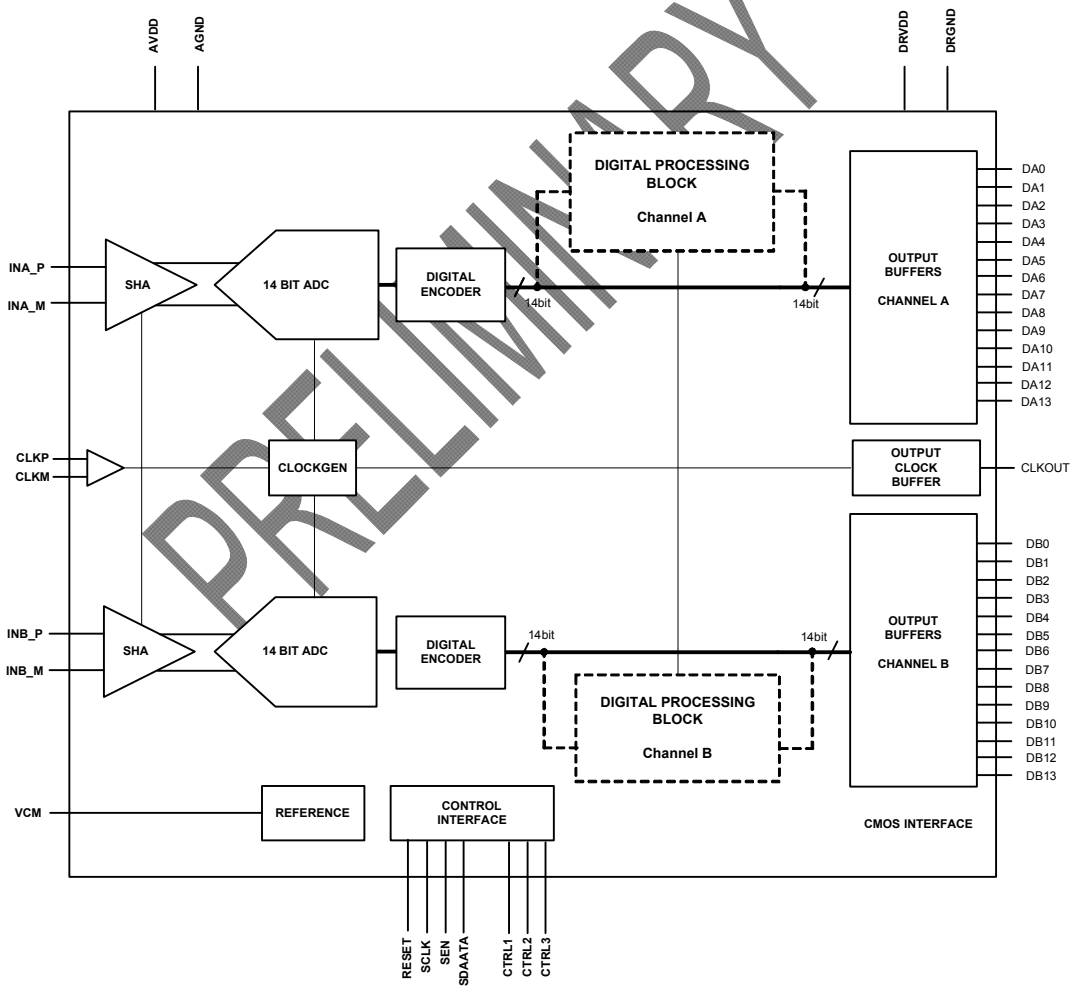
		ADS62P45	ADS62P44	ADS62P43	ADS62P42
SFDR, dBc	Fin = 10 MHz	92	92	94	94
	Fin = 170 MHz, 3.5dB gain	81	82	83	84
SINAD, dBFS	Fin = 10 MHz	73.8	73.8	73.9	74
	Fin = 170 MHz, 3.5dB gain	70.3	70.3	70.6	70.6
Power, mW per channel		396	350	294	259

DESCRIPTION

ADS62P4X is a family of dual channel 14-bit A/D converters with maximum sample rates up to 125 MSPS. It combines high performance and low power consumption in a compact 64 QFN package. Using an internal sample and hold and low jitter clock buffer, the ADC supports high SNR and high SFDR at high input frequencies. It has coarse and fine gain options that can be used to improve SFDR performance at lower full-scale input ranges.

ADS62P4X includes a digital processing block that consists of several useful & commonly used digital functions such as ADC offset correction, fine gain correction (in steps of 0.05 dB), decimation by 2,4,8 & in-built & custom programmable filters. By default, the digital processing block is bypassed & its functions are disabled.

Two output interface options exist – parallel CMOS and DDR LVDS (Double Data Rate). ADS62P4X includes internal references while traditional reference pins and associated decoupling capacitors have been eliminated. The device also supports an external reference mode. The device is specified over the industrial temperature range (-40°C to +85°C).



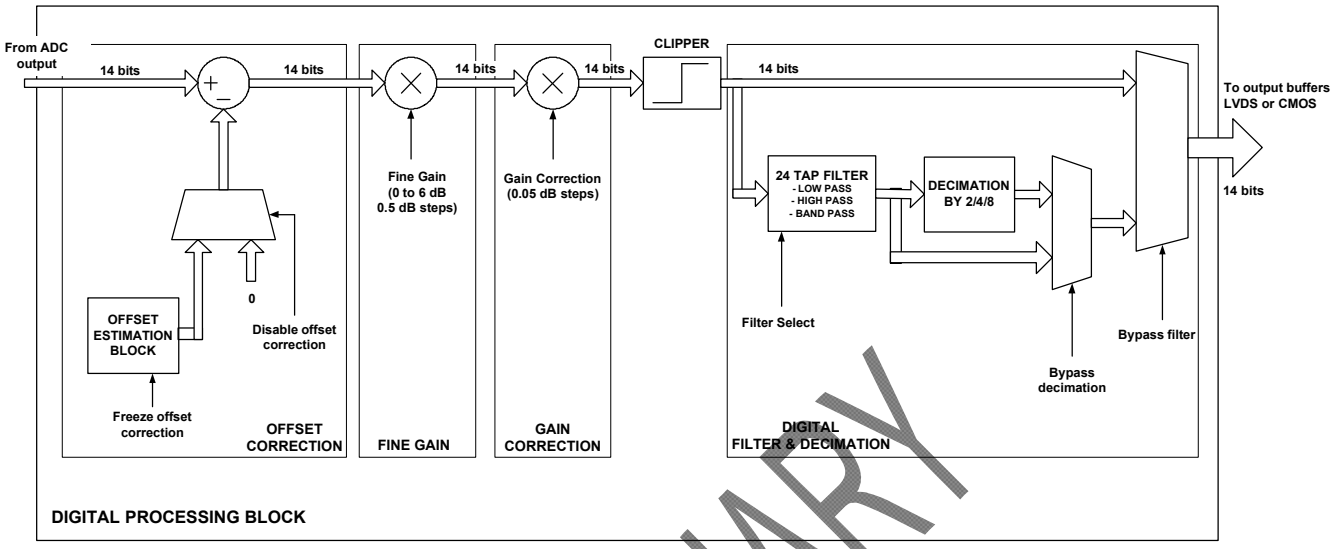


Figure 1 Digital Processing Block Diagram

PACKAGE/ORDERING INFORMATION (1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ECO PLAN (2)	LEAD/BALL FINISH	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS62P45	QFN-64	RGC	-40C to +85C	GREEN (RoHS & no Sb/Br)	Cu NiPdAu	AZ62P45	ADS62P45RGC	TUBE
ADS62P44	QFN-64	RGC	-40C to +85C			AZ62P44	ADS62P44RGC	TUBE
ADS62P43	QFN-64	RGC	-40C to +85C			AZ62P43	ADS62P43RGC	TUBE
ADS62P42	QFN-64	RGC	-40C to +85C			AZ62P42	ADS62P42RGC	TUBE

(1) $\theta_{JA} = TBD, \theta_{JC} = TBD$.

(2) Eco Plan - The planned eco-friendly classification:
Green (RoHS & no Sb/Br) : TI defines "Green" to mean Pb-Free (RoHS compatible) and free of Bromine (Br) and Antimony (Sb) based flame retardants.

ABSOLUTE MAXIMUM RATINGS (1)

	VALUE	UNIT
Supply voltage range, AVDD	- 0.3 V to 3.9	V
Supply voltage range, DRVDD	-0.3 V to 3.9	V
Voltage between AGND and DRGND	-0.3 to 0.3	V
Voltage between AVDD to DRVDD	-0.3 to 3.3	V
Voltage applied to external pin, CM (in external reference mode)	-0.3 to 2.0	V
Voltage applied to analog input pins, INA_P, INA_M, INB_P, INB_M	-0.3V to minimum(3.6, AVDD + 0.3V)	V
Voltage applied to clock input pins, CLKP, CLKM	-0.3V to AVDD + 0.3V	V
Operating free-air temperature range, T_A	-40 to 85	°C
Operating junction temperature range, T_J	125	°C
Storage temperature range, T_{stg}	-65 to 150	°C
Lead temperature 1.6 mm (1/16 ") from the case for 10 seconds	220	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	TYP	MAX	UNIT
SUPPLIES					
AVDD Analog supply voltage		3.0	3.3	3.6	V
DRVDD Digital supply voltage	CMOS interface	1.65	1.8 to 3.3	3.6	V
	LVDS interface	3.0	3.3	3.6	V
ANALOG INPUTS					
Differential input voltage range			2		V_{PP}
Input common-mode voltage			1.5 +/- 0.1		V
Voltage applied on CM in external reference mode			1.5 ± 0.05		V
CLOCK INPUT					
Input clock sample rate, Fs	ADS62P45	1		125	MSPS
	ADS62P44	1		105	MSPS
	ADS62P43	1		80	MSPS
	ADS62P42	1		65	MSPS
Input Clock amplitude differential (V_{CLKP}-V_{CLKM})	Sine wave, ac-coupled	0.3	3.0		V pp
	LVPECL, ac-coupled		1.6		V pp
	LVDS, ac-coupled		0.7		V pp
	LVCMOS, single-ended, ac-coupled		3.3		V
Input clock duty cycle		35 %	50 %	65 %	
DIGITAL OUTPUTS					
Output buffer drive strength	For C_{LOAD} <= 5 pF and DRVDD >= 2.2V		Default strength		
	For C_{LOAD} > 5 pF and DRVDD > 2.2V		Maximum strength		
	For DRVDD < 2.2V		Maximum strength		
C_{LOAD}, Maximum external load capacitance from each output pin to DRGND	CMOS interface			5	pF
	LVDS interface, without internal termination			5	pF
	LVDS interface, with 100 Ω internal termination			10	pF
R_{LOAD}, Differential load resistance between the LVDS output pairs (LVDS mode)			100		Ω
Operating free-air temperature, T_A		-40		85	°C

ELECTRICAL CHARACTERISTICS

Typical values at 25C, min & max values are across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 1.8V to 3.3V, 50% clock duty cycle, -1dBFS differential analog input, internal reference, applies to CMOS & LVDS interfaces unless otherwise noted.

PARAMETER	ADS62P45 125 MSPS			ADS62P44 105 MSPS			ADS62P43 80 MSPS			ADS62P42 65 MSPS			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Resolution			14			14			14			14	bits
Analog Input													
Differential input voltage range		2.0			2.0			2.0			2.0		V pp
Differential input resistance (at dc), see Figure 10		1			1			1			1		MΩ
Differential input capacitance, see Figure 11		7			7			7			7		pF
Analog input bandwidth		450			450			450			450		MHz
Analog input common mode current (per input pin of each channel)		165			140			110			91		µA
VCM common mode voltage output		1.5			1.5			1.5			1.5		V
VCM output current capability		4			4			4			4		mA
Power Supply													
IAVDD Analog supply current		232			205			172			152		mA
IDRVDD Output buffer supply current, CMOS interface 2.5MHz input signal, no load capacitance (1)		15			13			10.5			9		mA
Total power – CMOS interface, DRVDD = 1.8V		792	TBD		700	TBD		587	TBD		518	TBD	mW
Total power – LVDS interface, DRVDD = 3.3V		TBD			TBD			TBD			TBD		mW
Global power down		50	TBD		50	TBD		50	TBD		50	TBD	mW

(1) In CMOS mode, the DRVDD current scales with the sampling frequency and the load capacitance on output pins.

ELECTRICAL CHARACTERISTICS

Typical values at 25C, min & max values are across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 3.3V, 50% clock duty cycle, -1dBFS differential analog input, internal reference, applies to CMOS & LVDS interfaces, unless otherwise noted.

PARAMETERS	ADS62P45 125 MSPS			ADS62P44 105 MSPS			ADS62P43 80 MSPS			ADS62P42 65 MSPS			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY													
No Missing Codes	Assured			Assured			Assured			Assured			
DNL Differential Non-Linearity	TBD	+/- 0.8	TBD	TBD	+/- 0.7	TBD	TBD	+/- 0.5	TBD	TBD	+/- 0.4	TBD	LSB
INL Integral Non-Linearity	TBD	+/- 3	TBD	TBD	+/- 2.5	TBD	TBD	+/-1.5	TBD	TBD	+/-1.5	TBD	LSB
Offset Error	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	mV
Offset error temperature coefficient		TBD			TBD			TBD			TBD		µV/ °C
Offset error variation with supply		TBD			TBD			TBD			TBD		mV/V
There are two sources of gain error – internal reference inaccuracy and channel gain error													
Gain error due to internal reference inaccuracy alone	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	% FS
Reference gain error temperature coefficient		TBD			TBD			TBD			TBD		Δ%/ °C
Gain error of channel alone (1)	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	% FS
Channel gain error temperature coefficient		TBD			TBD			TBD			TBD		Δ%/ °C
Gain matching		TBD			TBD			TBD			TBD		

(1) This is specified by design and characterization; it is not tested in production.

ELECTRICAL CHARACTERISTICS

Typical values at 25C, min & max values are across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 3.3V, 50% clock duty cycle, -1dBFS differential analog input, internal reference, applies to CMOS & LVDS interfaces, unless otherwise noted.

PARAMETERS			ADS62P45 125 MSPS			ADS62P44 105 MSPS			ADS62P43 80 MSPS			ADS62P42 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Dynamic Characteristics															
SNR Signal to noise ratio, CMOS	Fin= 10MHz			74.3			74.3			74.4			74.5		dBFS
	Fin = 50MHz		TBD	73.8			73.8		TBD	74.1			74.2		
	Fin = 70MHz			73.6		TBD	73.6			74		TBD	74.1		
	Fin = 170MHz	0 dB gain		71.8			71.8			72.5			72.5		
		3.5 dB gain		71			71			71.4			71.4		
	Fin = 230MHz	0 dB gain		71			71			72			72		
		3.5 dB gain		70			70			71			71		
SNR Signal to noise ratio, LVDS	Fin= 10MHz			74.5			74.5			74.6			74.7		dBFS
	Fin = 50MHz		TBD	74			74		TBD	74.3			74.4		
	Fin = 70MHz			73.8		TBD	73.8			74.2		TBD	74.3		
	Fin = 170MHz	0 dB gain		72.1			72.1			72.7			72.7		
		3.5 dB gain		71			71			71.8			71.8		
	Fin = 230MHz	0 dB gain		71.2			71			72.2			72.2		
		3.5 dB gain		70.1			70.1			71.2			71.2		
RMS output noise	Inputs tied to common-mode			0.96			0.96			0.96			0.96		LSB

ELECTRICAL CHARACTERISTICS

Typical values at 25C, min & max values are across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 3.3V, 50% clock duty cycle, -1dBFS differential analog input, internal reference, applies to CMOS & LVDS interfaces, unless otherwise noted.

PARAMETERS			ADS62P45 125 MSPS			ADS62P44 105 MSPS			ADS62P43 80 MSPS			ADS62P42 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SINAD Signal to noise & distortion ratio, CMOS	Fin= 10MHz			73.8			73.8			73.9			74		dBFS
	Fin = 50MHz		TBD	73.2			73.2		TBD	73.6			73.7		
	Fin = 70MHz			73		TBD	73			73.4		TBD	73.5		
	Fin = 170MHz	0 dB gain		70.6			70.7			71.5			71.5		
		3.5 dB gain		70.1			70.2			70.6			70.6		
	Fin = 230MHz	0 dB gain		68.7			68.7			69.7			69.9		
		3.5 dB gain		68.4			68.5			69.5			69.6		
SINAD Signal to noise & distortion ratio, LVDS	Fin= 10MHz			74			74			74.1			74.1		dBFS
	Fin = 50MHz		TBD	73.4			73.4		TBD	73.8			73.8		
	Fin = 70MHz			73.2		TBD	73.4			73.6		TBD	73.6		
	Fin = 170MHz	0 dB gain		70.8			70.8			71.7			71.6		
		3.5 dB gain		70.5			70.5			70.8			70.7		
	Fin = 230MHz	0 dB gain		68.9			68.9			68.1			68		
		3.5 dB gain		68.6			68.7			69.7			69.7		
ENOB, Effective number of bits	Fin = 50 MHz		TBD	11.8			11.8		TBD	11.9			12		LSB

ELECTRICAL CHARACTERISTICS

Typical values at 25C, min & max values are across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 3.3V, 50% clock duty cycle, -1dBFS differential analog input, internal reference, applies to CMOS & LVDS interfaces, unless otherwise noted.

PARAMETERS			ADS62P45 125 MSPS			ADS62P44 105 MSPS			ADS62P43 80 MSPS			ADS62P42 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SFDR Spurious Free Dynamic Range	Fin= 10MHz			92			92			94			94		dBc
	Fin = 50MHz		TBD	82			82		TBD	88			88		
	Fin = 70MHz			85		TBD	86			86		TBD	86		
	Fin = 170MHz	0 dB gain		79			80			81			82		
		3.5 dB gain		81			82			83			84		
	Fin = 230MHz	0 dB gain		76			78			79			80		
		3.5 dB gain		78			80			81			82		
THD, Total Harmonic Distortion	Fin= 10MHz			90			90			92			92		dBc
	Fin = 50MHz		TBD	80.5			80.5		TBD	86			86		
	Fin = 70MHz			83.5		TBD	84			84		TBD	84		
	Fin = 170MHz	0 dB gain		76			77			78			79		
		3.5 dB gain		78			79			80			81		
	Fin = 230MHz	0 dB gain		73			75			76			77		
		3.5 dB gain		75			77			78			79		

ELECTRICAL CHARACTERISTICS

Typical values at 25C, min & max values are across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 3.3V, 50% clock duty cycle, -1dBFS differential analog input, internal reference, applies to CMOS & LVDS interfaces, unless otherwise noted.

PARAMETERS			ADS62P45 125 MSPS			ADS62P44 105 MSPS			ADS62P43 80 MSPS			ADS62P42 65 MSPS			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
HD2 Second Harmonic Distortion	Fin= 10MHz			94			94			96			96		dBc
	Fin = 50MHz		TBD	85			85		TBD	90			90		
	Fin = 70MHz			88		TBD	88			88		TBD	88		
	Fin = 170MHz	0 dB gain		79			80			81			82		
		3.5 dB gain		81			82			83			84		
	Fin = 230MHz	0 dB gain		76			78			79			80		
		3.5 dB gain		78			80			81			82		
HD3 Third Harmonic Distortion	Fin= 10MHz			92			92			94			94		dBc
	Fin = 50MHz		TBD	82			82		TBD	88			88		
	Fin = 70MHz			85		TBD	86			86		TBD	86		
	Fin = 170MHz	0 dB gain		79			80			81			82		
		3.5 dB gain		81			82			83			84		
	Fin = 230MHz	0 dB gain		76			78			79			80		
		3.5 dB gain		78			80			81			82		

ELECTRICAL CHARACTERISTICS

Typical values at 25C, min & max values are across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 3.3V, 50% clock duty cycle, -1dBFS differential analog input, internal reference, applies to CMOS & LVDS interfaces, unless otherwise noted.

PARAMETERS		ADS62P45 125 MSPS			ADS62P44 105 MSPS			ADS62P43 80 MSPS			ADS62P42 65 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Worst Spur Other than second, third harmonics	Fin= 10MHz		96			96			98			98		dBc
	Fin = 50MHz		88			88			92			94		
	Fin = 70MHz		91			91			91			91		
	Fin = 170MHz		83			84			85			86		
	Fin = 230MHz		85			86			87			88		
IMD 2-Tone Intermodulation Distortion	F1 = 46 MHz, F2 = 50 MHZ, each tone at -7 dBFS		95			95			98			98		dBFS
Input Overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input		1			1			1			1		clock cycles
Cross-talk	Cross-talk signal frequency = 10 MHZ		100			100			100			100		dB
	Cross-talk signal frequency = 50 MHZ		95			95			95			95		dB
PSRR AC Power Supply Rejection Ratio	For 100 mV pp, 1MHz signal on AVDD supply		TBD			TBD			TBD			TBD		dBc

DIGITAL CHARACTERISTICS

The DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1.

AVDD=3.3V, DRVDD=1.8V to 3.3V, unless otherwise specified.

PARAMETER	CONDITIONS	ADS62P45 / ADS62P44 / ADS62P43 / ADS62P42			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		µ A
Low-level input current			-33		µ A
Input capacitance			4		pF
DIGITAL OUTPUTS – CMOS MODE					
High-level output voltage			DRVDD		V
Low-level output voltage			0		V
Output capacitance (internal to device)			2		pF
DIGITAL OUTPUTS – LVDS MODE (1) (2), DRVDD = 3.3V					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output Differential Voltage, $\|V_{OD}\|$			350		mV
V_{OS} Output Offset Voltage	Common-mode voltage of OUTP and OUTM		1200		mV
Output Capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) LVDS buffer current setting, I_O = 3.5 mA

(2) External differential load resistance between the LVDS output pairs, R_{LOAD} = 50 Ω

TIMING CHARACTERISTICS – LVDS AND CMOS MODES (1)

Typical values at 25C, min and max values are across the full temperature range TMIN = -40C to TMAX = 85C, AVDD = 3.3V, DRVDD = 1.8V to 3.3V, 3.0 Vpp sine wave input clock, C_{LOAD} = 5pF (2), I_o = 3.5mA, R_{LOAD} = 100Ω (3), no internal termination, unless otherwise noted.

PARAMETER	CONDITIONS	ADS62P45			ADS62P44			ADS62P43			ADS62P42			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t_a, Aperture delay		TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
t_j, Aperture jitter			130			130			130			130		fs rms
Wake-up time	from power down global		15			15			15			15		µs
	from channel standby		100			100			100			100		ns
	from output buffer disable		100			100			100			100		ns
Latency	Default		14			14			14			14		Clock cycles
	Low latency mode		10			10			10			10		Clock cycles
DDR LVDS INTERFACE (4) DRVDD = 3.3V														
t_{su} Data setup time(5)	Data valid (6) to zero-crossing of CLKOUTP	TBD	1.5		TBD	2.3		TBD	3.8		TBD	5.2		ns
t_h Data hold time(5)	Zero-crossing of CLKOUTP to data becoming invalid (6)	TBD	2.3		TBD	2.3		TBD	2.3		TBD	2.3		ns
t_{PDI} Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	TBD	5.5	TBD	TBD	5.5	TBD	TBD	5.5	TBD	TBD	5.5	TBD	ns
LVDS bit clock duty cycle	Duty cycle of differential clock		50%			50%			50%			50%		
t_{RISE}, t_{FALL} Data rise time, Data fall time	Rise time measured from -100mV to +100mV, Fall time measured from +100mV to -100mV		110			110			110			110		ps
$t_{CLKRISE}$, $t_{CLKFALL}$ Output clock rise time, Output clock fall time			120			120			120			120		ps

PARAMETER	CONDITIONS	ADS62P45			ADS62P44			ADS62P43			ADS62P42			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
PARALLEL CMOS INTERFACE, DRVDD = 2.5V TO 3.3V														
t_{su} Data setup time (5)	Data valid (7) to zero-crossing of CLKOUT	TBD	3.5		TBD	4.3		TBD	5.8		TBD	7.2		ns
t_h Data hold time (5)	Zero-crossing of CLKOUT to data becoming invalid (7)	TBD	3.2		TBD	4		TBD	5.5		TBD	7		ns
t_{PDI} Clock propagation delay	Input clock rising edge cross-over to output clock rising edge cross-over	TBD	7.3	TBD	TBD	7.3	TBD	TBD	7.3	TBD	TBD	7.3	TBD	ns
Output clock duty cycle	Duty cycle of output clock, CLKOUT		53			53			53			53		
t_{RISE}, t_{FALL} Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD		1.5			1.5			1.5			1.5		ns
$t_{CLKRISE}$, $t_{CLKFALL}$ Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD Fall time measured from 80% to 20% of DRVDD		1.5			1.5			1.5			1.5		ns

Notes:

1. Timing parameters are ensured by design and characterization and not tested in production.
2. C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
3. I_O refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.
4. Measurements are done with a transmission line of 100Ω characteristic impedance between the device and the load.
5. Setup and hold time specifications take into account the effect of jitter on the output data and clock. These specifications also assume that the data and clock paths are perfectly matched within the receiver. Any mismatch in these paths within the receiver would appear as reduced timing margin.
6. Data valid refers to LOGIC HIGH of +100.0mV and LOGIC LOW of -100.0mV.
7. Data valid refers to LOGIC HIGH of 2.0V and LOGIC LOW of 0.8V for DRVDD = 3.3V & LOGIC HIGH of 1.7V and LOGIC LOW of 0.7V for DRVDD = 2.5V.

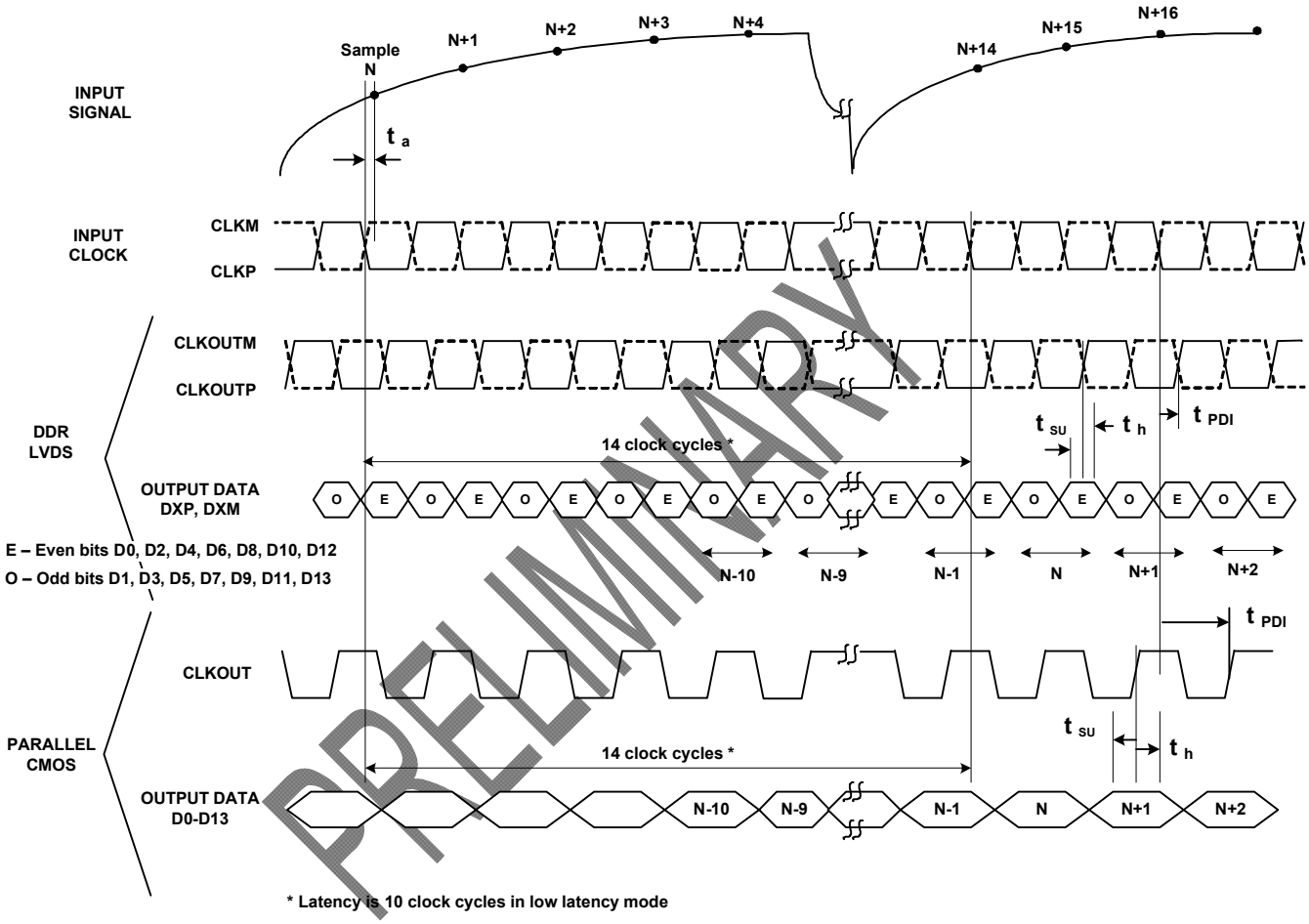


Figure 2 Latency diagram

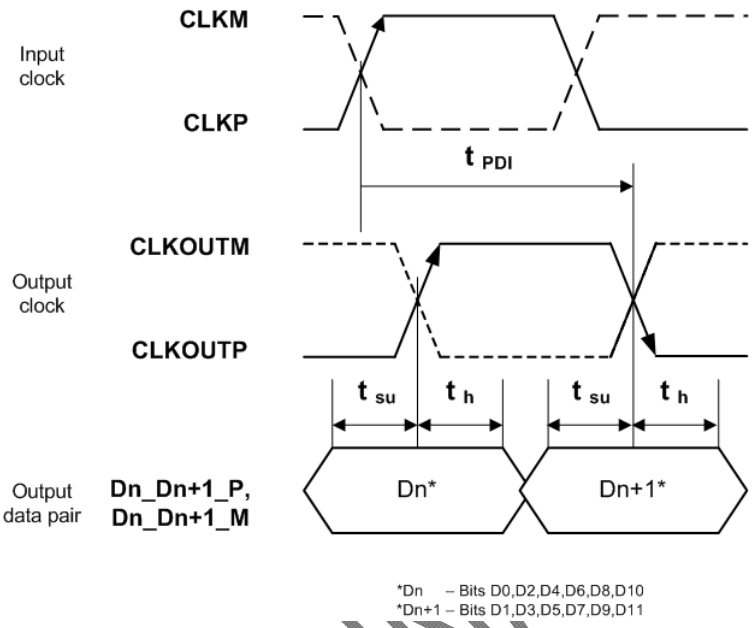


Figure 3 LVDS mode timing

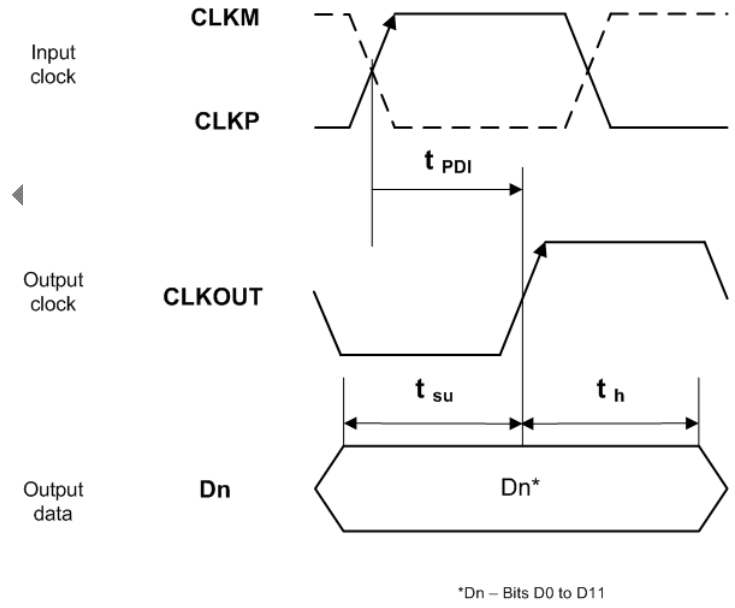


Figure 4 CMOS mode timing

DEVICE CONFIGURATION

ADS62P4X can be configured independently using either parallel interface control or serial interface programming.

USING PARALLEL INTERFACE CONTROL ONLY

To control the device using parallel interface, keep RESET tied to high (AVDD).

Pins SEN, SCLK, CTRL1, CTRL2 and CTRL3 can be used to directly control certain functions of the ADC. After power-up, the device will automatically get configured as per the parallel pin voltage settings (Table 4 to Table 6).

In this mode, SEN and SCLK function as parallel analog control pins, which can be configured using a simple resistor divider as shown in Figure 5. The table below has a description of the modes controlled by the parallel pins.

Table 3 PARALLEL PIN DEFINITION

Control Pin	Type of pin	Controls modes
SCLK	Analog control pins (controlled by analog voltage levels, see Figure 5).	Coarse gain and Internal/external reference
SEN		LVDS/CMOS interface and Output Data Format
CTRL1	Digital control pins (controlled by digital logic levels)	Together control various power down modes and MUX mode.
CTRL2		
CTRL3		

USING SERIAL INTERFACE PROGRAMMING ONLY

To program the device using the serial interface, keep RESET low.

Pins SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or setting bit <RST> = 1. After reset, the RESET pin must be kept low.

The serial interface section describes the register programming and register reset in more detail. Since the parallel pins (CTRL1, CTRL2, CTRL3) are not used in this mode, they must be tied to ground.

USING BOTH SERIAL INTERFACE AND PARALLEL CONTROLS

For increased flexibility, a combination of serial interface registers and parallel pin controls (CTRL1 to CTRL3) can also be used to configure the device. To allow this, keep RESET low.

The parallel interface control pins CTRL1 to CTRL3 are available. After power-up, the device will automatically get configured as per the voltage settings on these pins (Table 6).

SEN, SDATA, and SCLK function as serial interface digital pins and are used to access the internal registers of ADC. The registers must first be reset to their default values either by applying a pulse on RESET pin or by setting bit <RST> = 1. After reset, the RESET pin must be kept low. The serial interface section describes the register programming and register reset in more detail.

Since the power down modes can be controlled using both the parallel pins and serial registers, the priority between the two is determined by <OVRD> bit. When <OVRD> bit = 0, pins CTRL1 to CTRL3 control the power down modes. With <OVRD> = 1, register bits <POWER DOWN> control these modes, over-riding the pin settings.

DETAILS OF PARALLEL CONFIGURATION ONLY

The functions controlled by each parallel pin are described below.

Table 4 SCLK (ANALOG CONTROL PIN)

SCLK	DESCRIPTION
0	0dB gain and Internal reference
(3/8)AVDD	0dB gain and External reference
(5/8)2AVDD	3.5dB Coarse gain and External reference
AVDD	3.5dB Coarse gain and Internal reference

Table 5 SEN (ANALOG CONTROL PIN)

SEN	DESCRIPTION
0	2’s complement format and DDR LVDS output
(3/8)AVDD	Straight binary and DDR LVDS output
(5/8)AVDD	Straight binary and parallel CMOS output
AVDD	2’s complement format and parallel CMOS output

Table 6 CTRL1, CTRL2 and CTRL3 (DIGITAL CONTROL PINS)

CTRL1	CTRL2	CTRL3	DESCRIPTION
LOW	LOW	LOW	Normal operation
LOW	LOW	HIGH	Channel A output buffer disabled
LOW	HIGH	LOW	Channel B output buffer disabled
LOW	HIGH	HIGH	Channel A and B output buffer disabled
HIGH	LOW	LOW	Power global down
HIGH	LOW	HIGH	Channel A standby
HIGH	HIGH	LOW	Channel B standby
HIGH	HIGH	HIGH	MUX mode of operation, Channel A and B data is multiplexed and output on DB13 to DB0 pins. See Multiplexed output mode for detailed description.

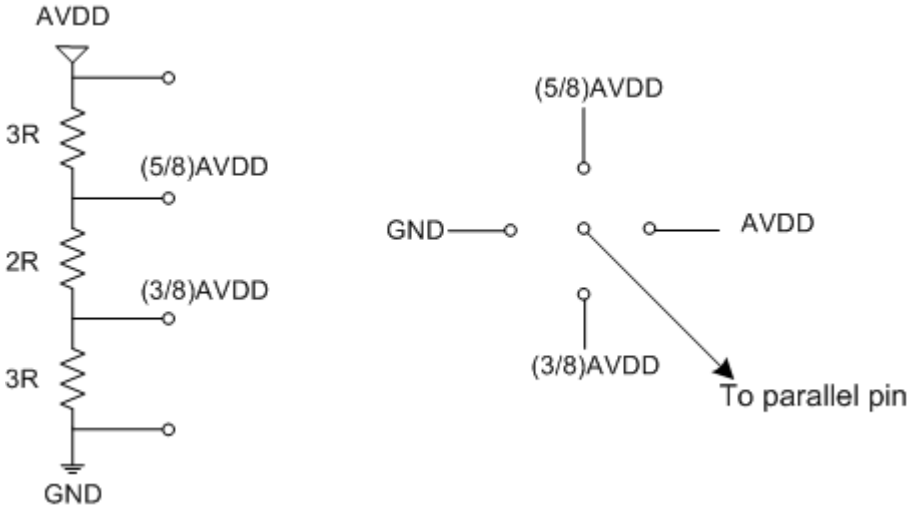


Figure 5 Simple scheme to configure analog control pins (SCLK, SEN)

SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed by the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock) and SDATA (Serial Interface Data).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. In case the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data can be loaded in multiple of 16-bit words within a single active SEN pulse.

The first 8 bits form the register address & the remaining 8 bits the register data. The interface can work with SCLK frequency from 20 MHz down to very low speeds (few Hertz) and also with non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers must be initialized to their default values. This can be done in one of two ways –

1) Either through hardware reset by applying a high-going pulse on RESET pin (of width greater than 10ns) as shown in Figure 6

OR

2) By applying software reset. Using the serial interface, set bit <RST> = 1. This initializes internal registers to their default values and then self-resets the <RST> bit to low. In this case, keep RESET pin low.

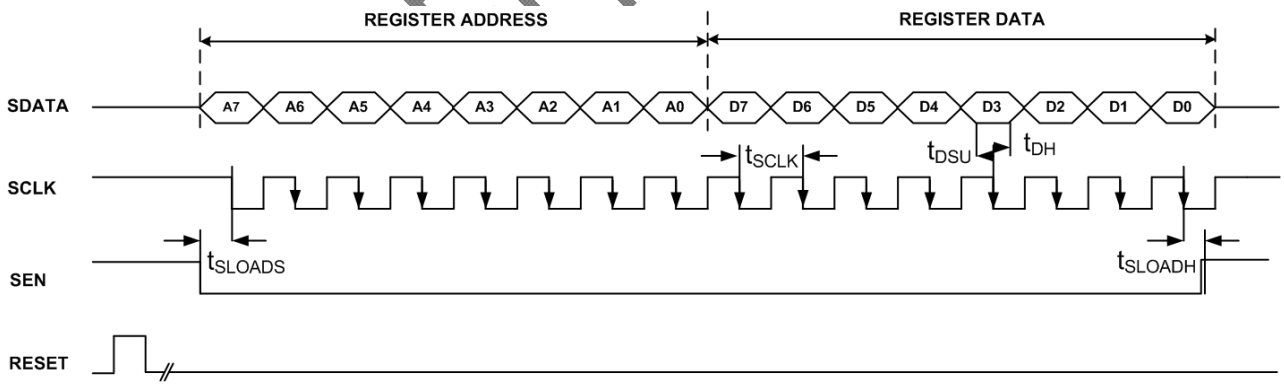


Figure 6 Serial Interface Timing

SERIAL INTERFACE TIMING CHARACTERISTICS

Typical values at 25C, min and max values across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, AVDD = 3.3V, DRVDD = 1.8V to 3.3V, unless otherwise noted.

PARAMETER		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency	> DC		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DS}	SDATA setup time	25			ns
t_{DH}	SDATA hold time	25			ns

RESET TIMING

Typical values at 25C, min and max values across the full temperature range T_{MIN} = -40C to T_{MAX} = 85C, unless otherwise noted.

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_1	Power-on delay	Delay from power-up of AVDD and DRVDD to RESET pulse active	5			ms
t_2	Reset pulse width	Pulse width of active RESET signal	10			ns
t_3	Register write delay	Delay from RESET disable to SEN active	25			ns
t_{PO}	Power-up time	Delay from power-up of AVDD and DRVDD to output stable		7		ms

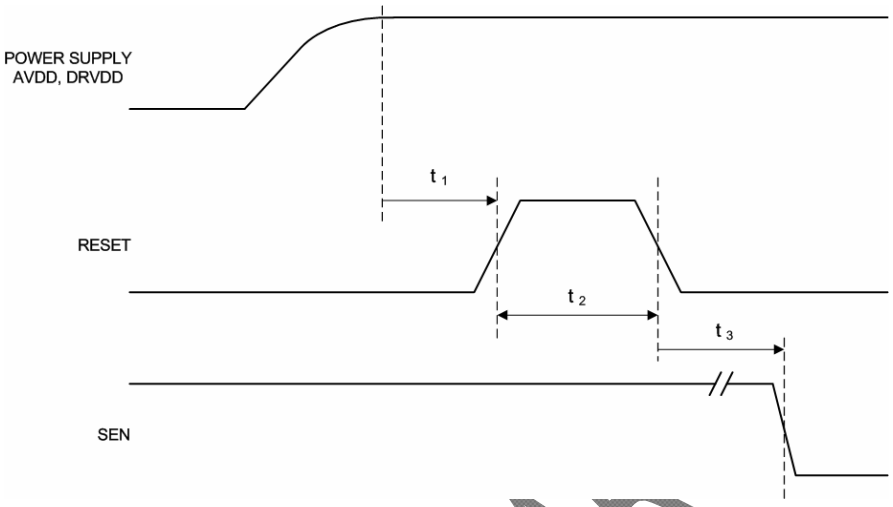


Figure 7 Reset timing diagram

Note: A high-going pulse on RESET pin is required in serial interface mode in case of initialization through hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

SERIAL REGISTER MAP

Table 7 Summary of functions supported by serial interface (1) (2)

REGISTER ADDRESS	REGISTER FUNCTIONS							
A7 - A0 IN HEX	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	<RST> Software Reset	0
10	<CLKOUT STRENGTH>		0	0	0	0	0	0
11	0	0	<CURRENT DOUBLE> LVDS buffer current double		<LVDS CURRENT> LVDS buffer current programmability		<DATAOUT STRENGTH>	
12	0	0	<LVDS TERMINATION> Internal termination programmability					
13	0	0	0	<OFFSET FREEZE>	0	0	0	0
14	<OVRD> Over-ride bit	0	<OUTPUT INTERFACE> LVDS or CMOS interface	<COARSE GAIN> 3.5 dB gain	<REF> Internal / External reference	<POWER DOWN MODES>		
16	0	0	0	<DATA FORMAT> 2s complement or straight binary	Bit/Byte wise (LVDS only)	<TEST PATTERNS>		
17	0	0	0	0	<FINE GAIN> 0 to 6 dB gain in 0.5 dB steps			
18	<CUSTOM LOW> Lower 8 bits							
19	0	0	<CUSTOM HIGH> Upper 6 bits					
1A	<LOW LATENCY>	<OFFSET TC> Offset correction time constant			<GAIN CORRECTION> 0 to 0.5 dB, steps of 0.05 dB			
1B	<OFFSET EN> Offset correction enable	0	<FILTER COEFF SELECT> In-built or custom coefficients	<DECIMATION Enable> Enable decimation	<ODD TAP Enable>	<DECIMATION RATE> Decimate by 2,4,8		
1D	0	0	0	0	0	0	<DECIMATION FILTER FREQ BANDS>	
1E to 2F	<FILTER COEFFICIENTS> 12 coefficients, each 12 bit signed							

1) Multiple functions in a register can be programmed in a single write operation.

DESCRIPTION OF SERIAL REGISTERS

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
00	0	0	0	0	0	0	<RST> Software Reset	0

D1 <RST>

1 Software reset applied – resets all internal registers and self-clears to 0.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
10	<CLKOUT STRENGTH>		0	0	0	0	0	0

D7-D6 <CLKOUT STRENGTH> Output clock buffer drive strength control

01 WEAKER than default drive

00 DEFAULT drive strength

11 STRONGER than default drive strength (recommended for load capacitances > 5 pF)

10 MAXIMUM drive strength (recommended for load capacitances > 5 pF)

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
11	0	0	<CURRENT DOUBLE> LVDS buffer current double		<LVDS CURRENT> LVDS buffer current programmability		<DATAOUT STRENGTH>	

D1-D0 <DATAOUT STRENGTH> Output data buffer drive strength control

01 WEAKER than default drive

00 DEFAULT drive strength

11 STRONGER than default drive strength (recommended for load capacitances > 5 pF)

10 MAXIMUM drive strength (recommended for load capacitances > 5 pF)

D3-D2 <LVDS CURRENT> LVDS Current programmability

00 3.5mA

01 2.5mA

10 4.5mA

11 1.75mA

D5-D4 <CURRENT DOUBLE> LVDS Current double control

00 default current, set by <LVDS CURR>

01 LVDS clock buffer current is doubled, 2x <LVDS CURR>

10 LVDS data & clock buffers current are doubled, 2x <LVDS CURR>

11 unused

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
12	0	0	<LVDS TERMINATION> Internal termination programmability					

D5-D3 <LVDS DATA TERM> Internal termination control for data outputs

000 No internal termination

001 300 Ω

010 180 Ω

011 110 Ω

100 150 Ω

101 100 Ω

110 81 Ω

111 60 Ω

D2-D0 <LVDS CLK TERM> Internal termination control for clock output

000 No internal termination

001 300 Ω

010 180 Ω

011 110 Ω

100 150 Ω

101 100 Ω

110 81 Ω

111 60 Ω

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
13	0	0	0	<OFFSET FREEZE>	0	0	0	0

D4 <OFFSET FREEZE> Offset correction becomes inactive and the last estimated offset value is used to cancel the offset

0 Offset correction active

1 Offset correction inactive

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
14	<OVRD> Over-ride bit	0	<OUTPUT INTERFACE> LVDS or CMOS interface	<COARSE GAIN> 3.5 dB gain	<REF> Internal / External reference	<POWER DOWN MODES>		

D2-D0 <POWER DOWN MODES>

000 Normal operation

001 Channel A output buffer disabled

010 Channel B output buffer disabled

011 Channel A & B output buffers disabled

100 Power down global

101 Channel A standby

110 Channel B standby

111 Multiplexed mode, MUX- (only with CMOS interface)
Channel A and B data is multiplexed and output on DB13 to DB0 pins.

D3 <REF> Reference mode

0 Internal reference enabled

1 External reference enabled

D4 <COARSE GAIN> Coarse gain control

0 0 dB coarse gain

1 3.5 dB coarse gain

D5 <OUTPUT INTERFACE> Output Interface selection

0 Parallel CMOS data outputs

1 DDR LVDS data outputs

D7 <OVRD> Over-ride bit - the power down modes can also be controlled using parallel pins. By setting <OVRD> = 1, register bits <POWER DOWN MODES> will over-ride the settings of the parallel pins.

0 Disable over-ride – pins CTRL1 to CTRL3 control power down modes.

1 Enable over-ride - bits <POWER DOWN MODES> control power down modes.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
16	0	0	0	<DATA FORMAT> 2s complement or straight binary	Bit / Byte wise (LVDS only)	<TEST PATTERNS>		

D2-D0 <TEST PATTERNS> Test Patterns to verify capture

000 Normal ADC operation

001 Outputs all zeros

010 Outputs all ones

011 Outputs toggle pattern

100 Outputs digital ramp

101 Outputs custom pattern

110 Unused

111 Unused

D3 Bit-wise/Byte-wise selection (DDR LVDS mode ONLY)

0 Bit wise – Even bits (D0, D2, D4, D6, D8, D10, D12) on CLKOUT rising edge and Odd bits (D1, D3, D5, D7, D9, D11, D13) on CLKOUT falling edge

1 Byte wise – Lower 7 bits (D0-D6) at CLKOUT rising edge and Upper 7 bits (D7-D13) at CLKOUT falling edge

D4 <DATA FORMAT> Data format selection

0 2s complement

1 Straight binary

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
17	0	0	0	0	<FINE GAIN> 0 to 6 dB gain in 0.5 dB steps			

D3-D0 <FINE GAIN> Gain programmability in 0.5 dB steps

0000 0 dB gain, default after reset

0001 0.5 dB gain

0010 1.0 dB gain

0011 1.5 dB gain

0100 2.0 dB gain

0101 2.5 dB gain

0110 3.0 dB gain

0111 3.5 dB gain

1000 4.0 dB gain

1001 4.5 dB gain

1010 5.0 dB gain

1011 5.5 dB gain

1100 6.0 dB gain

Others Unused

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
18	<CUSTOM LOW> Lower 8 bits							
19	0	0	<CUSTOM HIGH> Upper 6 bits					

D7-D0 <CUSTOM LOW>

8 lower bits of custom pattern available at the output instead of ADC data.

D5-D0 <CUSTOM HIGH>

6 upper bits of custom pattern available at the output instead of ADC data

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1A	<LOW LATENCY>	<OFFSET TC> Offset correction time constant			<GAIN CORRECTION> 0 to 0.5 dB, steps of 0.05 dB			

D3-D0 **<GAIN CORRECTION>** Enables fine gain correction in steps of 0.05 dB (same correction applies to both channels)

0000 0 dB
0001 +0.05 dB
0010 +0.10 dB
0011 +0.15 dB
0100 +0.20 dB
0101 +0.25 dB
0110 +0.30 dB
0111 +0.35 dB
1000 +0.40 dB
1001 +0.45 dB
1010 +0.5 dB

D6-D4 **<OFFSET TC>**, Time constant of offset correction in number of clock cycles (seconds, for sampling frequency = 125MSPS)

000 2^{27} (1.1 s)
001 2^{26} (0.55 s)
010 2^{25} (0.27 s)
011 2^{24} (0.13 s)
100 2^{28} (2.15 s)
101 2^{29} (4.3 s)
110 2^{27} (1.1 s)
111 2^{27} (1.1 s)

D7 **<LOW LATENCY>**

0 Default latency, 14 clock cycles
1 Low latency enabled, 10 clock cycles - Digital Processing Block is bypassed.

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1B	<OFFSET Enable> Offset correction enable	0	<FILTER COEFF SELECT> In-built or custom coefficients	<DECIMATION Enable> Enable decimation	<ODD TAP Enable>	<DECIMATION RATE> Decimate by 2,4,8		

D2-D0 <DECIMATION RATE>

000 Decimate by 2 (pre-defined or user coefficients can be used)

001 Decimate by 4 (pre-defined or user coefficients can be used)

011 No decimation (Pre-defined coefficients are disabled, only custom coefficients are available)

100 Decimate by 8 (Only custom coefficients are available)

D3 <ODD TAP ENABLE>

0 Even taps enabled (24 coefficients)

1 Odd taps enabled (23 coefficients)

D4 <DECIMATION ENABLE>

0 Decimation disabled

1 Decimation enabled

D5 <FILTER COEFF SELECT>

0 Pre-defined coefficients are loaded in the filter

1 User-defined coefficients are loaded in the filter (coefficients have to be loaded in registers – to -)

D7 <OFFSET Enable>

0 Offset correction disabled

1 Offset correction enabled

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1D	0	0	0	0	0	0	<DECIMATION FILTER FREQ BANDS>	

D1-D0 <DECIMATION FILTER FREQ BAND>

With decimate by 2, <DECIMATION RATE> = 000:

00 Low pass filter (-6 dB frequency at Fs/4)

01 High pass filter (-6 dB frequency at Fs/4)

10,11 Unused

With decimate by 4, <DECIMATION RATE> = 001:

00 Low pass filter (-3 dB frequency at Fs/8)

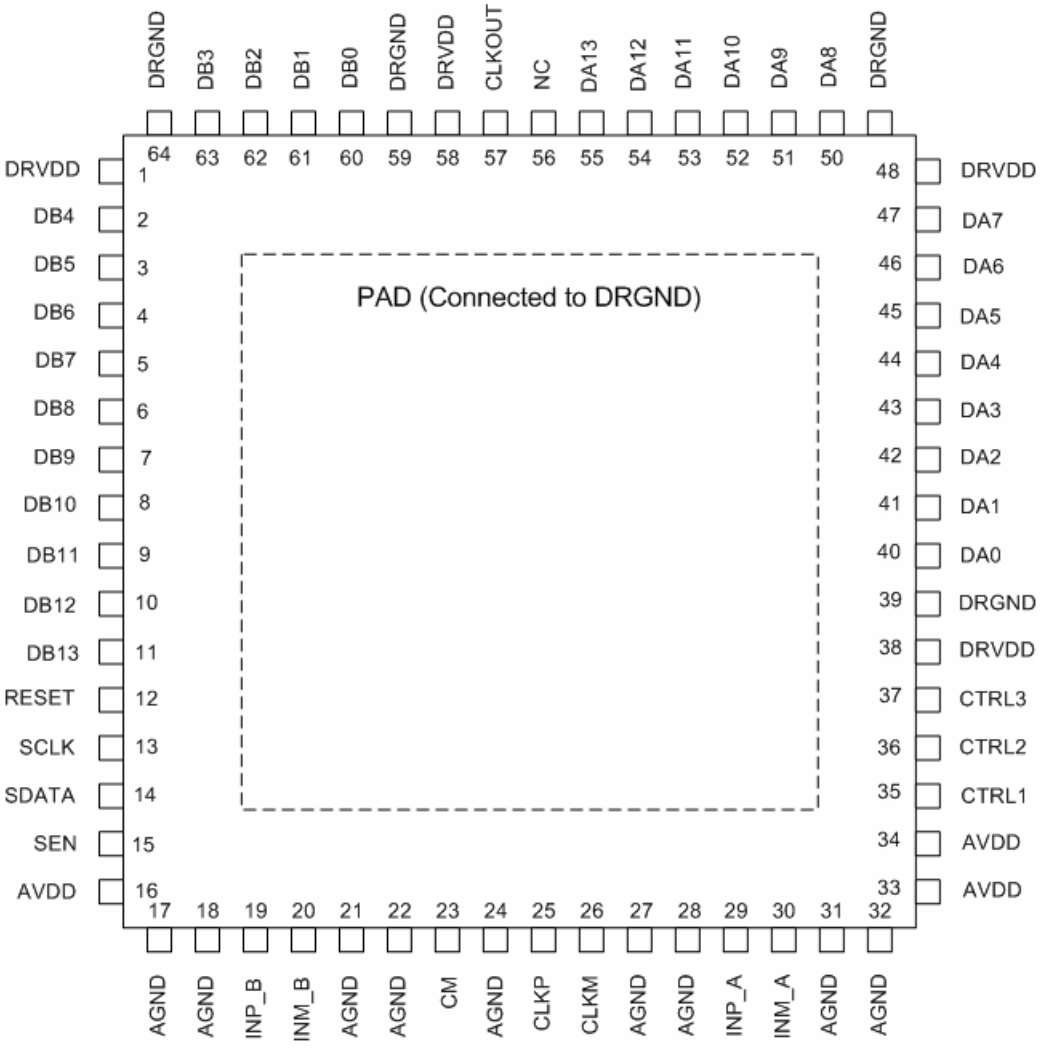
01 Band pass filter (center frequency at 3Fs/16)

10 Band pass filter (center frequency at 5Fs/16)

11 High pass filter (-3 dB frequency at 3Fs/8)

A7 - A0 (hex)	D7	D6	D5	D4	D3	D2	D1	D0
1E to 2F	Custom FIR coefficients See Table 14							

PIN DESCRIPTION (CMOS INTERFACE)

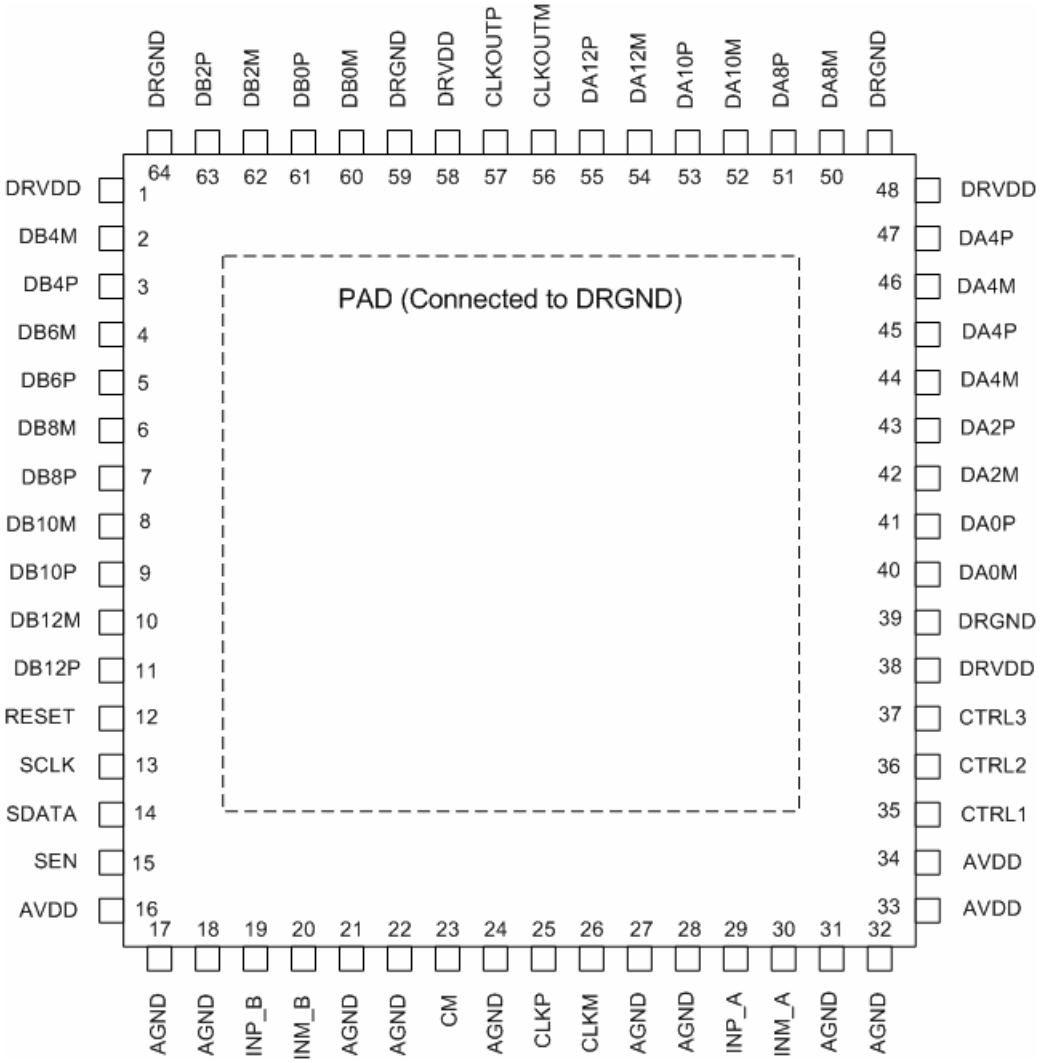


PIN ASSIGNMENTS (CMOS INTERFACE)

Pin Name	Description	Pin Number	Number of pins
AVDD	Analog power supply		
AGND	Analog ground		
CLKP, CLKM	Differential input clock		
INP_A, INM_A	Differential input signal – channel A		
INP_B, INM_B	Differential input signal – channel B		
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the ADC internal references.		
RESET	Serial interface RESET input. In serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset (refer to Serial Interface section). In parallel interface mode, the user has to tie RESET pin permanently HIGH. (SCLK, SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100KΩ pull-down resistor.		
SCLK	This pin functions as serial interface clock input when RESET is low. It functions as analog control pin when RESET is tied high & controls coarse gain and internal/external reference selection. See Table 4 for details. This pin has an internal pull-down resistor to ground.		
SDATA	This pin functions as serial interface data input when RESET is low. This pin has an internal pull-down resistor to ground.		
SEN	This pin functions as serial interface enable input when RESET is low. It functions as analog control pin when RESET is tied high & controls the output interface (LVDS/CMOS) and data format selection. See Table 5 for details. This pin has an internal pull-up resistor to AVDD.		
CTRL1	These are digital logic input pins. They control various power down and multiplexed mode. See Table 6 for details.		
CTRL2			
CTRL3			
DA13 to DA0	Channel A 14-bit data outputs, CMOS		
DB13 to DB0	Channel B 14-bit data outputs, CMOS		
CLKOUT	CMOS Output clock		
DRVDD	Digital supply		
DRGND	Digital ground		
PAD	Digital ground. Solder the pad to the digital ground on the board using multiple vias		

	for good electrical & thermal performance.		
NC	Do not connect		

PIN DESCRIPTION (LVDS INTERFACE)



PIN ASSIGNMENTS (LVDS INTERFACE)

Pin Name	Description	Pin Number	Number of pins
AVDD	Analog power supply		
AGND	Analog ground		
CLKP, CLKM	Differential input clock		
INP_A, INM_A	Differential input signal – Channel A		
INP_B, INM_B	Differential input signal – Channel B		
VCM	Internal reference mode – Common-mode voltage output. External reference mode – Reference input. The voltage forced on this pin sets the ADC internal references.		
RESET	Serial interface RESET input. In serial interface mode, the user MUST initialize internal registers through hardware RESET by applying a high-going pulse on this pin or by using software reset (refer to Serial Interface section). In parallel interface mode, the user has to tie RESET pin permanently HIGH. (SCLK, SDATA and SEN are used as parallel pin controls in this mode) The pin has an internal 100KΩ pull-down resistor.		
SCLK	This pin functions as serial interface clock input when RESET is low. It functions as analog control pin when RESET is tied high & controls coarse gain and internal/external reference selection. See Table 4 for details. This pin has an internal pull-down resistor to ground.		
SDATA	This pin functions as serial interface data input when RESET is low. This pin has an internal pull-down resistor to ground.		
SEN	This pin functions as serial interface enable input when RESET is low. It functions as analog control pin when RESET is tied high & controls the output interface (LVDS/CMOS) and data format selection. See Table 5 for details. This pin has an internal pull-up resistor to AVDD.		
CTRL1	These are digital logic input pins. Together they control various power down and multiplexed mode. See Table 6 for details.		
CTRL2			
CTRL3			
NC	Do not connect		

Pin Name	Description	Pin Number	Number of pins
DA0P	Channel A Differential output data D0 & D1, true		
DA0M	Channel A Differential output data D0 & D1 , complement		
DA2P	Channel A Differential output data D2 & D3 , true		
DA2M	Channel A Differential output data D2 & D3 , complement		
DA4P	Channel A Differential output data D4 & D5 , true		
DA4M	Channel A Differential output data D4 & D5 , complement		
DA6P	Channel A Differential output data D6 & D7 , true		
DA6M	Channel A Differential output data D6 & D7 , complement		
DA8P	Channel A Differential output data D8 & D9 , true		
DA8M	Channel A Differential output data D8 & D9 , complement		
DA10P	Channel A Differential output data D10 & D11 , true		
DA10M	Channel A Differential output data D10 & D11 , complement		
DA12P	Channel A Differential output data D12 & D13 , true		
DA12M	Channel A Differential output data D12 & D13 , complement		
CLKOUTP	Differential output clock, true		
CLKOUTM	Differential output clock, complement		
DB0P	Channel B Differential output data D0 & D1 , true		
DB0M	Channel B Differential output data D0 & D1 , complement		
DB2P	Channel B Differential output data D2 & D3 , true		
DB2M	Channel B Differential output data D2 & D3 , complement		
DB4P	Channel B Differential output data D4 & D5 , true		
DB4M	Channel B Differential output data D4 & D5 , complement		
DB6P	Channel B Differential output data D6 & D7 , true		
DB6M	Channel B Differential output data D6 & D7 , complement		
DB8P	Channel B Differential output data D8 & D9 , true		
DB8M	Channel B Differential output data D8 & D9 , complement		
DB10P	Channel B Differential output data D10 & D11 , true		
DB10M	Channel B Differential output data D10 & D11 , complement		
DB12P	Channel B Differential output data D12 & D13 , true		
DB12M	Channel B Differential output data D12 & D13 , complement		
DRVDD	Digital supply		
DRGND	Digital ground		
PAD	Digital ground. Solder the pad to the digital ground on the board using multiple vias for good electrical & thermal performance.		

APPLICATION INFORMATION

THEORY OF OPERATION

ADS62P4X is a low power 14 bit dual channel pipeline ADC family fabricated in a CMOS process using switched capacitor techniques.

The conversion process is initiated by a rising edge of the external input clock. Once the signal is captured by the input sample & hold, the input sample is sequentially converted by a series of small resolution stages, with the outputs combined in a digital correction logic block. At every clock edge the sample propagates through the pipeline resulting in a data latency of 14 clock cycles. The output is available as 14-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2s complement format.

ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture. This differential topology results in very good AC performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5V, available on VCM pin 13. For a full-scale differential input, each input pin INP, INM has to swing symmetrically between VCM + 0.5V and VCM - 0.5V, resulting in a 2Vpp differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5V nominal) and REFM (0.5V, nominal).

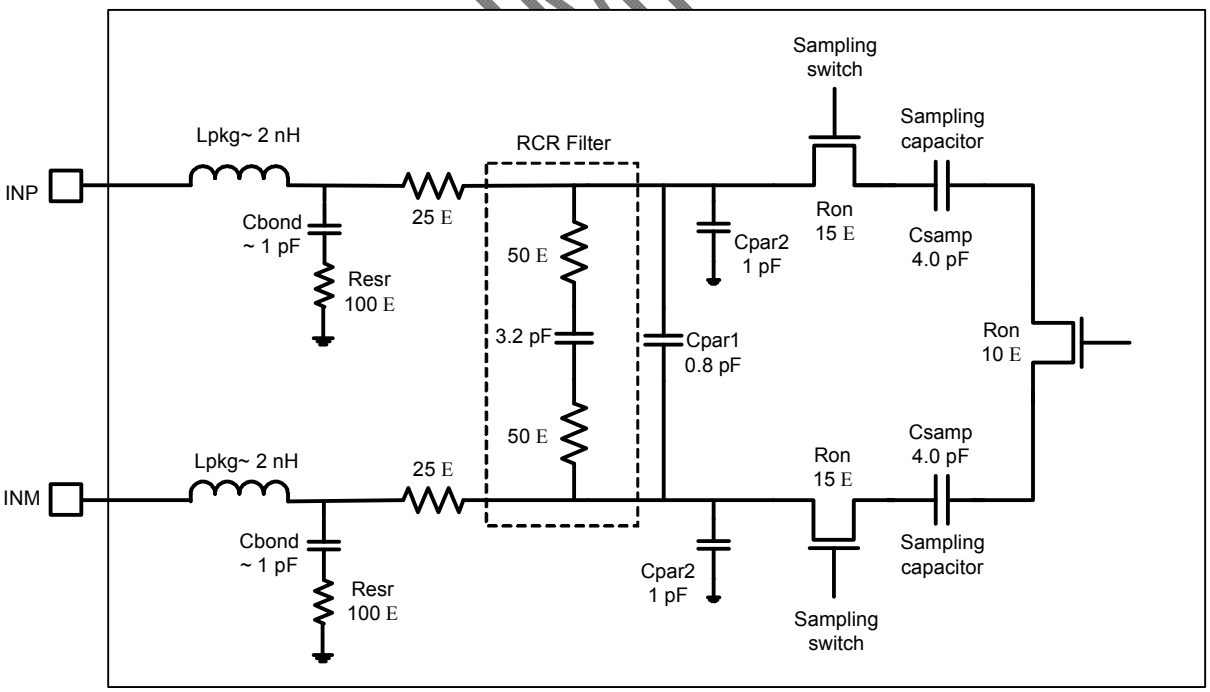


Figure 8 Analog Input Equivalent Circuit

The input sampling circuit has a high 3-dB bandwidth that extends up to 450 MHz (measured from the input pins to the sampled voltage).

TBD

Figure 9 ADC Analog Bandwidth

Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even order harmonic rejection. A 5 Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics.

It is also necessary to present low impedance (< 50 Ω) for the common mode switching currents. This can be achieved by using two resistors from each input terminated to the common mode voltage (VCM).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance must be considered. Figure 10 & Figure 11 show the impedance (Zin = Rin || Cin) looking into the ADC input pins.

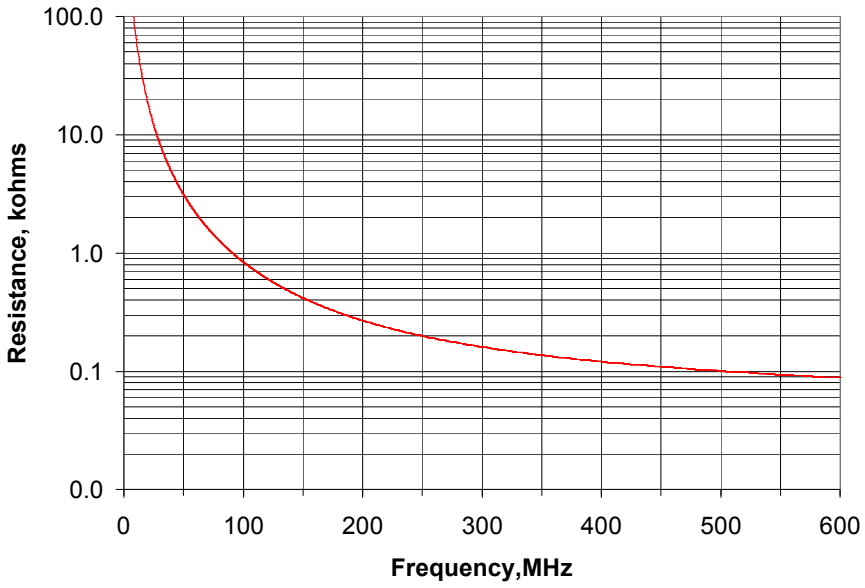


Figure 10 ADC Analog Input Resistance (Rin) across frequency

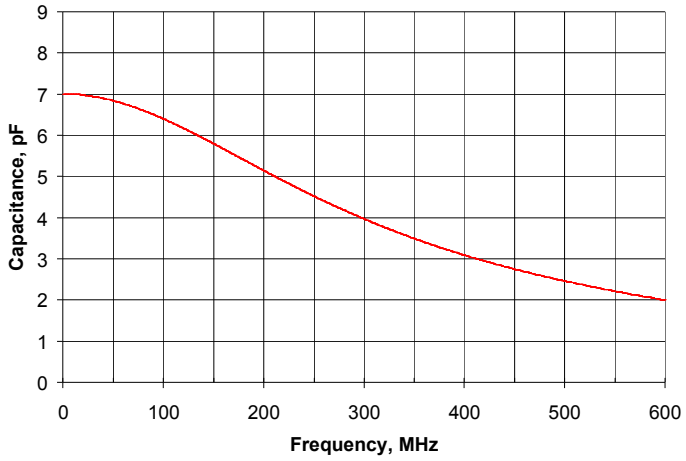


Figure 11 ADC Analog Input Capacitance (Cin) across frequency

Using RF-Transformer based drive circuits

Figure 12 shows a configuration using a single 1:1 turns ratio transformer (for example, Coilcraft WBC1-1) that can be used for low input frequencies (about 100 MHz). The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer' s leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common mode (VCM pin). The value of the termination resistors (connected to common mode) has to be low (< 100 Ω) to provide a low-impedance path for the ADC common-mode switching currents.

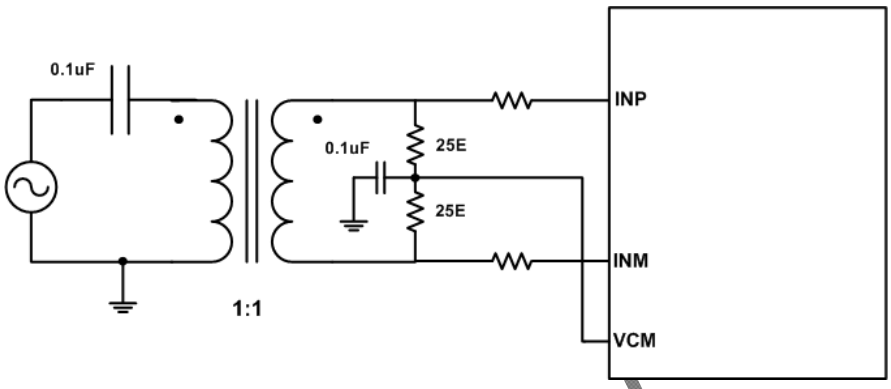


Figure 12 Drive circuit at low input frequencies

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high frequency input signals. Figure 13 shows an example using two transformers (Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the shaded box) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground.

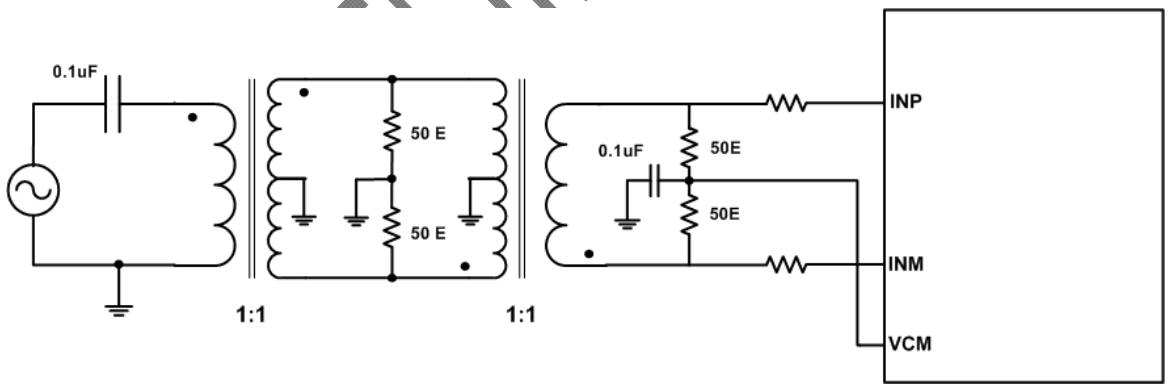


Figure 13 Drive circuit at high input frequencies

Using Differential Amplifier drive circuits

Figure 14 shows a drive circuit using a differential amplifier (TI's THS4509) to convert a single-ended input to differential output that can be interface to the ADC analog input pins. In addition to the single-ended to differential conversion, the amplifier also provides gain (10 dB). R_{FIL} helps to isolate the amplifier outputs from the switching input of the ADC. Together with C_{FIL} it also forms a low-pass filter that band-limits the noise (and signal) at the ADC input. As the amplifier output is ac-coupled, the common-mode voltage of the ADC input pins is set using two 200 W resistors connected to VCM.

The amplifier output can also be dc-coupled. Using the output common-mode control of the THS4509, the ADC input pins can be biased to 1.5 V. In this case, use +4 V and -1 V supplies for the THS4509 so that its output common-mode voltage (1.5 V) is at mid-supply.

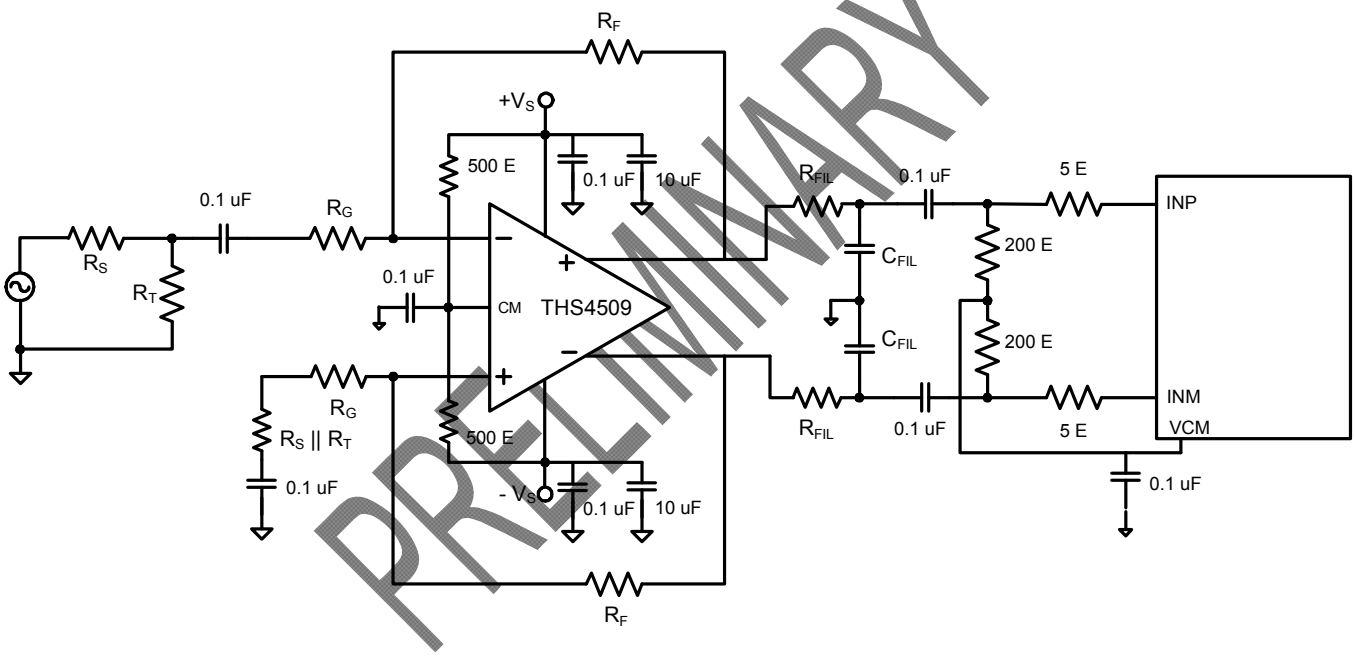


Figure 14 Drive Circuit using the THS4509

Input common-mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1uF low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. Each input pin of the ADC sinks a common-mode current, about 165 uA (at 125MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$\frac{165\mu A x Fs}{125MSPS} \qquad \text{Equation 1}$$

This equation helps to design the output capability and impedance of the CM driving circuit accordingly.

REFERENCE

ADS62P4X has built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the on-chip integration of the requisite reference capacitors eliminates the need for external decoupling. The full-scale input range of the converter can be controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit <REF>.

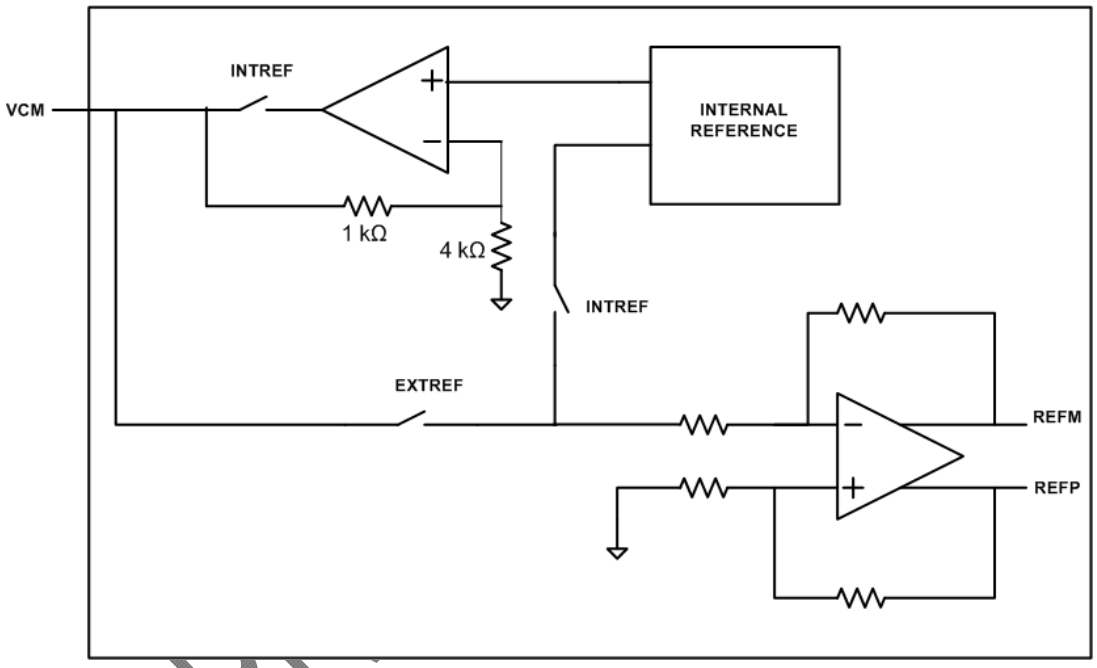


Figure 15 Reference section

Internal reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5V nominal) is output on VCM pin, which can be used to externally bias the analog input pins.

External reference

When the device is in external reference mode, the VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

Full-scale differential input pp = (Voltage forced on VCM) x 1.33 Equation 2

In this mode, the 1.5V common-mode voltage to bias the input pins has to be generated externally.

COARSE GAIN AND PROGRAMMABLE FINE GAIN

ADS62P4X includes gain settings that can be used to get improved SFDR performance (over 0dB gain mode). For each gain setting, the analog input full-scale range scales proportionally, as shown in Table 8 .

The coarse gain is a fixed setting of 3.5 dB and is designed to improve SFDR with little degradation in SNR. The fine gain is programmable in 0.5 dB steps from 0 to 6 dB; however the SFDR improvement is achieved at the expense of SNR. So, the programmable fine gain makes it possible to trade-off between SFDR and SNR. The coarse gain makes it possible to get best SFDR but without losing SNR significantly.

The gains can be programmed using the serial interface (bits <COARSE GAIN> and <FINE GAIN>). Note that the default gain after reset is 0dB.

Table 8 Full-scale range across gains

Gain, dB	Type	Full-Scale, Vpp
0	Default after reset	2V
3.5	Coarse (fixed)	1.34
0.5	Fine (programmable)	1.89
1.0		1.78
1.5		1.68
2.0		1.59
2.5		1.50
3.0		1.42
3.5		1.34
4.0		1.26
4.5		1.19
5.0		1.12
5.5		1.06
6.0		1.00

CLOCK INPUT

The clock inputs can be driven differentially (SINE, LVPECL or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to VCM using internal 5 kΩ resistors as shown in Figure 16. This allows using transformer-coupled drive circuits for sine wave clock or ac-coupling for LVPECL, LVDS clock sources (Figure 18 and Figure 19).

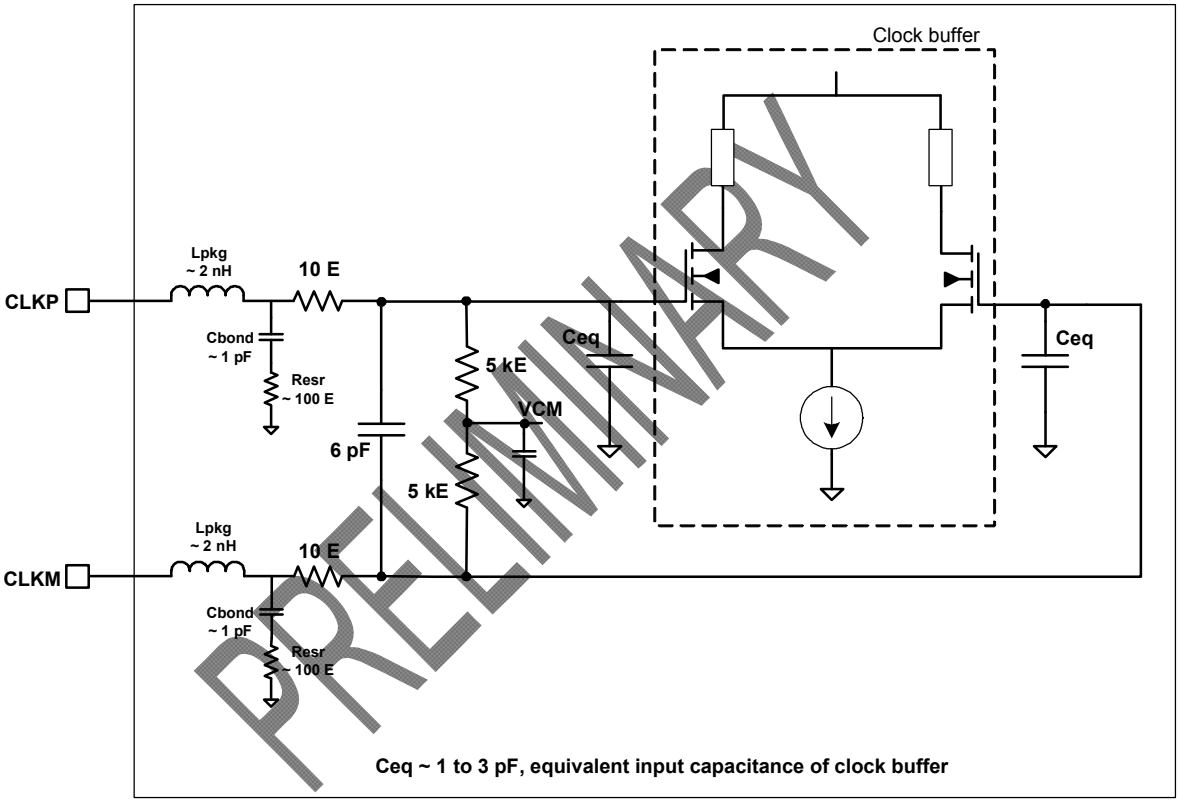


Figure 16 Internal Clock buffer

TBD

Figure 17 Clock Input Impedance

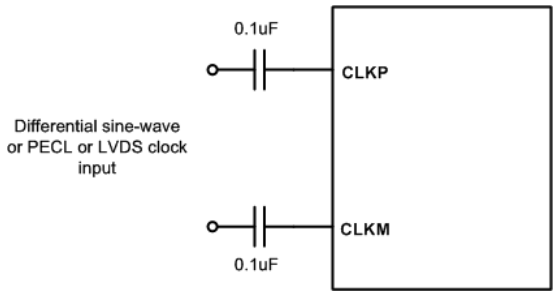


Figure 18 Differential clock driving circuit

Single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM (pin 11) connected to ground with a 0.1-µ F capacitor, as shown in Figure 19.

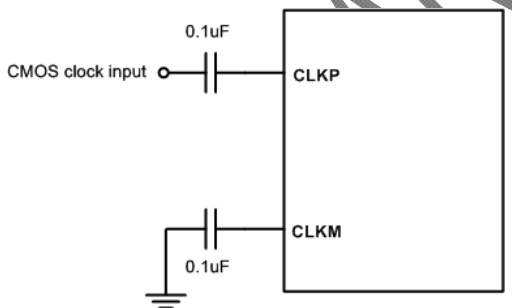


Figure 19 Single-ended clock driving circuit

For best performance, the clock inputs have to be driven differentially, reducing susceptibility to common-mode noise.

For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input.

POWER DOWN

ADS62P4X has three power down modes – power down global, channel standby and individual channel output buffer disable. These can be set using either the serial register bits or using the control pins CTRL1 to CTRL3.

POWER DOWN MODES	CONFIGURE USING				TOTAL POWER, mW (1)	WAKE-UP TIME
	SERIAL INTERFACE <POWER DOWN MODES>	PARALLEL CONTROL PINS				
		CTRL1	CTRL2	CTRL3		
Normal operation	000	low	low	low	792	-
Channel A output buffer disabled	001	low	low	high	782	Fast (100 ns)
Channel B output buffer disabled	010	low	high	low	782	Fast (100 ns)
Channel A & B output buffer disabled	011	low	high	high	772	Fast (100 ns)
Power down global	100	high	low	low	50	Slow (15 µ s)
Channel A standby	101	high	low	high	482	Fast (100 ns)
Channel B standby	110	high	high	low	482	Fast (100 ns)
Multiplexed (MUX) mode – Output data of channel A & B is multiplexed & available on DB13 to DB0 pins.	111	high	high	high	-	-

1. Sampling frequency = 125 MSPS, DRVDD = 1.8V

Power down global

In this mode, the entire chip including both the A/D converters, internal reference and the output buffers are powered down resulting in reduced total power dissipation of about 50 mW. The output buffers are in high impedance state. The wake-up time from the global power down to data becoming valid in normal mode is typically 15 µ s.

Channel standby (individual or both channels)

This mode allows the individual ADCs to be powered down. The internal references are active & this results in fast wake-up time, about 100 ns. The total power dissipation in standby is about 482 mW.

Output buffer disable (individual or both channels)

Each channel' s output buffer can be disabled & put in high impedance state. Wakeup time is fast, about 100 ns.

Input clock stop

In addition to the above, the converter enters a low-power mode when the input clock frequency falls below 1 MSPS. The power dissipation is about 140 mW.

POWER SUPPLY SEQUENCE

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated in the device. Externally, they can be driven from separate supplies or from a single supply.

DIGITAL OUTPUT INFORMATION

ADS62P4X provides 14 bit data per channel and a common output clock synchronized with the data. The output interface can be either parallel CMOS or DDR LVDS voltage levels and can be selected using serial register bit <OUTPUT INTERFACE> or parallel pin SEN.

Parallel CMOS interface

In the CMOS mode, the output buffer supply (DRVDD) can be operated over a wide range from 1.8 V to 3.3 V (typical). Each data bit is output on separate pin as CMOS voltage level, every clock cycle (Figure 20).

For DRVDD > 2.2 V, it is recommended to use the CMOS output clock (CLKOUT) to latch data in the receiving chip. The rising edge of CLKOUT can be used to latch data in the receiver, even at the highest sampling speed. It is recommended to minimize the load capacitance seen by data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For DRVDD < 2.2 V, it is recommended to use external clock (for example, input clock delayed to get desired setup / hold times).

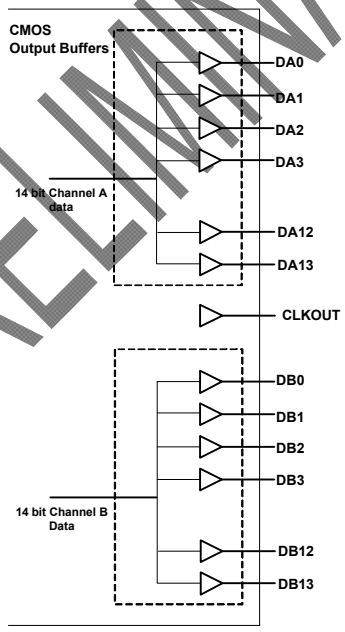


Figure 20 CMOS Output Interface

Output Buffer Strength Programmability

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, ADS62P4X CMOS output buffers are designed with controlled drive strength to get best SNR. The default drive strength also ensures wide data stable window for load capacitances up to 5 pF and DRVDD supply voltage > 2.2 V.

To ensure wide data stable window for load capacitance > 5 pF, there exists option to increase the output data & clock drive strengths using the serial interface (<DATAOUT STRENGTH> & <CLKOUT STRENGTH>). Note that for DRVDD supply voltage < 2.2 V, it is recommended to use maximum drive strength (for any value of load capacitance).

CMOS Interface Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

$$\text{Digital current due to CMOS output switching} = C_L \times \text{DRVDD} \times (N \times F_{AVG}),$$

where C_L = load capacitance, $N \times F_{AVG}$ = average number of output bits switching.

Figure TBD shows the current with various load capacitances across sampling frequencies at 2 MHz analog input frequency.

DDR LVDS Interface

The LVDS interface works only with 3.3V DRVDD supply. In this mode, the 14 data bits of each channel and a common output clock are available as LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair every clock cycle (DDR - Double Data Rate,
Figure 22).

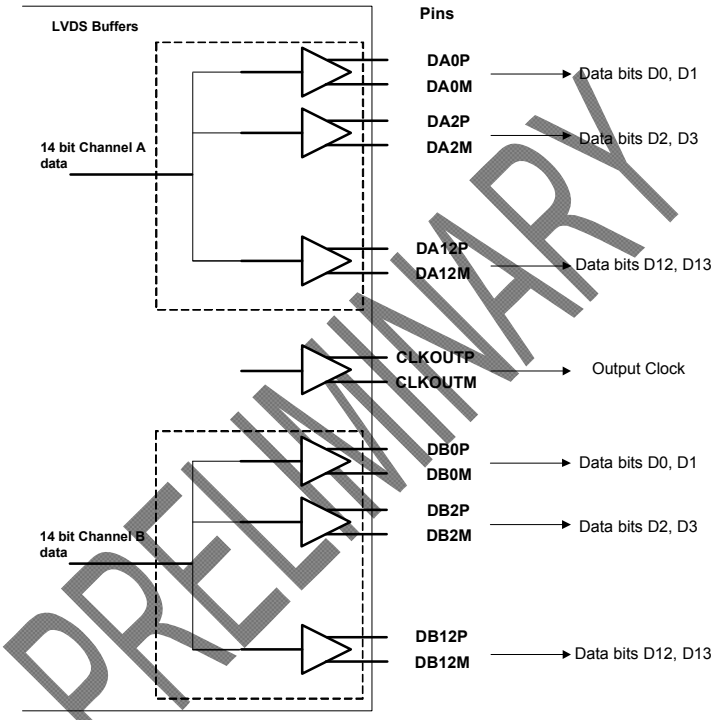


Figure 21 DDR LVDS outputs

Even data bits D0, D2, D4, D6, D8, D10 and D12 are output at the rising edge of CLKOUTP and the odd data bits D1, D3, D5, D7, D9, D11 and D13 are output at the falling edge of CLKOUTP. Both the rising and falling edges of CLKOUTP have to be used to capture all the data bits.

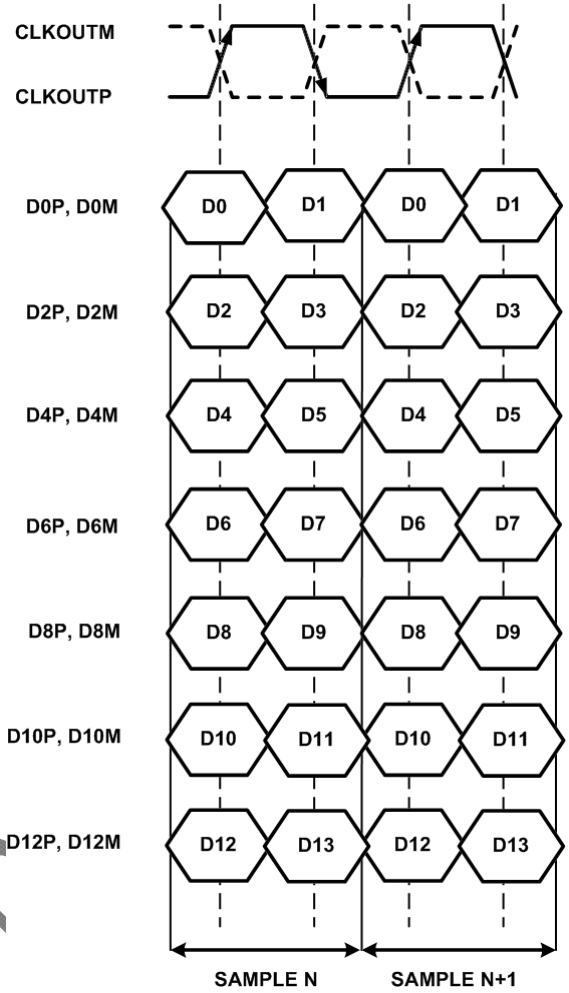


Figure 22 DDR LVDS interface

LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100 Ω, this results in a 350-mV single-ended voltage swing (700-mVPP differential swing). The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.75 mA (<LVDS CURRENT>). In addition, there exists a current double mode, where this current is doubled for the data and output clock buffers (register bits <CURRENT DOUBLE>).

LVDS Buffer Internal Termination

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. The termination resistances available are – 300 Ω, 185 Ω, and 150 Ω (nominal with ±20% variation). Any combination of these three terminations can be programmed; the effective termination is the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 60 Ω.

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100 Ω internal and 100 Ω external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode. Figure 23 &
TBD
Figure 24 compare the LVDS eye diagrams without and with 100 Ω internal termination. With internal termination, the eye looks clean even with 10 pF load capacitance (from each output pin to ground). The terminations can be programmed using register bits <LVDS TERMINATION>.

TBD

Figure 23 LVDS Eye Diagram – No Internal Termination

TBD

Figure 24 LVDS Eye Diagram – With 100Ω Internal Termination

Output Data Format

Two output data formats are supported – 2s complement and straight binary. They can be selected using the serial interface register bit <DATA FORMAT> or controlling the SEN pin in parallel configuration mode.
In the event of an input voltage overdrive, the digital outputs go to the appropriate full scale level. For a positive overdrive, the output code is 0x3FFF in offset binary output format, and 0x1FFF in 2s complement output format. For a negative input overdrive, the output code is 0x0000 in offset binary output format and 0x2000 in 2s complement output format.

Multiplexed Output mode

This mode is available only with CMOS interface. In this mode, the digital outputs of both the channels are multiplexed and output on a single bus (DA0-DA13 pins), as per the timing diagram shown in Figure 25. The channel B output pins (DB0-DB13) are tri-stated. Since the output data rate on the DB bus is effectively doubled, this mode is recommended only for low sampling frequencies (< 65 MSPS).

This mode can be enabled using register bits <POWER DOWN MODES> or using the parallel pins CTRL1 -3 ().

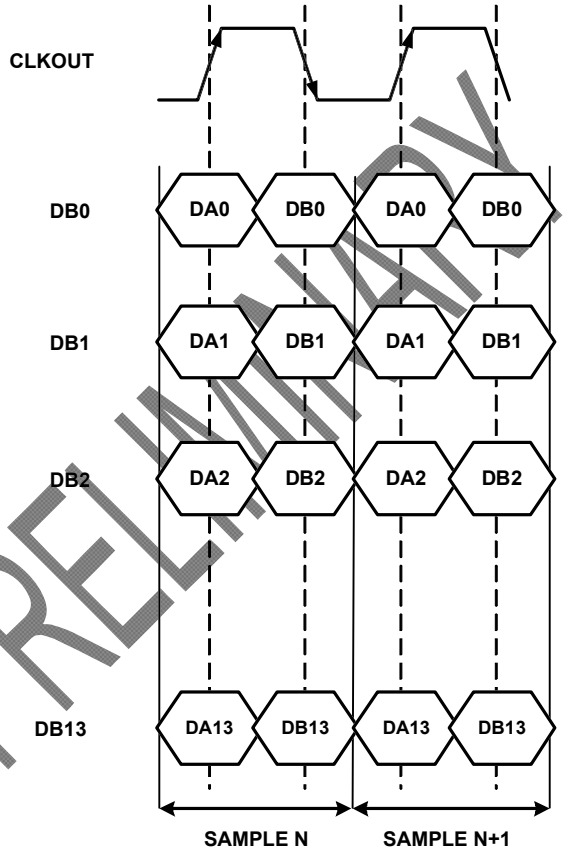


Figure 25 Multiplexed mode - Output Timing

Low Latency mode

The default latency of ADS62P4X is 14 clock cycles. For applications, which cannot tolerate large latency, ADS62P4X includes a special mode with 10 clock cycles latency. In the low latency condition, the Digital Processing block is bypassed and its features (offset correction, fine gain, decimation filters) are not available.

DETAILS OF THE DIGITAL PROCESSING BLOCK

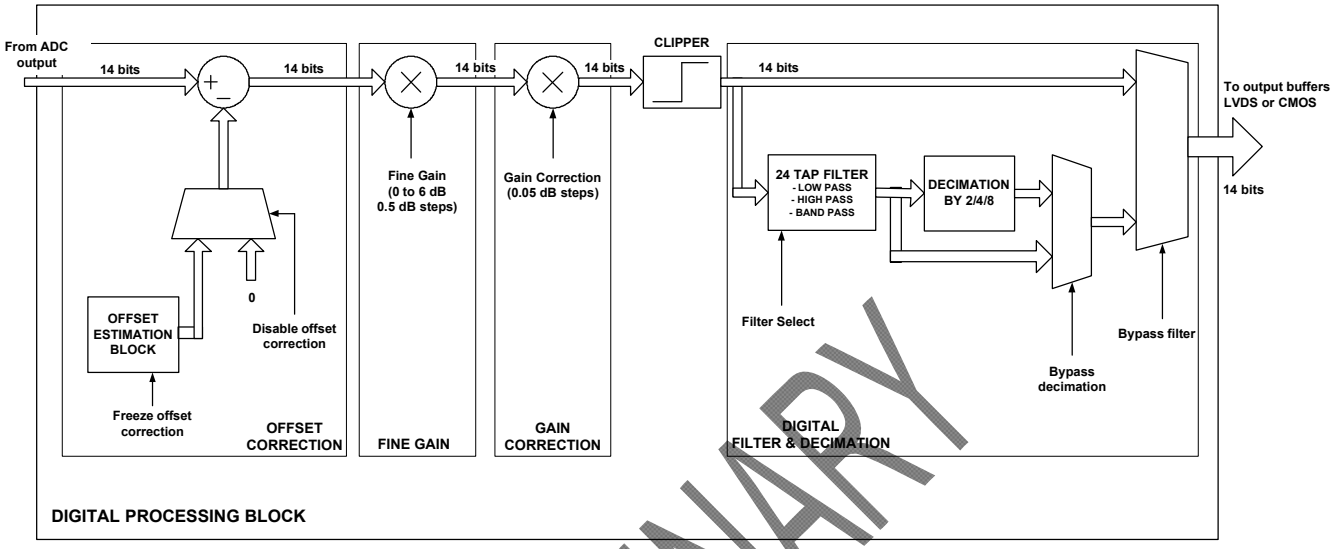


Figure 26 Digital Processing Block Diagram

Several common digital processing functions have been integrated in the device – offset correction, fine gain, gain correction decimation & digital filters. By default after reset, the digital processing block is bypassed & all its functions are disabled.

OFFSET CORRECTION

ADS62P4X has an internal offset correction algorithm that estimates and corrects dc offset up to +/-10mV. The correction can be enabled using the serial register bit <OFFSET LOOP EN>. Once enabled, the algorithm estimates the channel offset and applies the correction every clock cycle. The time constant of the correction loop is a function of the sampling clock frequency. The time constant can be controlled using register bits <OFFSET LOOP TC> as described in Table 9.

It is also possible to freeze the offset correction using the serial interface (<OFFSET LOOP FREEZE>). Once frozen, the offset estimation becomes inactive and the last estimated value is used for correction every clock cycle. Note that the offset correction is disabled by default after reset.

Figure 27 shows the time response of the offset correction algorithm, after it is enabled.

Table 9 Time Constant of Offset Correction Algorithm

<OFFSET LOOP TC> D6-D5-D4	Time constant (TC_{CLK}), number of clock cycles	Time constant, sec (=TC_{CLK} x 1/Fs) (1)
000	2^{27}	1.1
001	2^{26}	0.55
010	2^{25}	0.27
011	2^{24}	0.13
100	2^{28}	2.15
101	2^{29}	4.3
110	2^{27}	1.1
111	2^{27}	1.1

(1) Sampling frequency, Fs = 125 MSPS

TBD

Figure 27 Time Response of Offset Correction

GAIN CORRECTION

ADS62P4X includes option to make fine corrections to the ADC channel gain. The corrections can be done in steps of 0.05 dB, up to a maximum of 0.5 dB, using the register bits <GAIN CORRECTION>. Only positive corrections are supported and the same correction applies to both the channels.

Table 10 Gain Correction Values

<GAIN CORRECTION> D3-D2-D1-D0	Amount of correction, dB
0000	0
0001	+0.05
0010	+0.1
0011	+0.15
0100	+0.20
0101	+0.25
0110	+0.30
0111	+0.35
1000	+0.40
1001	+0.45
1010	+0.5
Other combinations	Unused

DECIMATION FILTER

ADS62P4X includes option to decimate the ADC output data with in-built low pass, high pass or band pass filters.

The decimation rates & the type of filter can be selected using register bits <DECIMATION RATE> & <DECIMATION FILTER TYPE>. Decimation rates of 2, 4 or 8 are available and either low pass, high pass or band pass filters can be selected (Table 11). By default, the decimation filter is disabled - use register bit <DECIMATION ENABLE> to enable it.

Table 11 Decimation Filter Modes (1)

Combination of decimation rates & filter types		Serial interface settings						
Decimation	Type of filter	<DECIMATION RATE>			<DECIMATION FILTER FREQ BAND>		<FILTER COEFF SELECT>	<DECIMATION ENABLE>
Decimate by 2	In-built low pass filter (pass band = 0 to Fs/4)	0	0	0	0	0	0	1
	In-built high pass filter (pass band = Fs/4 to Fs/2)	0	0	0	0	1	0	1
Decimate by 4	In-built low pass filter (pass band = 0 to Fs/8)	0	0	1	0	0	0	1
	In-built 2nd band pass filter (pass band = Fs/8 to Fs/4)	0	0	1	0	1	0	1
	In-built 3rd band pass filter (pass band = Fs/4 to 3Fs/8)	0	0	1	1	0	0	1
Decimate by 4	In-built last band pass filter (pass band = 3Fs/8 to Fs/2)	0	0	1	1	1	0	1
Decimate by 2	Custom filter (user programmable coefficients)	0	0	0	X	X	1	1
Decimate by 4	Custom filter (user programmable coefficients)	0	0	1	X	X	1	1
Decimate by 8	Custom filter (user programmable coefficients)	1	0	0	X	X	1	1
No decimation	Custom filter (user programmable coefficients)	0	1	1	X	X	1	0

Decimation filter equation

The decimation filter is implemented as 24-tap FIR with symmetrical coefficients (each coefficient is 12-bit signed).

The filter equation is:

$$y(n) = \left(\frac{1}{2^{11}}\right) \bullet (h0 \bullet x(n) + h1 \bullet x(n-1) + h2 \bullet x(n-2) + \ldots + h11 \bullet x(n-11) + h11 \bullet x(n-12) + \ldots + h1 \bullet x(n-22) + h0 \bullet x(n-23))$$

By setting the register bit <ODD TAP ENABLE> = 1, a 23-tap FIR is implemented:

$$y(n) = \left(\frac{1}{2^{11}}\right) \bullet (h0 \bullet x(n) + h1 \bullet x(n-1) + h2 \bullet x(n-2) + \ldots + h10 \bullet x(n-10) + h11 \bullet x(n-11) + h10 \bullet x(n-12) + \ldots + h1 \bullet x(n-21) + h0 \bullet x(n-22))$$

In the above equations,

h0, h1 …h11 are 12 bit signed representation of the coefficients,

x(n) is the input data sequence to the filter &

y(n) is the filter output sequence.

Pre-defined coefficients

The in-built filter types (low pass, high pass & band pass) use pre-defined coefficients. The frequency response of the in-built filters is shown in Figure 28 & Figure 29.

TBD

Figure 28 Decimate by 2 filter response

TBD

Figure 29 Decimate by 4 filter response

Table 12 Pre-defined coefficients for Decimate by 2 filters

Coefficients	Decimate by 2	
	Low pass filter	High pass filter
h0	23	-22
h1	-37	-65
h2	-6	-52
h3	68	30
h4	-36	66
h5	-61	-35
h6	35	-107
h7	118	38
h8	-100	202
h9	-197	-41
h10	273	-644
h11	943	1061

Table 13 Pre-defined coefficients for Decimate by 4 filters

Coefficients	Decimate by 4			
	Low pass filter	1st Band-pass filter	2nd Band-pass filter	High pass filter
h0	-17	-7	-34	32
h1	-50	19	-34	-15
h2	71	-47	-101	-95
h3	46	127	43	22
h4	24	73	58	-8
h5	-42	0	-28	-81
h6	-100	86	-5	106
h7	-97	117	-179	-62
h8	8	-190	294	-97
h9	202	-464	86	310
h10	414	-113	-563	-501
h11	554	526	352	575

Custom filter coefficients with decimation

The filter coefficients can also be programmed by the user (custom). For custom coefficients, set the register bit <FILTER COEFF SELECT> & load the coefficients (h0 to h11) in registers 1E to 2F using the serial interface (Table 14) as:

Register content = 12 bit signed representation of [real coefficient value x 2^{11}]

Custom filter coefficients without decimation

The filter with custom coefficients can also be used with the decimation mode disabled. In this mode, the filter implementation is 12-tap FIR:

$$y(n) = \left(\frac{1}{2^{11}}\right) \bullet (h6 \bullet x(n) + h7 \bullet x(n-1) + h8 \bullet x(n-2) + \ldots + h11 \bullet x(n-5) + h11 \bullet x(n-6) + \ldots + h7 \bullet x(n-10) + h6 \bullet x(n-11))$$

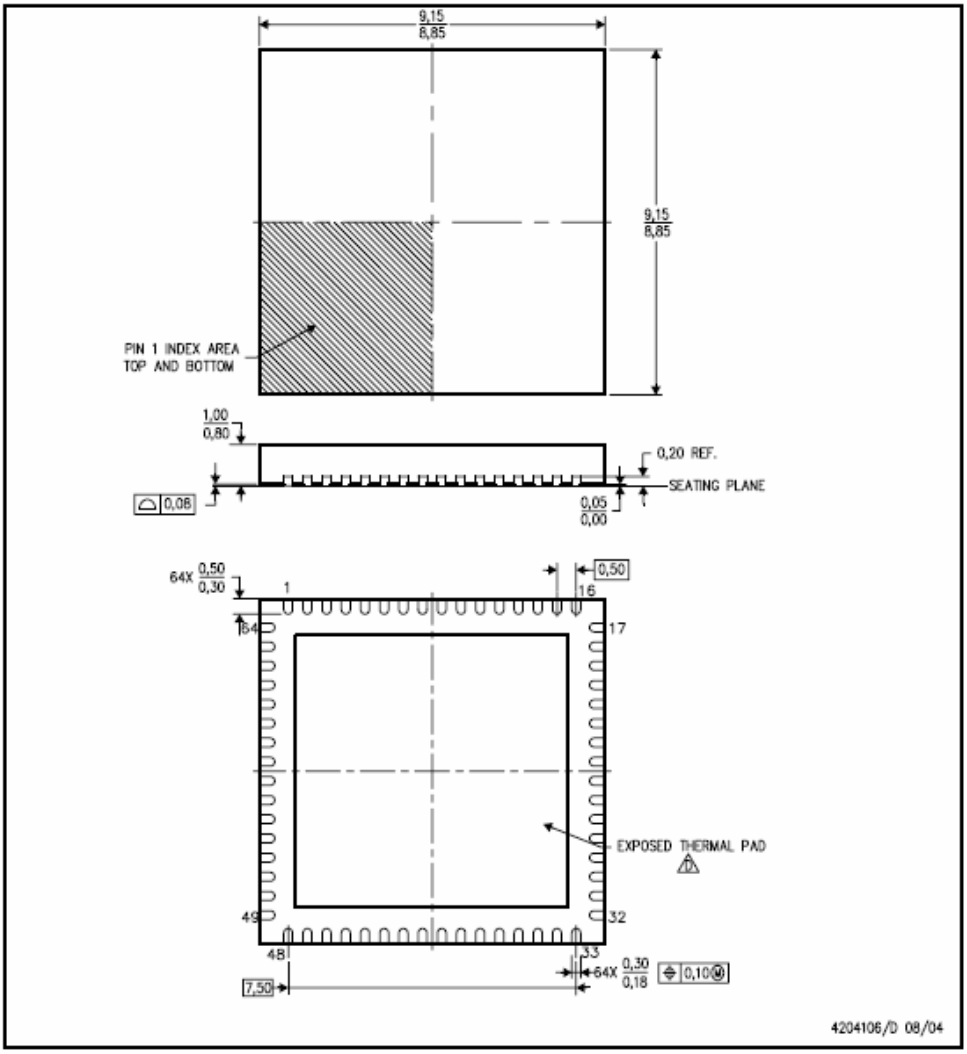
Table 14 Register Map for Custom FIR coefficients

REGISTER ADDRESS	REGISTER FUNCTIONS							
A7 - A0 in hex	D7	D6	D5	D4	D3	D2	D1	D0
1E	Coefficient h0 <7:0>							
1F	Coefficient h1 <3:0>				Coefficient h0 <11:8>			
20	Coefficient h1 <11:4>							
21	Coefficient h2 <7:0>							
22	Coefficient h3 <3:0>				Coefficient h2 <11:8>			
23	Coefficient h3 <11:4>							
24	Coefficient h4 <7:0>							
25	Coefficient h5 <3:0>				Coefficient h4 <11:8>			
26	Coefficient h5 <11:4>							
27	Coefficient h6 <7:0>							
28	Coefficient h7 <3:0>				Coefficient h6 <11:8>			
29	Coefficient h7 <11:4>							
2A	Coefficient h8 <7:0>							
2B	Coefficient h9 <3:0>				Coefficient h8 <11:8>			
2C	Coefficient h9 <11:4>							
2D	Coefficient h10 <7:0>							
2E	Coefficient h11 <3:0>				Coefficient h10 <11:8>			
2F	Coefficient h11 <11:4>							

PACKAGE INFORMATION

MECHANICAL DATA

RGC (S–PQFP–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration .
⚠ The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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PACKAGE OPTION ADDENDUM

22-Jan-2008

PACKAGING INFORMATION

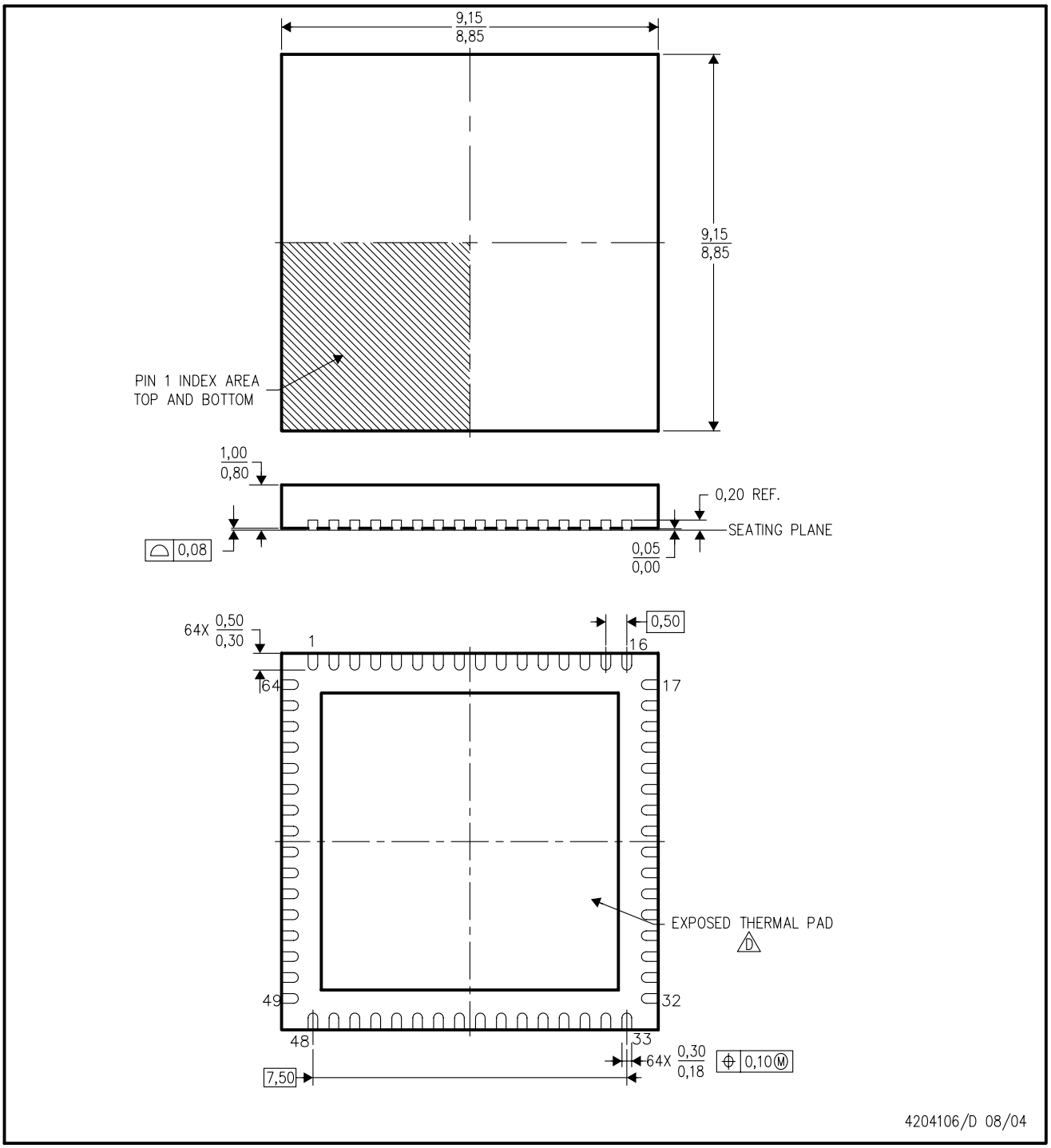
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS62P42IRGCR	PREVIEW	QFN	RGC	64	2500	TBD	Call TI	Call TI
ADS62P42IRGCT	PREVIEW	QFN	RGC	64	250	TBD	Call TI	Call TI
ADS62P43IRGCR	PREVIEW	QFN	RGC	64	2500	TBD	Call TI	Call TI
ADS62P43IRGCT	PREVIEW	QFN	RGC	64	250	TBD	Call TI	Call TI
ADS62P44IRGCR	PREVIEW	QFN	RGC	64	2500	TBD	Call TI	Call TI
ADS62P44IRGCT	PREVIEW	QFN	RGC	64	250	TBD	Call TI	Call TI
ADS62P45IRGCR	PREVIEW	QFN	RGC	64	2500	TBD	Call TI	Call TI
ADS62P45IRGCT	PREVIEW	QFN	RGC	64	250	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

RGC (S–PQFP–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration .
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

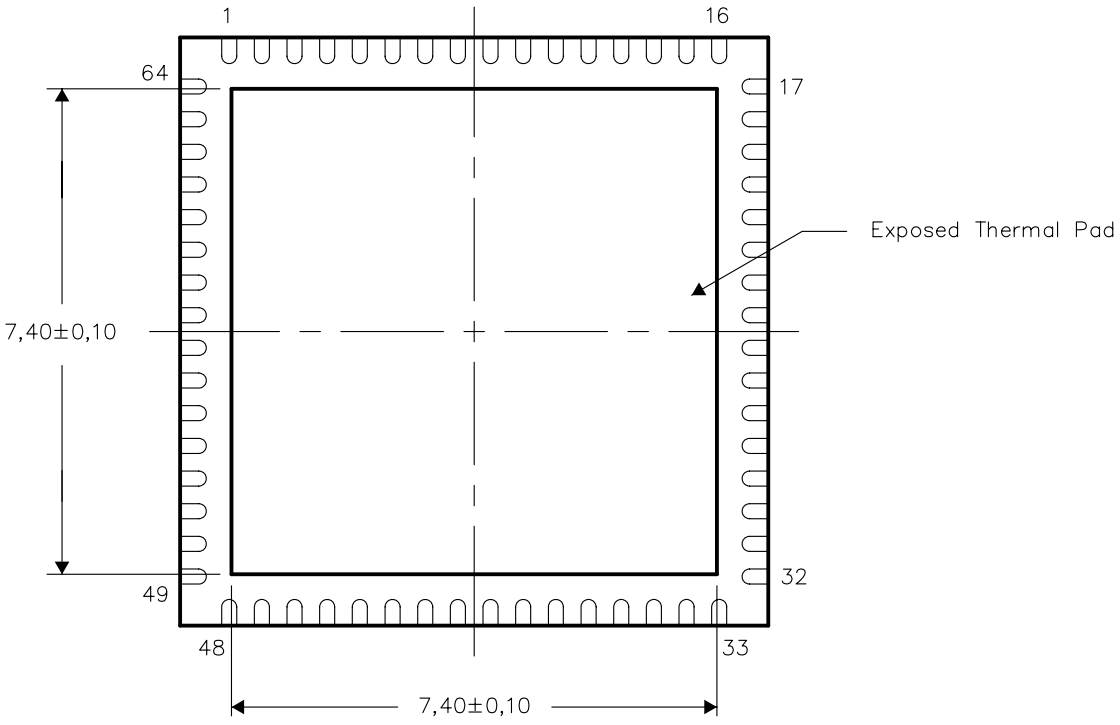
RGC (S–PQFP–N64)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

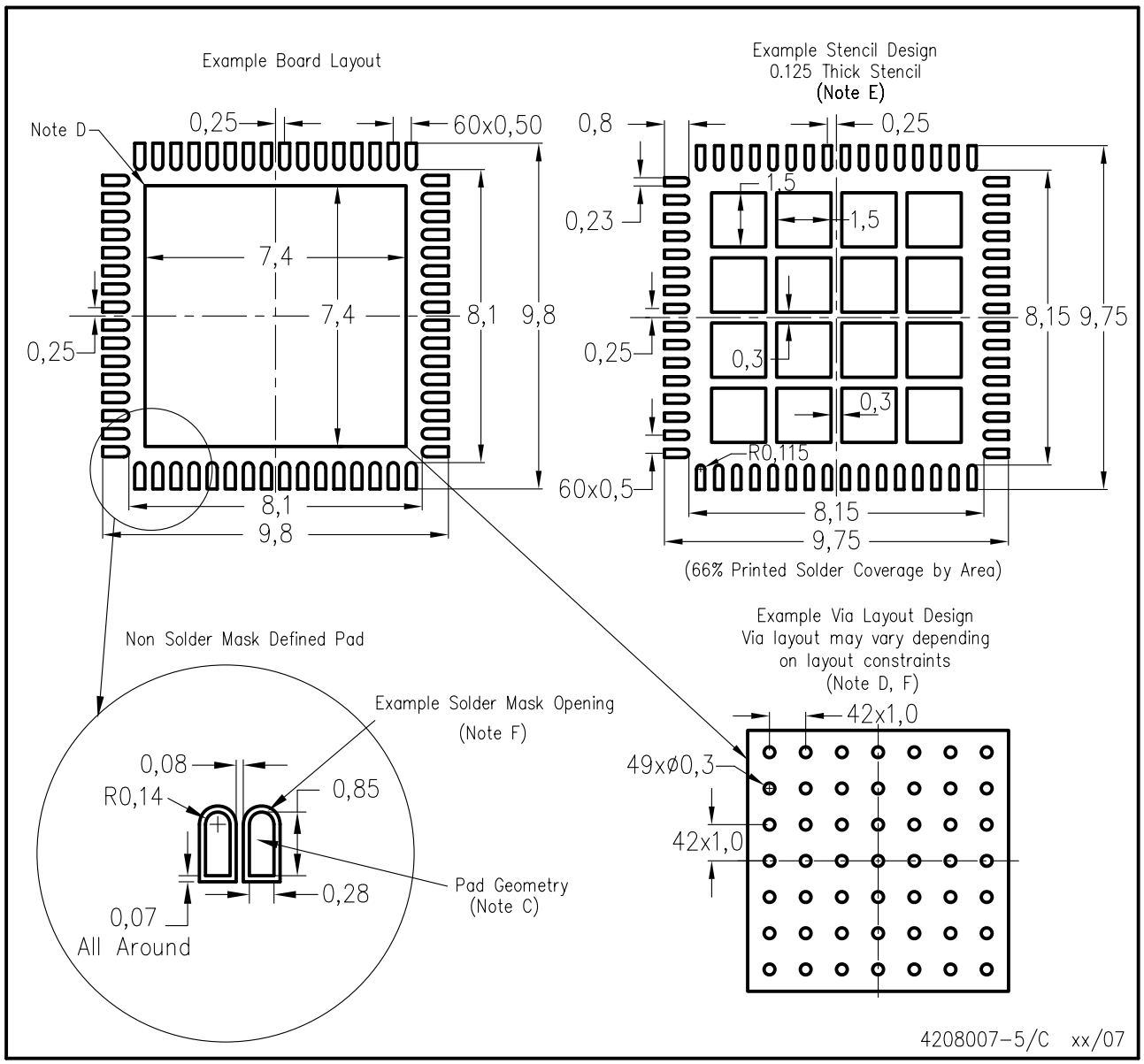


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGC (S–PQFP–N64)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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