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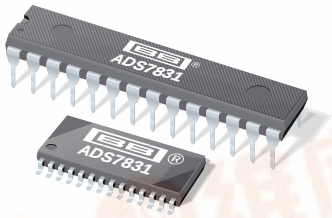


ADS7831

12-Bit 600kHz Sampling CMOS ANALOG-to-DIGITAL CONVERTER

FEATURES

- 600kHz THROUGHPUT RATE
- STANDARD ±2.5V INPUT RANGE
- 69dB min SINAD WITH 250kHz INPUT
- COMPLETE WITH S/H, REF, CLOCK, ETC.
- PARALLEL DATA w/LATCHES
- FULLY SPECIFIED –40°C TO +85°C
- 15MHz –3dB BANDWIDTH
- 28-PIN 0.3" PDIP AND SOIC

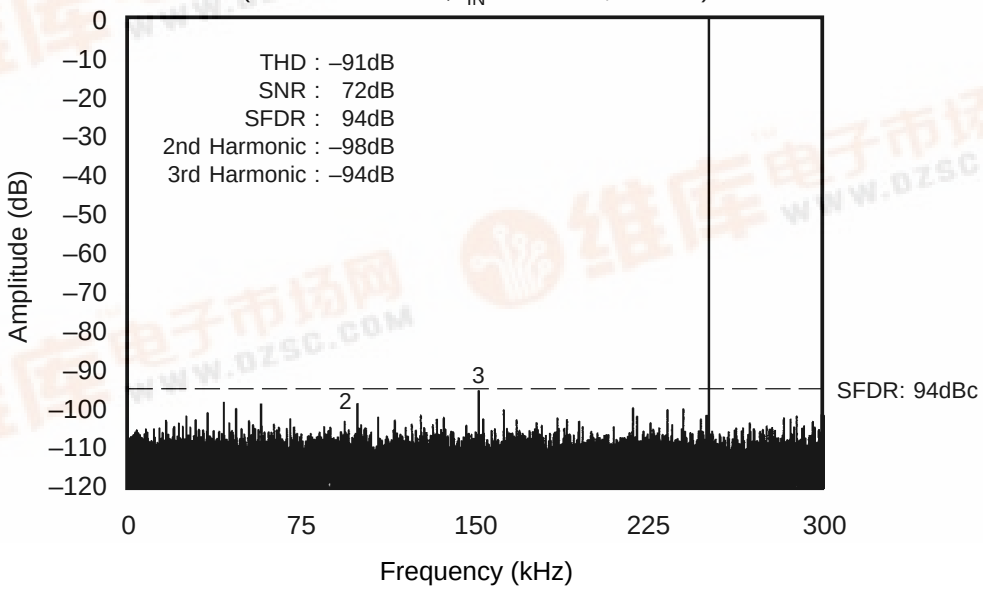
DESCRIPTION

The ADS7831 is a complete 12-bit sampling A/D using state-of-the-art CMOS structures. It contains a complete 12-bit capacitor-based SAR A/D with inherent S/H, reference, clock, interface for microprocessor use, and three-state output drivers.

The ADS7831 is specified at a 600kHz sampling rate, and guaranteed over the full temperature range. A ±2.5V input range and excellent Nyquist performance provide an optimum solution in ±5V supply systems.

The 28-pin ADS7831 is available in a plastic 0.3" DIP and in an SOIC, both fully specified for operation over the industrial –40°C to +85°C range.

FREQUENCY SPECTRUM
(16384 Point FFT; f_{IN} = 250kHz, –0.5dB)



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PDS-1275 Printed in U.S.A. March, 1995

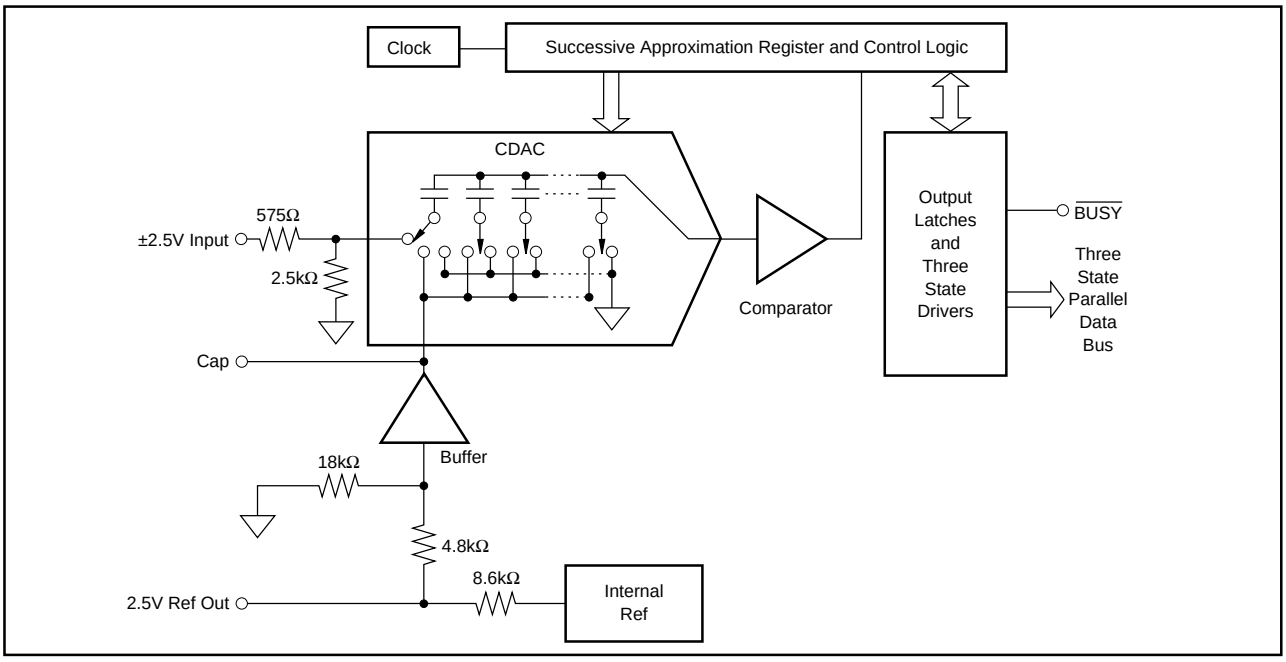
SPECIFICATIONS

At T_A = –40°C to +85°C, f_S = 600kHz, $+V_{DIG} = +V_{ANA}$ = +5V, $–V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

PARAMETER	CONDITIONS	ADS7831P, U			UNITS
		MIN	TYP	MAX	
RESOLUTION				12	Bits
ANALOG INPUT					
Voltage Range			±2.5		V
Impedance			3.1		kΩ
Capacitance			5		pF
THROUGHPUT SPEED					
Conversion Time			1.3		µs
Complete Cycle	Acquire & Convert			1.66	µs
Throughput Rate		600			kHz
DC ACCURACY					
Integral Linearity Error				±1	LSB[1]
Differential Linearity Error				±1	LSB
No Missing Codes			Guaranteed		
Total Unadjusted Error[2, 3]				±10	LSB
(Includes Bipolar Zero Error and Full Scale Error)					
Power Supply Sensitivity					
($+V_{DIG} = +V_{ANA} = V_D$)	+4.75V < V_D < +5.25V –5.25V < $–V_{ANA}$ < –4.75V			±5	LSB
AC ACCURACY					
Spurious-Free Dynamic Range	f_{IN} = 250kHz	77	87		dB[4]
Total Harmonic Distortion	f_{IN} = 250kHz		–85	–77	dB
Signal-to-(Noise+Distortion)	f_{IN} = 250kHz	69	71		dB
Signal-to-Noise	f_{IN} = 250kHz	69	72		dB
Usable Bandwidth[5]			1.6		MHz
Full-Power Bandwidth			15		MHz
SAMPLING DYNAMICS					
Aperture Delay			20		ns
Aperture Jitter			10		ps
Transient Response	FS Step		200		ns
Overvoltage Recovery[6]			250		ns
REFERENCE					
Reference Voltage		2.45	2.5	2.55	V
Reference DC Source Current			100		µA
(External load should be static)					
DIGITAL INPUTS					
Logic Levels					
V_{IL}		–0.3		+0.8	V
V_{IH}		+2.4		V_D + 0.3	V
I_{IL}	V_{IL} = 0V			±10	µA
I_{IH}	V_{IH} = 5V			±10	µA
DIGITAL OUTPUTS					
Data Format			Parallel 12-bits		
Data Coding			Binary Two's Complement		
V_{OL}	I_{SINK} = 1.6mA			+0.4	V
V_{OH}	I_{SOURCE} = 500µA	+2.8			V
Leakage Current	High-Z State, V_{OUT} = 0V to V_{DIG}			±5	µA
Output Capacitance	High-Z State			15	pF
DIGITAL TIMING					
Bus Access Time				62	ns
Bus Relinquish Time				83	ns
POWER SUPPLIES					
Specified Performance					
$+V_{DIG} = +V_{ANA}$		+4.75	+5	+5.25	V
$–V_{ANA}$		–5.25	–5	–4.75	V
$+I_{DIG}$			+16		mA
$+I_{ANA}$			+16		mA
$–I_{ANA}$			–12		mA
Power Dissipation	f_S = 600kHz		220	275	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C
Storage		–65		+150	°C
Thermal Resistance (θ_{JA})					
Plastic DIP			75		°C/W
SOIC			75		°C/W

NOTES: (1) LSB means Least Significant Bit. For the 12-bit, ±2.5V input ADS7831, one LSB is 1.22mV. (2) Measured with 50Ω in series with analog input. Adjustable to zero with external potentiometers. (3) Total unadjusted error is the worst case of –Full Scale or +Full Scale untrimmed deviation from ideal first and last code transitions and includes the effect of offset error. (4) All specifications in dB are referred to a full-scale ±2.5V input. (5) Usable Bandwidth defined as Full-Scale input frequency at which Signal-to-(Noise+Distortion) degrades to 60dB, or 10 bits of accuracy. 6) Recovers to specified performance after 2 x FS input over voltage.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Analog Inputs: V_{IN}	±25V
REF	$+V_{ANA}$ +0.3V to AGND2 –0.3V
CAP	Indefinite Short to AGND2
	Momentary Short to $+V_{ANA}$
Ground Voltage Differences: DGND, AGND1, AGND2	±0.3V
$+V_{ANA}$	+7V
$+V_{DIG}$ to $+V_{ANA}$	+0.3V
$+V_{DIG}$	7V
$–V_{ANA}$	–7V
Digital Inputs	–0.3V to $+V_{DIG}$ +0.3V
Maximum Junction Temperature	+165°C
Internal Power Dissipation	825mW
Lead Temperature (soldering, 10s)	+300°C

PACKAGE AND ORDERING INFORMATION[1]

MODEL	PACKAGE	PACKAGE DRAWING NUMBER
ADS7831P	28-Pin Plastic DIP	246
ADS7831U	28-Pin SOIC	217

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

ELECTROSTATIC DISCHARGE SENSITIVITY

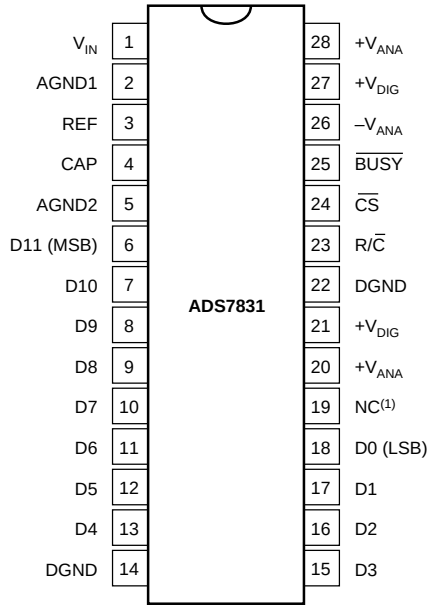
Electrostatic discharge can cause damage ranging from performance degradation to complete device failure. Burr-Brown Corporation recommends that all integrated circuits be handled and stored using appropriate ESD protection methods.

PIN ASSIGNMENTS

PIN #	NAME	DIGITAL I/O	DESCRIPTION
1	V_{IN}		Analog Input. Connect via 50Ω to analog input. Full-scale input range is ±2.5V.
2	AGND1		Analog Ground. Used internally as ground reference point. Minimal current flow.
3	REF		Reference Input/Output. Outputs internal reference of +2.5V nominal. Can also be driven by external system reference. In both cases, decouple to ground with a 0.1µF ceramic capacitor.
4	CAP		Reference Buffer Output. 10µF tantalum capacitor to ground. Nominally +2V.
5	AGND2		Analog Ground.
6	D11 (MSB)	O	Data Bit 11. Most Significant Bit (MSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
7	D10	O	Data Bit 10. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
8	D9	O	Data Bit 9. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
9	D8	O	Data Bit 8. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
10	D7	O	Data Bit 7. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
11	D6	O	Data Bit 6. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
12	D5	O	Data Bit 5. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
13	D4	O	Data Bit 4. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
14	DGND		Digital Ground.
15	D3	O	Data Bit 3. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
16	D2	O	Data Bit 2. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
17	D1	O	Data Bit 1. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
18	D0 (LSB)	O	Data Bit 0. Least Significant Bit (LSB) of conversion results. Hi-Z state when $\overline{CS}$ is HIGH, or when R/$\overline{C}$ is LOW, or when a conversion is in progress.
19			Not internally connected.
20	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 21, 27 and 28.
21	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 27 and 28.
22	DGND		Digital ground.
23	R/$\overline{C}$	I	Read/Convert Input. With $\overline{CS}$ LOW, a falling edge on R/$\overline{C}$ puts the internal sample/hold into the hold state and starts a conversion. With $\overline{CS}$ LOW and no conversion in progress, a rising edge on R/$\overline{C}$ enables the output data bits.
24	$\overline{CS}$	I	Chip Select. With R/$\overline{C}$ LOW, a falling edge on $\overline{CS}$ will initiate a conversion. With R/$\overline{C}$ HIGH and no conversion in progress, a falling edge on $\overline{CS}$ will enable the output data bits.
25	$\overline{BUSY}$	O	Busy Output. Falls when a conversion is started, and remains LOW until the conversion is completed and the data is latched into the output register. With $\overline{CS}$ LOW and R/$\overline{C}$ HIGH, output data will be valid when $\overline{BUSY}$ rises, so that the rising edge can be used to latch the data.
26	$-V_{ANA}$		Analog Negative Supply Input. Nominally –5V. Decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.
27	$+V_{DIG}$		Digital Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 28.
28	$+V_{ANA}$		Analog Positive Supply Input. Nominally +5V. Connect directly to pins 20, 21 and 27, and decouple to ground with 0.1µF ceramic and 10µF tantalum capacitors.

PIN CONFIGURATION

Top View **DIP/SOIC**

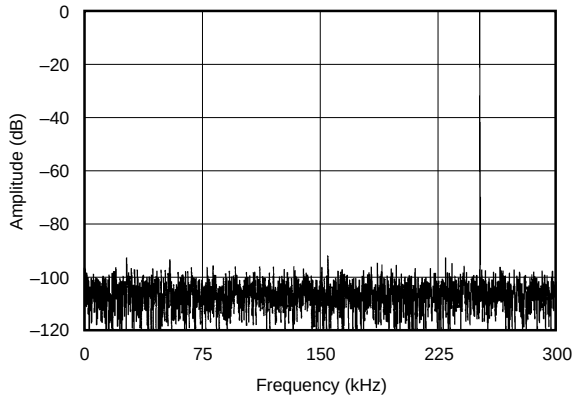


NOTE: (1) Not Internally Connected.

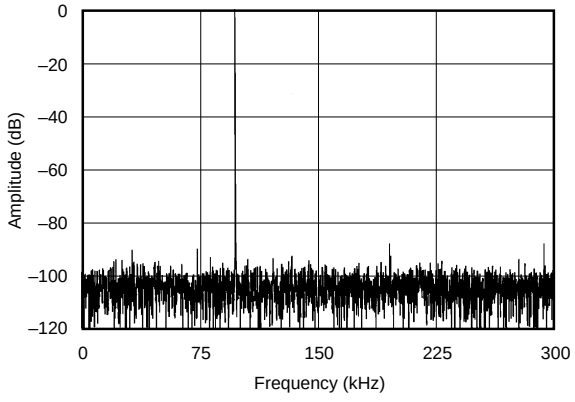
TYPICAL PERFORMANCE CURVES

T = +25°C, f_S =600kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.

FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 252kHz, –0.5dB)



FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 502kHz, –0.5dB)



FREQUENCY SPECTRUM
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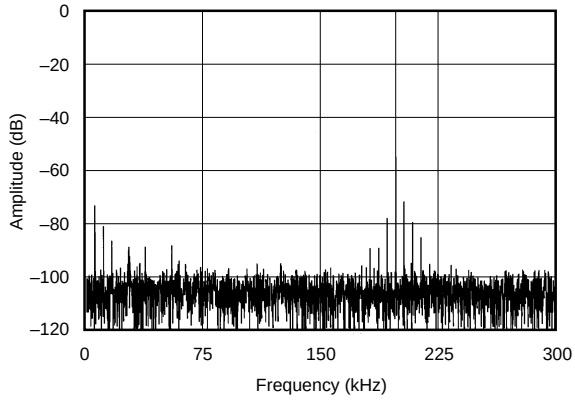
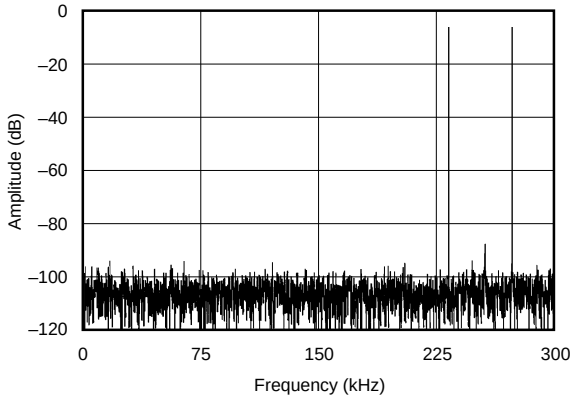
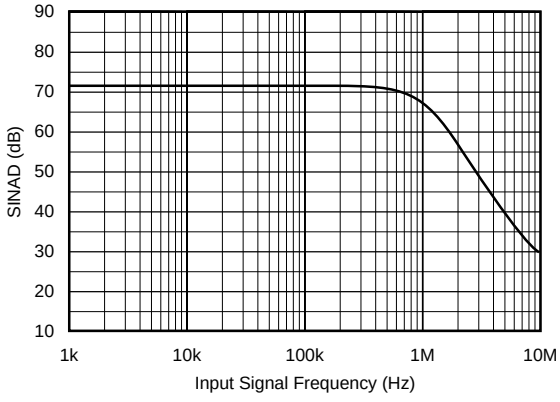


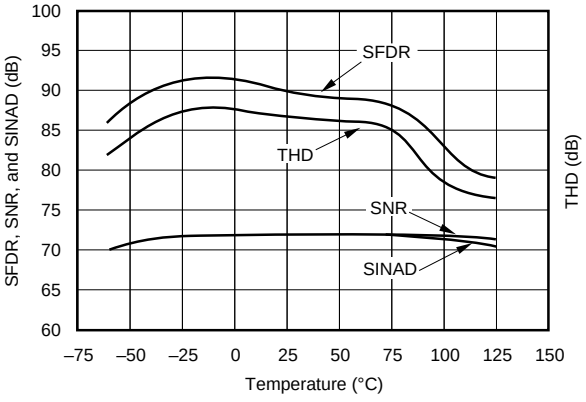
FREQUENCY SPECTRUM
(4096 Point FFT; $f1_{IN}$ = 232kHz, –6.5dB;
$f2_{IN}$ = 272kHz, –6.5dB)



SIGNAL-TO-(NOISE + DISTORTION)
vs INPUT FREQUENCY (f_{IN} = –0.5dB)

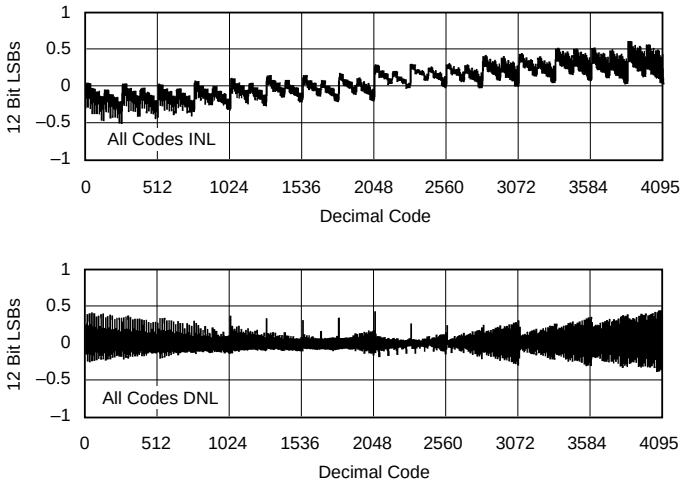


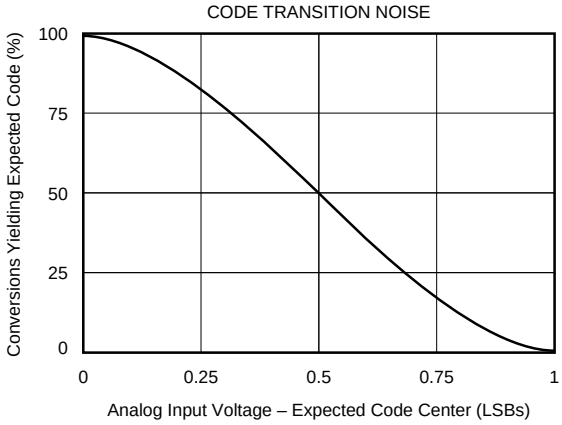
A.C. PARAMETERS vs TEMPERATURE
(f_{IN} = 250kHz, –0.5dB)

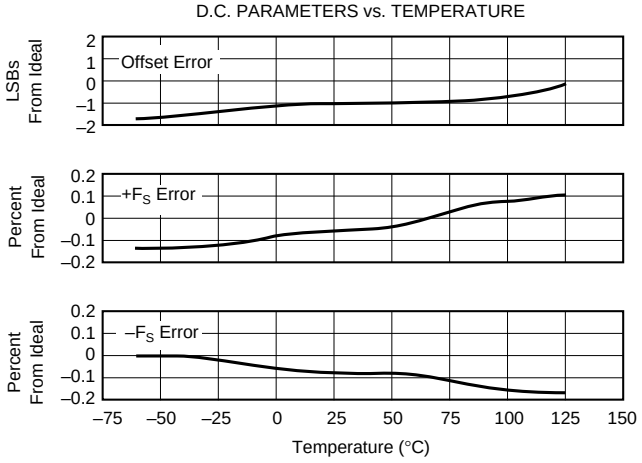


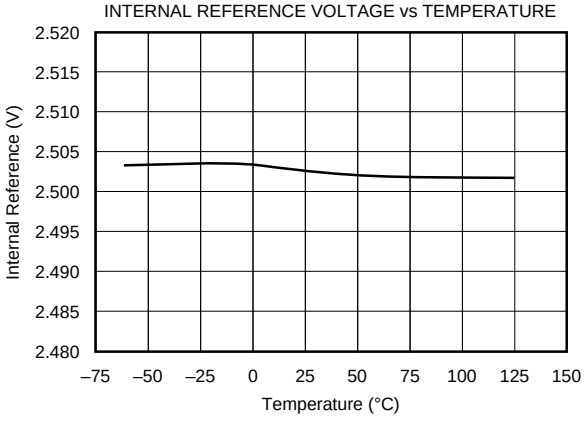
TYPICAL PERFORMANCE CURVES (CONT)

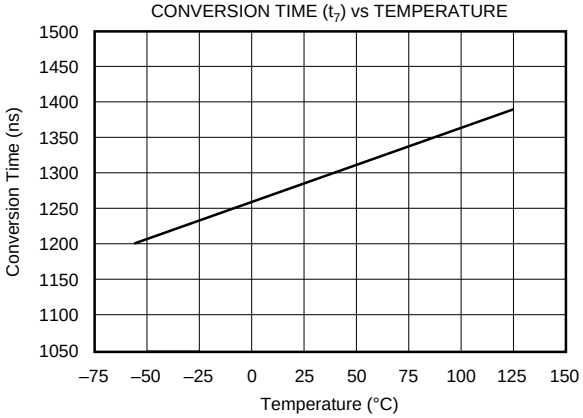
T = +25°C, f_S =600kHz, $+V_{DIG}$ = $+V_{ANA}$ = +5V, $-V_{ANA}$ = –5V, using internal reference and the 50Ω input resistor shown in Figure 4b, unless otherwise specified.











BASIC OPERATION

Figure 1 shows a basic circuit to operate the ADS7831. Taking R/$\overline{C}$ (pin 23) LOW for 40ns will initiate a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the output registers are updated. Data will be output in Binary Two's Complement with the MSB on D11 (pin 6). $\overline{BUSY}$ going HIGH can be used to latch the data. All convert commands will be ignored while $\overline{BUSY}$ is LOW.

The ADS7831 will begin tracking the input signal at the end of the conversion. Allowing 1.66µs between convert commands assures accurate acquisition of a new signal.

STARTING A CONVERSION

The combination of $\overline{CS}$ (pin 24) and R/$\overline{C}$ (pin 23) LOW for a minimum of 40ns immediately puts the sample/hold of the ADS7831 in the hold state and starts a conversion. $\overline{BUSY}$ (pin 25) will go LOW and stay LOW until the conversion is completed and the internal output register has been updated. All new convert commands during $\overline{BUSY}$ LOW will be ignored.

The ADS7831 will begin tracking the input signal at the end of the conversion. Allowing 1.66µs between convert commands assures accurate acquisition of a new signal. Refer to Table I for a summary of $\overline{CS}$, R/$\overline{C}$, and $\overline{BUSY}$ states and Figures 2 and 3 for timing parameters.

$\overline{CS}$ and R/$\overline{C}$ are internally OR'd and level triggered. There is not a requirement which input goes LOW first when initiating a conversion. If it is critical that $\overline{CS}$ or R/$\overline{C}$ initiate the conversion, be sure the less critical input is LOW at least 10ns prior to the initiating input.

To reduce the number of control pins, $\overline{CS}$ can be tied LOW using R/$\overline{C}$ to control the read and convert modes. Note that the parallel output will be active whenever R/$\overline{C}$ is HIGH and no conversion is in progress. See the **Reading Data** section and refer to Table I for control line functions for 'read' and 'convert' modes.

$\overline{CS}$	R/$\overline{C}$	$\overline{BUSY}$	OPERATION
1	X	X	None. Databus in Hi-Z state.
↓	0	1	Initiates conversion. Databus remains in Hi-Z state.
0	↓	1	Initiates conversion. Databus enters Hi-Z state.
0	1	↑	Conversion completed. Valid data from the most recent conversion on the databus.
↓	1	1	Enables databus with valid data from the most recent conversion.
↓	1	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	↑	0	Conversion in progress. Databus in Hi-Z state, enabled when the conversion is completed.
0	0	↑	Conversion completed. Valid data from the most recent conversion in the output register, but the output pins D11-D0 remain tri-stated.
X	X	0	New convert commands ignored. Conversion in progress.

Table I. Control Line Functions for 'read' and 'convert'.

DESCRIPTION	ANALOG INPUT	DIGITAL INPUT	
Full Scale Range	±2.5V	BINARY TWO'S COMPLEMENT	
Least Significant Bit (LSB)	1.22mV	BINARY CODE	HEX CODE
+Full Scale (2.5V – 1LSB)	2.499V	0111 1111 1111	7FF
Midscale	0V	0000 0000 0000	000
One LSB below Midscale	–1.22mV	1111 1111 1111	FFF
–Full Scale	–2.5V	1000 0000 0000	800

TABLE II. Ideal Input Voltages and Output Codes.

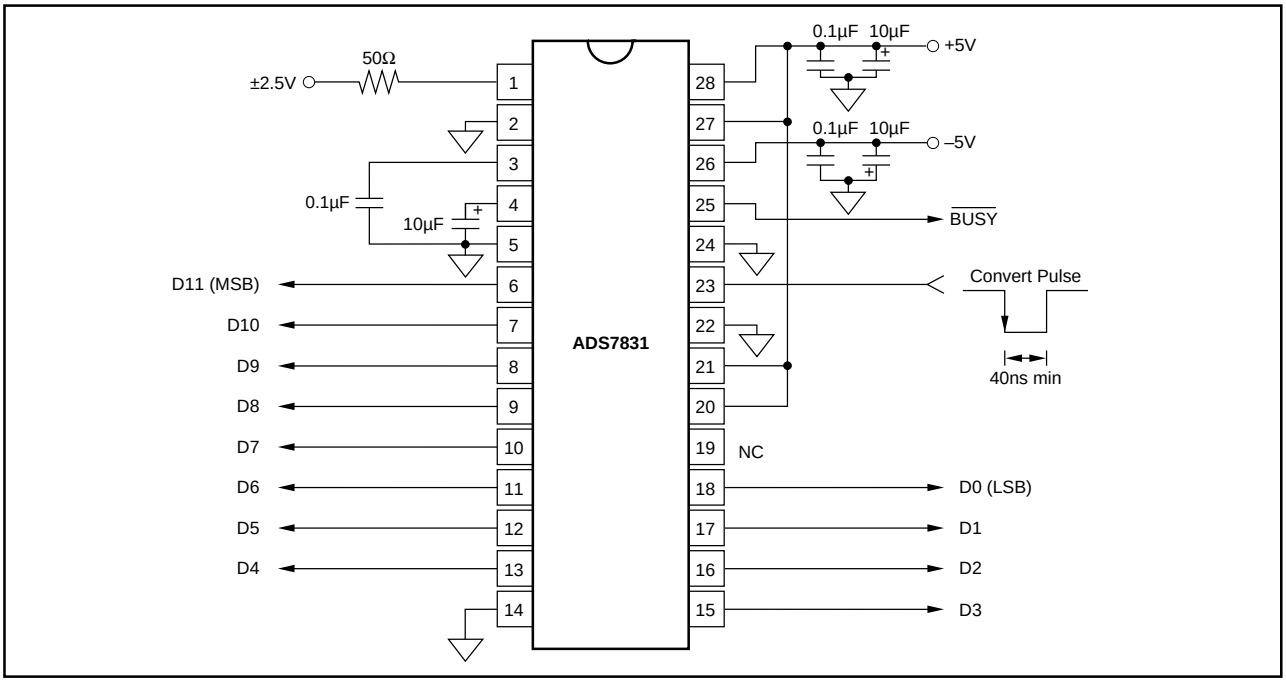


FIGURE 1. Basic Operation

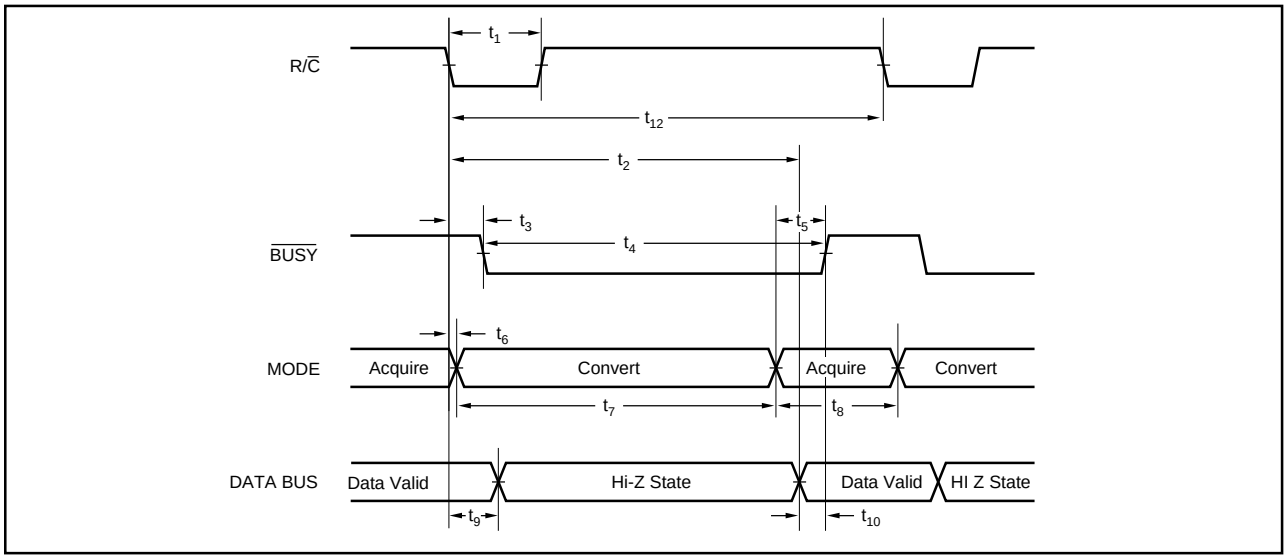


FIGURE 2. Conversion Timing with Outputs Enabled After Conversion ($\overline{CS}$ Tied Low).

READING DATA

The ADS7831 outputs full parallel data in Binary Two's Complement data output format. The parallel output will be active when R/$\overline{C}$ (pin 23) is HIGH, $\overline{CS}$ (pin 24) is LOW, and no conversion is in progress. Any other combination will tri-state the parallel output. Valid conversion data can be read in a full parallel, 12-bit word on D11-D0 (pins 6-13 and 15-18). Refer to Table II for ideal output codes.

After the conversion is completed and the output registers have been updated, $\overline{BUSY}$ (pin 25) will go HIGH. Valid data from the most recent conversion will be available on D11-D0 (pins 6-13 and 15-18). $\overline{BUSY}$ going HIGH can be used to latch the data. Refer to Table III and Figures 2 and 3.

Note: For best performance, the external data bus connected to D11-D0 should not be active during a conversion. The switching noise of the external asynchronous data signals can cause digital feed through degrading the converter's performance.

The number of control lines can be reduced by tieing $\overline{CS}$ LOW while using R/$\overline{C}$ to initiate conversions and activate the output mode of the converter. See Figure 2.

ANALOG INPUT

The ADS7831 has a ±2.5V input range. Figures 4a and 4b show the necessary circuit connections for the ADS7831 with and without external trim. Offset and full scale error(1) specifications are tested and guaranteed with the 50Ω resistor shown in Figure 4b. This external resistor makes it possible to trim the offset ±12mV using R_1 and P_1 as shown in Figure 4a. This resistor may be left out if the offset and gain errors will be corrected in software or if they are negligible in regards to the particular application. See the **Calibration** section of the data sheet for details.

The nominal input impedance of 3.125kΩ results from the combination of the internal resistor network shown on page 3 of this data sheet and the external 50Ω resistor. The input resistor divider network provides inherent over-voltage protection guaranteed to at least ±25V. The 50Ω, 1% resistor does not compromise the accuracy or drift of the converter. It has little influence relative to the internal resistors, and tighter tolerances are not required.

Note: The values shown for the internal resistors are for reference only. The exact values can vary by ±30%. This is true of all resistors internal to the ADS7831. Each resistive divider is trimmed so that the proper division is achieved.

NOTE: (1) Full scale error includes offset and gain errors measured at both +FS and –FS.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Convert Pulse Width	40			ns
t_2	Data Valid Delay After Start of Conversion		1310	1460	ns
t_3	$\overline{BUSY}$ Delay From Start of Conversion		75	125	ns
t_4	$\overline{BUSY}$ LOW		1300	1440	ns
t_5	$\overline{BUSY}$ Delay After End of Conversion		90		ns
t_6	Aperture Delay		20		ns
t_7	Conversion Time		1285	1400	ns
t_8	Acquisition Time		200	250	ns
t_7 & t_8	Throughput Time		1485	1650	ns
t_9	Bus Relinquish Time	10	55	83	ns
t_{10}	$\overline{BUSY}$ Delay After Data Valid	20	65	100	ns
t_{11}	R/$\overline{C}$ to $\overline{CS}$ Setup Time	10			ns
t_{12}	Time Between Conversions	1660			ns
t_{13}	Bus Access Time	10	30	62	ns

TABLE III. Timing Specifications (T_{MIN} to T_{MAX}).

CALIBRATION

The ADS7831 can be trimmed in hardware or software. The offset should be trimmed before the gain since the offset directly affects the gain.

Hardware Calibration

To calibrate the offset and gain of the ADS7831, install the proper resistors and potentiometers as shown in Figure 4a. The calibration range is ±12mV for the offset and ±30mV for full scale.

Potentiometer P_1 and resistor R_1 form the offset adjust circuit and P_2 and R_2 the gain adjust circuit. The exact values are not critical. R_1 and R_2 should not be made any larger than the value shown. They can easily be made smaller to provide increased adjustment range. Reducing these below 15% of the indicated values could begin to adversely affect the operation of the converter.

P_1 and P_2 can also be made larger to reduce power dissipation. However, larger resistances will push the useful adjustment range to the edges of the potentiometer. P_1 should probably not exceed 20kΩ and P2 100kΩ in order to maintain reasonable sensitivity.

Software Calibration or No Calibration

The ADS7831 does not require external resistors for its basic operation. However, the component is designed to be used with an external 50Ω resistor on the input, and the specifications apply to this condition. If this resistor is not used, the only specification that will be affected is total unadjusted error.

With the 50Ω resistor, the nominal input voltage range is ±2.5V and the total unadjusted error is ±10LSBs guaranteed. Without the 50Ω resistor, the nominal input voltage range will be ±2.46V and the total unadjusted error is not guaranteed. While it will typically be much less, the total unadjusted error could be as high as ±20LSBs.

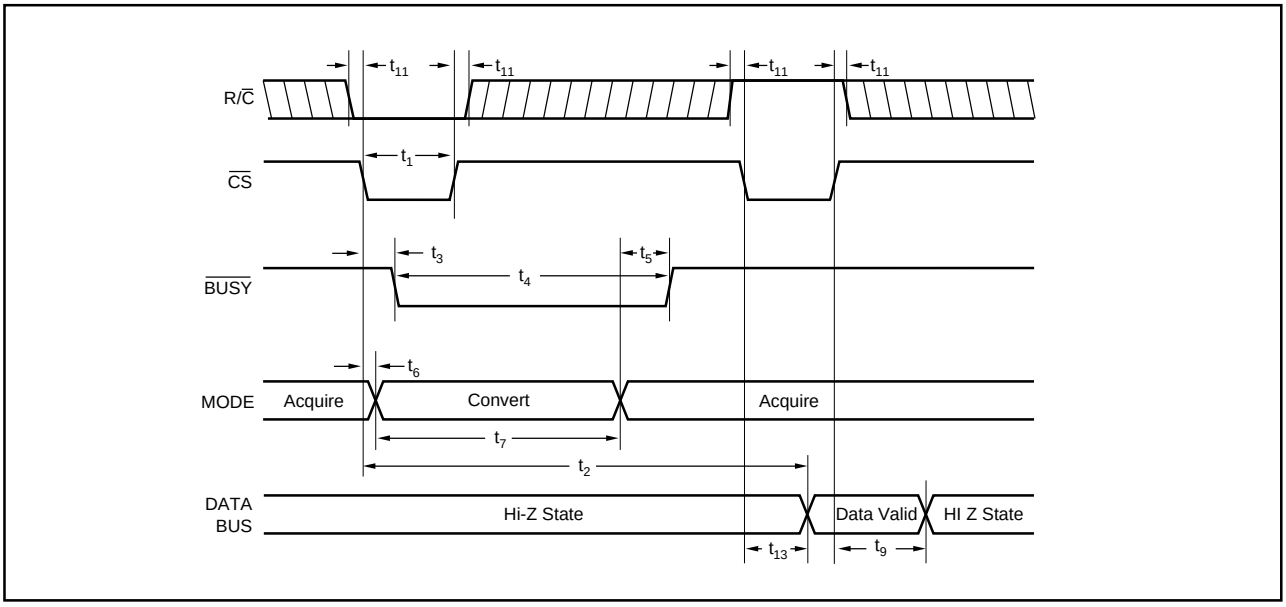


FIGURE 3. Using $\overline{CS}$ to Control Conversion and Read Timing.

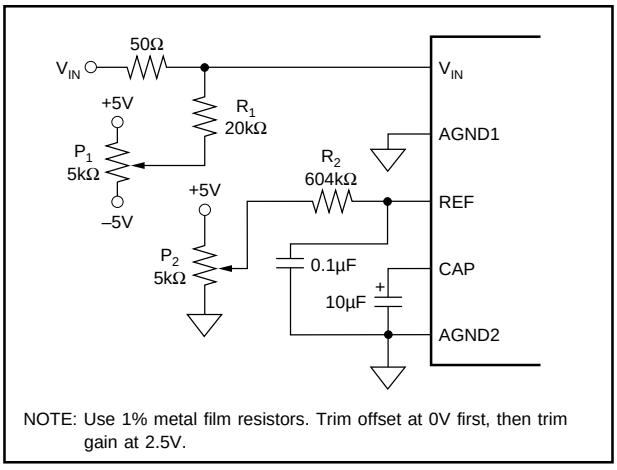


FIGURE 4a. Circuit Diagram With External Hardware Trim.

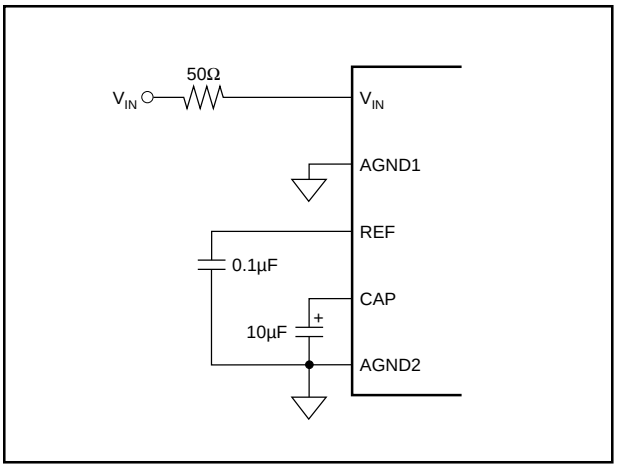


FIGURE 4b. Circuit Diagram Without External Hardware Trim.

REFERENCE

REF

REF (pin 3) is the output for the internal 2.5V reference. A 0.1µF capacitor should be connected as close to the REF pin as possible. The capacitor and the output resistance of REF create a low pass filter to band limit noise on the reference. Using a smaller value capacitor will introduce more noise to the reference degrading the SNR and SINAD. The REF pin should not be used to drive external AC or DC loads.

CAP

CAP (pin 4) is the output of the internal reference buffer. A 10µF capacitor should be placed as close to the CAP as possible to provide optimum switching currents for the CDAC throughout the conversion cycle and compensation for the output of the buffer. Using a capacitor any smaller than 2.2µF can cause the output buffer to oscillate and may not have sufficient charge for the CDAC. Capacitor values larger than 10µF will have little effect on improving performance. The voltage on the CAP pin is approximately 2V when using the internal reference, or 80% of an externally supplied reference.

LAYOUT

POWER

The ADS7831 uses the majority of its power for analog and static circuitry and it should be considered as an analog component. For optimum performance, tie the analog and digital +5V power pins to the same +5V power supply and tie the analog and digital grounds together.

For best performance, the ±5V supplies can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If ±12V or ±15V supplies are present, simple regulators can be used. The +5V power for the A/D should be separate from the +5V used for the system's digital logic. Connecting V_{DIG} (pin 27) directly to a digital supply can reduce converter performance due to switching noise from the digital logic.

Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both V_{DIG} and V_{ANA} should be tied to the same +5V source.

GROUNDING

Three ground pins are present on the ADS7831. DGND (pin 22) is the digital supply ground. AGND2 (pin 5) is the analog supply ground. AGND1 (pin 2) is the ground which all analog signals internal to the A/D are referenced. AGND1 is more susceptible to current induced voltage drops and must have the path of least resistance back to the power supply.

All the ground pins of the ADS should be tied to the analog ground plane, separated from the system's digital logic ground, to achieve optimum performance. Both analog and digital ground planes should be tied to the "system" ground as near to the power supplies as possible. This helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample hold on many CMOS A/D converters release a significant amount of charge injection which can cause the driving op amp to oscillate. The FET switch on the ADS7831, compared to FET switches on other CMOS A/D converters, releases 5%—10% of the charge. There is also a resistive front end which attenuates any charge which is released. The end result is a minimal requirement for the op amp on the front end. Any op amp sufficient for the signal in an application will be sufficient to the drive the ADS7831.

The resistive front end of the ADS7831 also provides a guaranteed ±25V over voltage protection. In most cases, this eliminates the need for external input protection circuitry.

INTERMEDIATE LATCHES

The ADS7831 does have tri-state outputs for the parallel port, but intermediate latches should be used if the bus will be active during conversions. If the bus is not active during conversions, the tri-state outputs can be used to isolate the A/D from other peripherals on the same bus.

Intermediate latches are beneficial on any monolithic A/D converter. The ADS7831 has an internal LSB size of 610µV. Transients from fast switching signals on the parallel port, even when the A/D is tri-stated, can be coupled through the substrate to the analog circuitry causing degradation of converter performance.