Isolated Half-Bridge Driver with Integrated Isolated High-Side Supply

PRELIMINARY TECHNICAL DATA

ADuM6132

FEATURES

- Integrated Isolated High Side Supply
- 250mW Isolated DC/DC converter
- 200mA Output Sink Current, 200mA Output Source Current
- High common-mode transient immunity: > 25 kV/µs
- High temperature operation: 105°C
- Wide body SOIC 16-lead package
- Safety and regulatory approvals (pending)
  - UL recognition
    - 3750 V rms for 1 minute per UL 1577
  - CSA component acceptance notice #5A
    - CSA/IEC 60950-1, 400 V_{RMS}
  - VDE certificate of conformity
    - DIN V VDE 0884-10 (VDE V 0884-10):2006-12
    - V_{IORM} = 560 V peak

APPLICATIONS

- MOSFET/IGBT Gate Drive
- Motor Drives
- Solar Panel Inverters
- Power Supplies

GENERAL DESCRIPTION

The ADuM6132[1] is an isolated half-bridge gate driver that employs Analog Devices' *i*Coupler® technology to provide an isolated high-side driver with an integrated 300 mW high-side supply. This supply, provided by an internal isolated DC/DC converter powers not only the ADuM6132's high-side output but also any external buffer circuitry that would commonly be used with the ADuM6132. This eliminates the cost, space, and performance difficulties associated with external supply configurations such as a bootstrap circuitry. The architecture isolates the high side channel and high side power from the control and low side interface circuitry. Care has been taken to ensure close matching between the high and low side driver timing characteristics, reduces the need for dead time margin.

In comparison to gate drivers employing high voltage level translation methodologies, the ADuM6132 offers the benefit of true, galvanic isolation. The differential voltage between high and low side channels can be as high as 1131V in some configurations (see Table 7).

[1] Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075 329. Other patents pending.

FUNCTIONAL BLOCK DIAGRAM

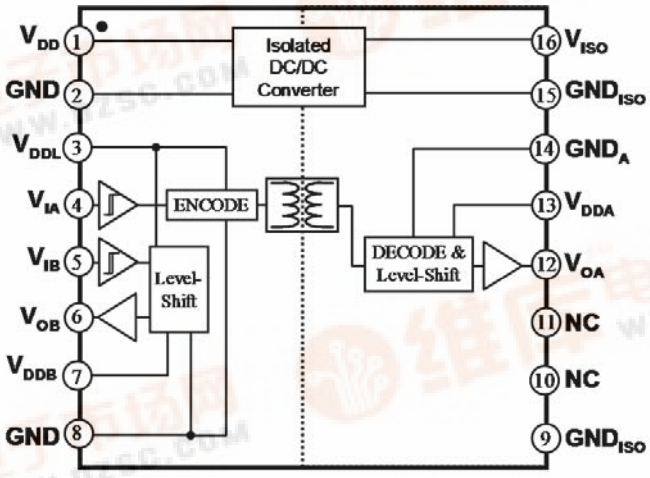

Figure 1. ADuM6132 Functional Block Diagram

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground. $4.5 \le V_{DD} = V_{DDL} \le 5.5$ V, $12.5 \le V_{DDB} \le 17.0$ V, $V_{DDA} = V_{ISO}$. All min/max specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at $T_A = 25°C$, $V_{DD} = V_{DDL} = 5.0V$, $V_{DDB} = 15$ V, $V_{DDA} = V_{ISO}$.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Isolated Power Supply						
Input Current, Quiescent	$I_{DD(Q)}$			250	mA	I_{ISO}=0, DC signal inputs
Input Current, Loaded	I_{DD}			350	mA	$I_{ISO} = I_{ISO(max,)}$
Maximum Output Current[1]	$I_{ISO(max)}$	22			mA	$12.5 \le V_{ISO} \le 17.0$
Output Voltage	V_{ISO}	12.5	15	17	V	$0 \le I_{ISO} \le 22$
Logic Supply						
Input Current	I_{DDL}		1.8	3.0	mA	
Output Supplies, Channel A or Channel B[2]						
Supply Current, Quiescent	$I_{DDA(Q)}$, $I_{DDB(Q)}$		1.0	2	mA	
Supply Current, f_{IN}=20kHz	$I_{DDA(20)}$, $I_{DDB(20)}$		1.1	2.1	mA	C_L = 200 pF
Supply Current, f_{IN}=100kHz	$I_{DDA(100)}$, $I_{DDB(100)}$		1.3	2.3	mA	C_L = 200 pF
Supply Current, f_{IN}=1000kHz	$I_{DDA(1000)}$, $I_{DDB(1000)}$		4.5	5.5	mA	C_L = 200 pF
Logic Inputs, Channel A or Channel B						
Input Current	I_{IA}, I_{IB}	−10	0.01	10	µA	$0 \le V_{IA}$, $V_{IB} \le 5.5V$
Logic High Input Voltage	V_{IAH}, V_{IBH}	0.7 xV_{DDL}			V	
Logic Low Input Voltage	V_{IAL}, V_{IBL}			0.3 x V_{DDL}	V	
Outputs, Channel A or Channel B						
Channel A High Level Output Voltage	V_{OAH}	V_{DDA} −0.1			V	I_{OAH} = -1 mA
Channel B High Level Output Voltage	V_{OBH}	V_{DDB} −0.1			V	I_{OBH} = -1 mA
Low Level Output Voltages	V_{OAL},V_{OBL}			0.1	V	I_{OAL}, I_{OBL} = +1 mA
High Level Output Current, Peak[3]	I_{OAH}, I_{OBH}	200			mA	
Low Level Output Current, Peak[3]	I_{OAL}, I_{OBL}	200			mA	
Undervoltage Lockout, V_{DDA} or V_{DDB} Supply						
Positive going threshold	V_{DDAUV+}, V_{DDBUV+}	11.0	11.7	12.3	V	
Negative going threshold	V_{DDAUV-}, V_{DDBUV-}	10.0	10.7	11.2	V	
Hysteresis	V_{DDBUVH}, V_{DDBUVH}	0.8	1.0	1.2	V	
Undervoltage Lockout, V_{DDL} Supply						
Positive going threshold	V_{DDLUV+}	3.5		4.2	V	
Negative going threshold	V_{DDLUV-}	3.0		3.7	V	
Hysteresis	V_{DDLUVH}	0.3			V	
SWITCHING SPECIFICATIONS						
Minimum Pulse Width[4]	PW			50	ns	C_L = 200 pF
Maximum Switching Frequency[5]	f_{IN}	1000			KHz	C_L = 200 pF
Propagation Delay[6]	t_{PHL}, t_{PLH}	40	60	100	ns	C_L = 200 pF
Change versus temperature			100		ps/°C	
Pulse-Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	PWD			10	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising or Falling Matching Edge Polarity[7]	t_{M2}			20	ns	C_L = 200 pF
Channel-to-Channel Matching, Rising vs. Falling Opposite Edge Polarity[8]	t_{M1}			20	ns	C_L = 200 pF
Part-to-Part Matching[9]				60	ns	C_L = 200 pF
Output Rise Time (10%–90%)	t_R			15	ns	C_L = 200 pF
Output Fall Time (10%–90%)	t_F			15	ns	C_L = 200 pF

[1] The maximum output current is the maximum isolated supply current that the ADuM6132 can provide. This current supports external loads as well as the needs of the ADuM6132 Channel A output circuitry. This is achieved via external connection of V_{ISO} to V_{DDA} and GND_{ISO} to GND_A (Figure 3). The net current available to power external loads is the ADuM6132 output current I_{ISO} less the Channel A supply current I_{DDA}.

[2] I_{DDA} is supplied by the output of the integrated isolated dc/dc power as described in Footnote 1 above. I_{DDB} is supplied by external power connection to V_{DDB} pin. See Figure 3.

[3] Duration less than 1 second. Average output current must conform to the limit shown under the Absolute Maximum Ratings.

[4] The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed. Operation below the minimum pulse width is not recommended.

[5] The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed. Operation beyond the maximum frequency is not recommended since high switching rates can cause droop in the output supply voltage.

[6] t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

[7] "Channel-to-channel matching, rising or falling matching edge polarity" is the magnitude of the propagation delay difference between two channels of the same part when both inputs are either both rising or falling edges. The loads on each channel are equal.

[8] "Channel-to-channel matching, rising vs. falling opposite edge polarity" is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and one input is a falling edge. The loads on each channel are equal.

[9] Part-to-part matching is the magnitude of the propagation delay difference between the same channels of two different parts. This includes rising vs. rising, falling vs. falling, or rising vs. falling edges. The supply voltages, temperatures, and loads of each part are equal.

PACKAGE CHARACTERISTICS

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input Side- High Side Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input to High Side Output)[1]	C_{I-O}		2.0		pF	
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		45		°C/W	4-layer PC board

[1] The device is considered a two-terminal device: Pins 1-8 are shorted together, and Pins 9-16 are shorted together.

REGULATORY INFORMATION

The ADuM6132 will be approved by the organizations listed in Table 3.

Table 3.

UL (pending)	CSA (Pending)	VDE (Pending)
Recognized under 1577 component recognition program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Double/reinforced insulation, 3750 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms maximum working voltage	Reinforced insulation, 560 V peak
		Complies with DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01, DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000, DIN V VDE 0884-10 (VDE V 0884-10):2006-12
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL1577, each ADuM6132 is proof tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM6132 is proof tested by applying an insulation test voltage ≥1050 V peak for 1 sec (partial discharge detection limit = 5 pC). The * marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 4.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		3750	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	8.0 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	8.0 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

The ADuM6132 is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The * marking on the package denotes DIN V VDE V 0884-10 approval.

Table 5.

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	$V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	$V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC		672	V peak
Highest Allowable Overvoltage	Transient overvoltage, $t_{TR} = 10$ sec	V_{TR}	6000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure; see			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	265	mA
Side 2 Current		I_{S2}	335	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

RECOMMENDED OPERATING CONDITIONS

Table 6.

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD}	4.5	5.5	V
Channel B Supply Voltage[1]	V_{DDB}	12.5	17	V
Input Signal Rise and Fall Times			1	ms
Common-Mode Transient Immunity, Input-to-Output		−50	+50	kV/µs

[1] All voltages are relative to their respective ground.

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	−55	+150	°C
Ambient Operating Temperature	T_A	−40	+105	°C
Input Supply Voltage[1]	V_{DD}	−0.5	+7.0	V
Channel B Supply Voltage[1]	V_{DDB}	−0.5	+27	V
Input Voltage[1]	V_{IA}, V_{IB}	−0.5	V_{DDI} + 0.5	V
Output Voltage[1]	V_{OA}, V_{OB}	−0.5	V_{ISO} + 0.5, V_{DDB} + 0.5	V
Output DC Current	I_{OA}, I_{OB}	−100	+100	mA
Common-Mode Transients[2]		−100	+100	kV/µs

[1] All voltages are relative to their respective ground.
[2] Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the Absolute Maximum Ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ambient temperature = 25°C, unless otherwise noted.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 7. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Voltage, Bipolar Waveform	565	V peak	50-year minimum lifetime
AC Voltage, Unipolar Waveform		V peak	
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	1131	V peak	Maximum approved working voltage per IEC 60950-1

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the **Insulation Lifetime** section for more details

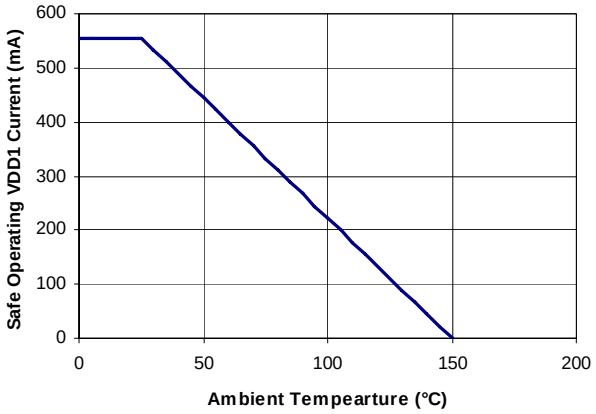

Figure 2 Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

PIN CONFIGURATIONS AND PIN FUNCTION DESCRIPTIONS

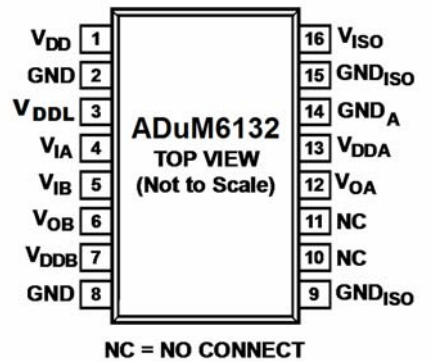

Figure 3. ADuM6132 Pin Configuration

Table 8. ADuM6132 Pin Function Descriptions

Pin No.	Mnemonic	Function
1	V_{DD}	Input supply voltage for isolated power supply, 4.5V to 5.5V
2	GND	Ground reference for isolated power supply input and logic inputs
3	V_{DDL}	Input supply voltage for logic, 4.5V to 5.5V
4	V_{IA}	Logic input A
5	V_{IB}	Logic input B
6	V_{OB}	Output B (non-isolated).
7	V_{DDB}	Output B supply voltage input (non-isolated), 12.5V to 17V
8	GND	Ground reference for isolated power supply input and logic inputs
9	GND_{ISO}	Ground reference for isolated power supply output
10	NC	No Connect
11	NC	No Connect
12	V_{OA}	Output A (isolated)
13	V_{DDA}	Output A supply voltage input, must be connected externally to V_{ISO} (pin16)
14	GND_A	Output A ground reference, must be connected externally to GND_{ISO} (pin 15)
15	GND_{ISO}	Ground reference for isolated power supply output
16	V_{ISO}	Isolated power supply voltage output

Table 9. ADuM6132 Truth Table (Positive Logic)

V_{IA} Input	V_{IB} Input	V_{DDL} State	V_{DDB} State	V_{OA} Output	V_{OB} Output	Notes
L	L	Powered	Powered	L	L	
L	H	Powered	Powered	L	H	
H	L	Powered	Powered	H	L	
H	H	Powered	Powered	H	H	
X	X	Unpowered	Powered	L	L	V_{OA} returns to input state within 1 µs of V_{DD} power restoration.
X	X	Powered	Unpowered	L	L	

APPLICATION INFORMATION

TYPICAL APPLICATION USAGE

The architecture of the ADuM6132 is ideal for motor drive and inverter applications where the low side channels are common to the controller. This arrangement requires only two isolation regions in a package. All of the isolated signals and Isolated power are grouped on one side of the package so full package creepage and clearance are maintained. The low side drive as well as the control signals share a common reference and are also grouped together.

In order to maximize the efficacy of external bypass capacitors, the isoPower DC/DC converter is not internally tied to the data channels, and should be treated as a completely independent subsystem, except for a UVLO function (see Undervoltage lockout). This means that power must be applied to V_{DD} to operate the DC/DC converter. Power must also be applied to V_{DDL} and V_{DDB} to operate the data input and the channel B driver output. On the secondary side, the power generated at the VISO pin must be applied as an input power supply to the V_{DDA} pin. GND_{ISO} and GND_A must be connected together.

The ADuM6132 is intended for driving low gate capacitance transistors (200 pF typically). Most high voltage applications involve larger transistors than this. To accommodate these applications, users can implement a buffer configuration with the ADuM6132 as shown in Figure 3. In many cases, this buffer configuration is the least expensive option to drive high capacitance devices and provides the greatest amount of design flexibility. The precise buffer/high voltage transistor combination can be selected to fit the needs of the application.

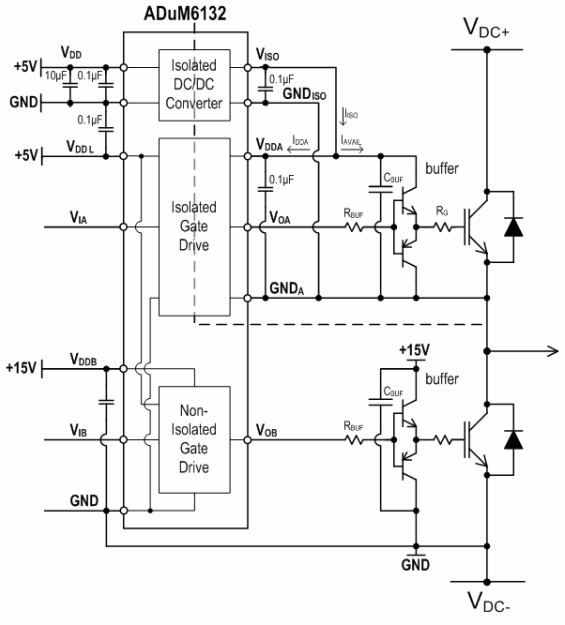

Figure 3. Typical Application Circuit

PC BOARD LAYOUT

The ADuM6132 digital isolator with integrated 250mW *iso*Power DC/DC converter requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (Figure 4). The power supply section of the ADuM6132 uses a very high oscillator frequency to efficiently pass power through its chip scale transformers. In addition, the normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low ESR high frequency capacitor, ripple suppression and proper regulation require a large value capacitor in parallel, see Table 10. The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

Supply	Pins	Bypass Capacitors
V_{DD}	1,2	0.1μF, 10μF
V_{DDB}	7,8	0.1μF
V_{DDL}	2,3	0.1μF
V_{DDA}	13,14	0.1μF
V_{ISO}	15,16	0.1μF, 10μF

Table 10 Recommended Bypass Capacitors

In applications involving high common-mode transients, care should be taken to ensure that board capacitive coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed such that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this could cause voltage differentials between pins exceeding the device's Absolute Maximum Ratings, specified in **Error! Reference source not found.** leading to latch-up and/or permanent damage.

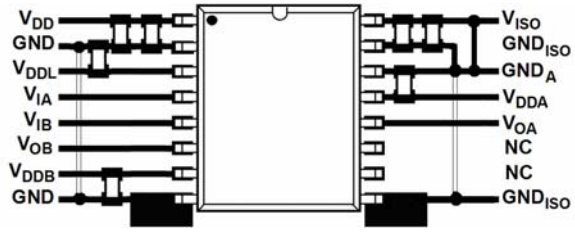

Figure 4. Recommended Printed Circuit Board Layout

The ADuM6132 is a power device that dissipates about 1W of power when fully loaded and running at maximum speed. Since it is not possible to apply a heat sink to an isolation device, the device primarily depends on heat dissipation into the PCB through the GND pins. If the device will be used at high ambient temperatures, care should be taken to provide a thermal path from the GND pins to the PCB ground plane.

The board layout in Figure 4 shows enlarged pads for pins 8 and 9. Multiple vias should be implemented from the pad to the ground plane. This will significantly reduce the temperatures inside of the chip. The dimensions of the expanded pads are left to discretion of the designer and the available board space.

THERMAL ANALYSIS

The ADuM6132 parts consist of several internal die, attached to two lead frame paddles. For the purposes of thermal analysis it is treated as a thermal unit with the highest junction temperature reflected in the θ_{JA} from **Error! Reference source not found.** The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4 layer board with fine width traces and still air. Under normal operating conditions the ADuM6132 will operate at full load across the full temperature range without derating the output current. However, following the recommendations in the PC Board Layout section will decrease the thermal resistance to the PCB allowing increased thermal margin it high ambient temperatures.

UNDERVOLTAGE LOCKOUT

The ADuM6132 has undervoltage lockout (UVLO) circuits on the V_{DDL}, V_{DDA}, and V_{DDB} supplies. For each supply its respective UVLO circuit monitors the supply voltage and takes a predetermined action based on whether the supply voltage is above or below a given threshold. These thresholds are specified in Table 1.

In the recommended configuration of Figure 3 only two independent supplies are controlled by the user: V_{DDB} and V_{DDL}/V_{DD} (V_{DDL}=V_{DD} in Figure 3). V_{DDA} is supplied by the internal DC/DC converter via the V_{ISO}=V_{DDA} external connection. Nevertheless, the V_{DDA} UVLO functionality is included in the below table so that the user has an understanding of the V_{OA} output behavior as the internal DC/DC converter powers on and off.

Table 11. Undervoltage Lockout Functionality Table

User-provided supplies		V_{ISO}-powered supply	
V_{DDL} Supply	V_{DDB} Supply	V_{DDA} Supply	Resultant Effect
H	H	H	Normal operation. Internal DC/DC converter active. V_{OA}/V_{OB} output logic states match V_{IA}/V_{IB} input logic states.
H	H	L	Internal DC/DC converter active but V_{ISO} belpow UVLO threshold. V_{OA} output driven low. V_{OB} output operates normally.
X	L	X	Internal DC/DC converter turned off (V_{ISO} = 0). V_{OA} output driven low. V_{OB} output drive low.
L	X	X	Internal DC/DC converter turned off (V_{ISO} = 0). V_{OA} output driven low. V_{OB} output drive low.

Notes:
L: denotes supply voltage < undervoltage lockout threshold
H: denotes supply voltage > undervoltage lockout threshold
X: denotes supply voltage level is irrelevant

When all three supplies are above their respective UVLO thresholds the ADuM6132 operates normally. The internal DC/DC converter is active and both outputs operate as determined by their respective input logic signals. If either of the user-provided supplies is below its UVLO threshold, the ADuM6132 is put into a disabled mode. In this mode the internal DC/DC converter is turned off and both outputs are driven low. The V_{OB} output is driven low by either the V_{DDL} or V_{DDB} UVLO circuit (whichever is below its threshold). The V_{OA} output is driven low as the internal DC/DC converter is turned off. The V_{ISO} supply voltage is drops to zero. Since V_{DDA} is connected to V_{ISO}, it also is brought down to zero. Once V_{DDA} is below its UVLO threshold V_{OA} is driven low by the V_{DDA} UVLO circuit.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high.

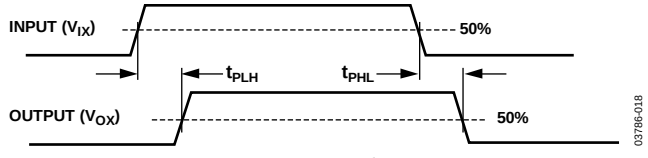

Figure 5. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how

accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM6132 component.

MAGNETIC FIELD IMMUNITY

The ADuM6132 is extremely immune to external magnetic fields. The limitation on the ADuM6132's magnetic field immunity is set by the condition in which induced voltage in the transformer's receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this may occur.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta / dt)\sum \Pi r_n^2; n = 1, 2, ...N$$

where:

β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM6132 and an imposed requirement that the induced voltage is at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 6.

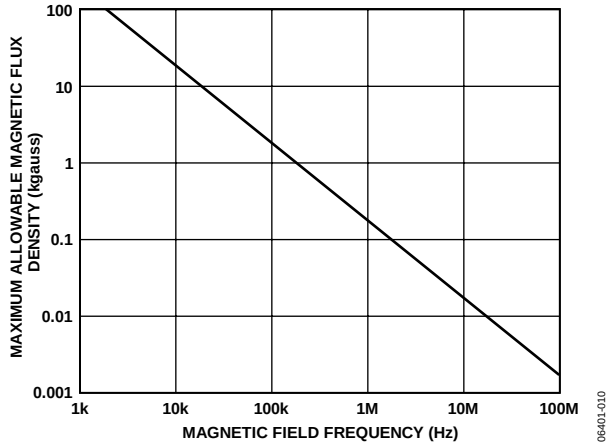

Figure 6. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (with the worst-case polarity), it reduces the received pulse from > 1.0 V to 0.75 V. Note that this is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM6132 transformers. Figure 7 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 7, the ADuM6132 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example, one would have to place a 0.5 kA current 5 mm away from the ADuM6132 to affect the component's operation.

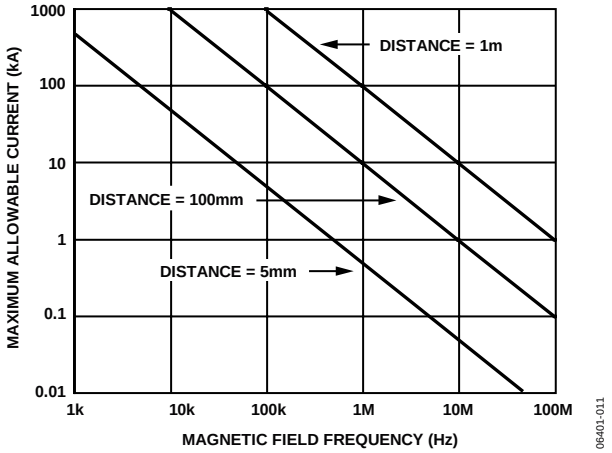

Figure 7. Maximum Allowable Current for Various Current-to-ADuM6132 Spacings

Note that at combinations of strong magnetic fields and high frequencies, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM5230.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. Table 7 summarizes the peak voltages for 50 years of service life for a bipolar ac operating condition and the maximum Analog Devices recommended working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM6132 depends on the

voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 8, Figure 9, and Figure 10 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 7 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage cases. Any cross insulation voltage waveform that does not conform to Figure 9 or Figure 10 should be treated as a bipolar ac waveform and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 7. Note that the voltage presented in Figure 9 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

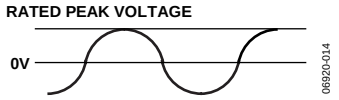

Figure 8. Bipolar AC Waveform

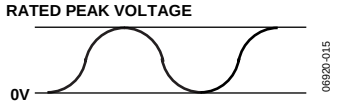

Figure 9. Unipolar AC Waveform

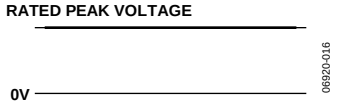

Figure 10. DC Waveform

OUTLINE DIMENSIONS

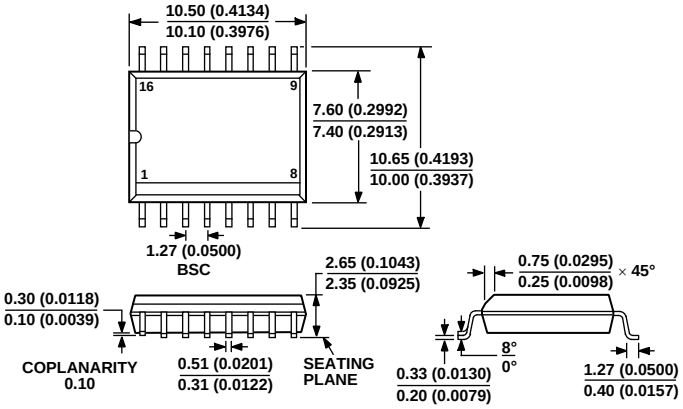

Figure 6. 16-Lead Standard Small Outline Package [SOIC]— Wide Body (RW-16). Dimensions shown in millimeters (inches)

ORDERING GUIDE

Model	No. of Channels	Output Peak Current (A)	Output Voltage (V)	Temperature Range	Package Description	Package Option
ADuM6132ARWZ[1]	2	0.2	15	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM6132ARWZ-RL[1]	2	0.2	15	−40°C to +105°C	16-Lead SOIC_W, 13-inch Tape and Reel Option (1, 000 Units)	RW-16

[1] Z = Pb-free part.

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