Fully Accurate 12-/14-/16-Bit V_{OUT} DAC SPI Interface 2.7 V to 5.5 V in a TSSOP

Preliminary Technical Data

AD5025/45/65

FEATURES

- Low power Dual 12-/14-/16 bit DAC, ± 1LSB INL
- Individual Voltage reference pins
- Rail-to-rail operation
- 2.7 V to 5.5 V power supply
- Power-on reset to zero scale or midscale
- Power down to 400 nA @ 5 V, 200 nA @ 3 V
- 3 power-down functions
- Per channel power-down
- Low glitch upon power up
- Hardware Power Down lock Out Capability
- Hardware $\overline{LDAC}$ with $\overline{LDAC}$ override function
- $\overline{CLR}$ Function to programmable code
- SDO daisy-chaining option
- 14 lead TSSOP

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

GENERAL DESCRIPTION

The AD5025/45/65 are low power, dual 12-/14-/16-bit buffered voltage-out DACs offering relative accuracy specs of 1 LSB INL with individual reference pins and can operate from a single 2.7 V to 5.5 V supply. The AD5025/45/65 64 parts also offer a differential accuracy specification of ±1 LSB. The parts use a versatile 3-wire, low power Schmitt trigger serial interface that operates at clock rates up to 50 MHz and is compatible with standard SPI®, QSPI™, MICROWIRE™, and DSP interface standards. The reference for the AD5025/45 and AD5065 are supplied from an external pin. A reference buffer is also provided on-chip. The AD5025/45/64 incorporates a power-on reset circuit that ensures the DAC output powers up zero scale or midscale and remains there until a valid write takes place to the device. The AD5025/45/65 contain a power-down feature that reduces the current consumption of the device to typically 330 nA at 5 V and provides software selectable output loads while in power-down mode. The parts are put into power-down mode over the serial interface. Total unadjusted error for the parts is <2 mV.

Both parts exhibit very low glitch on power-up. The outputs of all DACs can be updated simultaneously using the $\overline{LDAC}$ function, with the added functionality of user-selectable DAC channels to simultaneously update. There is also an asynchronous $\overline{CLR}$ that clears all DACs to a software-selectable code—0 V, midscale, or full scale. The Part also features a power down lockout pin $\overline{PDL}$, which can be used to prevent the DAC from entering power down under any circumstances over the serial interface.

Functional Block Diagrams

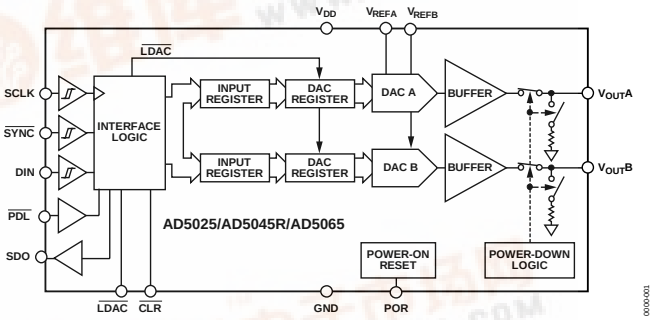

Figure 1.AD5025/45/65

Table 1. Related Devices

Part No.	Description
AD5666	Quad,16-bit buffered D/A,16 LSB INL, TSSOP
AD5066	Quad,16-bit unbuffered D/A,1 LSB INL, TSSOP
AD5064/44/24	Quad 16-bit *nano*DAC, 1 LSB INL, TSSOP
AD5063/62	16-bit *nano*DAC, 1 LSB INL, MSOP
AD5061	16-/14bit *nano*DAC, 4 LSB INL, SOT-23
AD5060/40	16-/14bit *nano*DAC, 1 LSB INL, SOT-23

PRODUCT HIGHLIGHTS

1. Dual channel available in 14-lead TSSOP package with individual Voltage reference pins.
2. 12-/14-/-16 bit accurate, 1 LSB INL.
3. Low glitch on power-up.
4. High speed serial interface with clock speeds up to 50 MHz.
5. Three power-down modes available to the user.
6. Reset to known output voltage (zero scale or midscale).
7. Power Down lockout capability.

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REVISION HISTORY

SPECIFICATIONS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, 2.2V $\leq V_{REFIN} \leq$. V_{DD} unless otherwise specified. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

	B Grade[1]				
Parameter	**Min**	**Typ**	**Max**	**Unit**	**Conditions/Comments**
STATIC PERFORMANCE[2]					
Resolution	16			Bits	AD5065
	14				AD5045
	12				AD5025
Relative Accuracy		0.5	±1	LSB	AD5065 T_A = -40°C to +105°C
		0.5	±1.5		AD5065 T_A = -40°C to +125°C
		0.5	±1	LSB	AD5045 T_A = -40°C to +105°C
		0.5	±1.5		AD5045 T_A = -40°C to +125°C
		0.5	±1	LSB	AD5025 T_A = -40°C to +105°C
		0.5	±1.5		AD5025 T_A = -40°C to +125°C
Differential Nonlinearity			±1	LSB	AD5065/45/25: Guaranteed monotonic by design
Total Unadjusted Error Tue		0.2	±2	mV	AD5065/45/25 T_A = -40°C to +105°C
		0.2	±2	mV	AD5065/45/25 T_A = -40°C to +125°C
Offset Error		1	9	mV	All 0s loaded to DAC register
Offset Error Drift		±2		µV/°C	
Full-Scale Error		−0.2	−1	% FSR	All 1s loaded to DAC register
Gain Error			±1	% FSR	
Gain Temperature Coefficient		±2.5		ppm	Of FSR/°C
DC Power Supply Rejection Ratio		−80		dB	V_{DD} ± 10%
DC Crosstalk		0.5		LSB	Due to single-channel full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		0.5		LSB/mA	Due to load current change
		0.5		LSB	Due to powering down (per channel)
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{DD}	V	
Capacitive Load Stability		1		pF	R_L = 2 kΩ, R_L = 100 kΩ and R_L = ∞
DC Output Impedance (Normal mode)		0.5		Ω	
DC Output Impedance					DAC in Power Down mode
(output connected to 100kΩ network)		100		kΩ	Output impedance tolerance ± 20Ω
(output connected to 1kΩ network)		1		kΩ	Output impedance tolerance ± 400Ω
Short-Circuit Current		60		mA	DAC = full scale, o/p shorted to Gnd
		45		mA	DAC = zero scale, o/p shorted to V_{DD}
Power-Up Time		4.5		µs	Coming out of power-down mode V_{DD} = 5 V
DC PSRR		-92		dB	V_{DD}±10%, DAC = full scale
Wideband SFDR		-67		dB	Output frequency = 10Khz
REFERENCE INPUTS					
Reference Input Range	2.2		V_{DD}	V	
Reference Current		30	50	µA	Per DAC channel V_{REF} = V_{DD} = 5.5 V
Reference Input Impedance		120		KΩ	Per DAC channel
LOGIC INPUTS[3]					
Input Current[4]			±3	µA	All digital inputs

Parameter	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
Input Low Voltage, V_{INL}			0.8	V	V_{DD} = 5 V
Input High Voltage, V_{INH}	2			V	V_{DD} = 5 V
Pin Capacitance		4		pF	
LOGIC OUTPUTS (SDO)[3]					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 2 mA
Output High Voltage, V_{OH}	V_{DD} – 1				I_{SOURCE} = 2 mA
High Impedance Leakage Current			±0.25	µA	
High Impedance Output Capacitance		2		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	All digital inputs at 0 or V_{DD}
					DAC active, excludes load current
I_{DD} (Normal Mode)[5]					$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		3.2	4	mA	
I_{DD} (All Power-Down Modes)[6]					
V_{DD} = 4.5 V to 5.5 V		0.4	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] [1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of 512 to 65,024. Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Total current flowing into all pins.
[5]. Interface inactive. All DACs active. DAC outputs unloaded
[6]. All four DACs powered down

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} =4.096V unless otherwise specified . All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time		5		µs	¼ to ¾ scale settling to ±1 LSB,R_L = 5kΩ single channel update including DAC calibration sequence
Output Voltage Settling Time		14		µs	¼ to ¾ scale settling to ±1 LSB,R_L = 5kΩ all channel update including DAC calibration sequence
Slew Rate		1.5		V/µs	
Digital-to-Analog Glitch Impulse		4		nV-s	1 LSB change around major carry
Reference Feedthrough		−90		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 Hz to 20 MHz
SDO Feedthrough		3		nV-s	Daisy-chain mode; SDO load is 10 pF
Digital Feedthrough		0.1		nV-s	
Digital Crosstalk		0.5		nV-s	
Analog Crosstalk		6		nV-s	
DAC-to-DAC Crosstalk		6.5		nV-s	
AC Crosstalk		6		nV-s	
AC PSRR		TBD			
Multiplying Bandwidth		340		kHz	V_{REF} = 2 V ± 0.2 V p-p
Total Harmonic Distortion		−80		dB	V_{REF} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		64		nV/√Hz	DAC code = 0x8400, 1 kHz
		60		nV/√Hz	DAC code = 0x8400, 10 kHz
Output Noise		6		µV p-p	0.1 Hz to 10 Hz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to + 105°C, typical at 25°C.

TIMING CHARACTERISTICS

All input signals are specified with tr = tf = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 3 and Figure 5. V_{DD} = 2.7 V to 5.5 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 4.

Parameter	Limit at T_{MIN}, T_{MAX} V_{DD} = 2.7 V to 5.5 V	Unit	Conditions/Comments
t_1[1]	20	ns min	SCLK cycle time
t_2	10	ns min	SCLK high time
t_3	10	ns min	SCLK low time
t_4	16.5	ns min	$\overline{SYNC}$ to SCLK falling edge set-up time
t_5	5	ns min	Data set-up time
t_6	5	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_8	1.9	us min	Minimum $\overline{SYNC}$ high time (single channel update)
t_8	10.5	us min	Minimum $\overline{SYNC}$ high time (all channel update)
t_9	16.5	ns min	$\overline{SYNC}$ rising edge to SCLK fall ignore
t_{10}	0	ns min	SCLK falling edge to $\overline{SYNC}$ fall ignore
t_{11}	20	ns min	$\overline{LDAC}$ pulse width low
t_{12}	20	ns min	SCLK falling edge to $\overline{LDAC}$ rising edge
t_{13}	10	ns min	$\overline{CLR}$ pulse width low
t_{14}	10	ns min	SCLK falling edge to $\overline{LDAC}$ falling edge
t_{15}	10.6	us min	$\overline{CLR}$ pulse activation time
t_{16}[2, 3]	22	ns max	SCLK rising edge to SDO valid
t_{17}[3]	5	ns min	SCLK falling edge to $\overline{SYNC}$ rising edge
t_{18}[3]	8	ns min	$\overline{SYNC}$ rising edge to SCLK rising edge
t_{19}[3]	0	ns min	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge
t_{20}	20	ns min	$\overline{PDL}$ pulse width activation time

[1] Maximum SCLK frequency is 50 MHz at V_{DD} = 2.7 V to 5.5 V. Guaranteed by design and characterization; not production tested.
[2] Measured with the load circuit of Figure 16. t_{16} determines the maximum SCLK frequency in daisy-chain mode.
[3] Daisy-chain mode only.

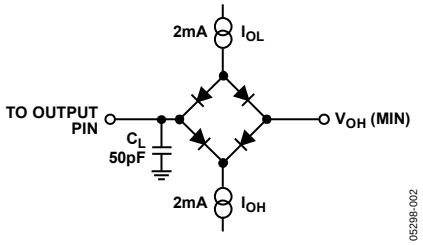

Figure 2. Load Circuit for Digital Output (SDO) Timing Specifications

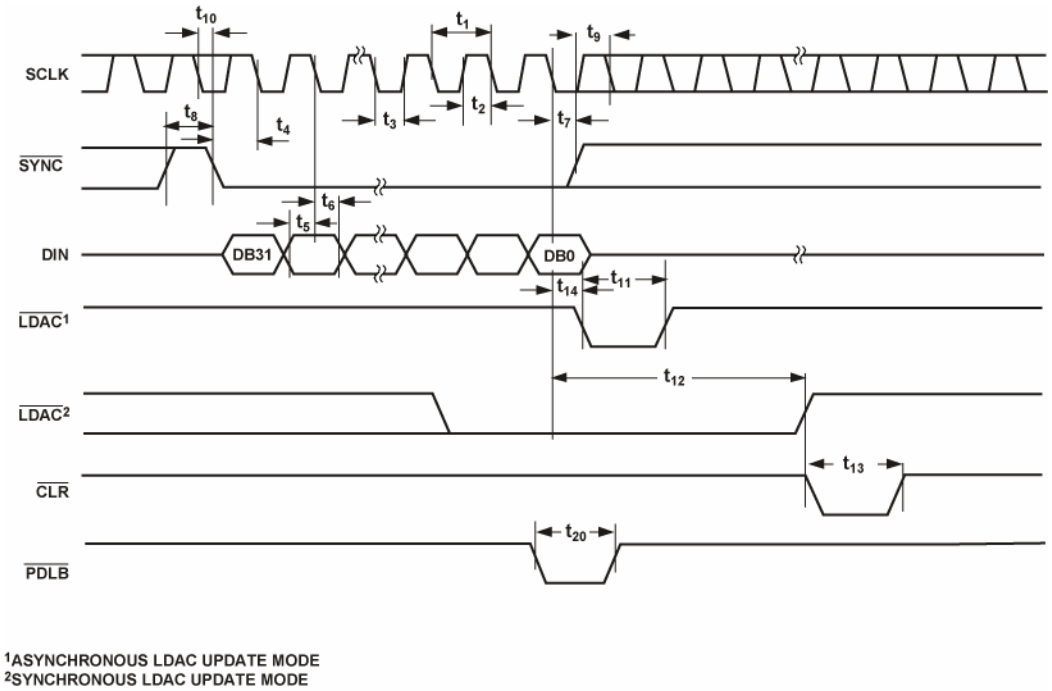

Figure 3. Serial Write Operation

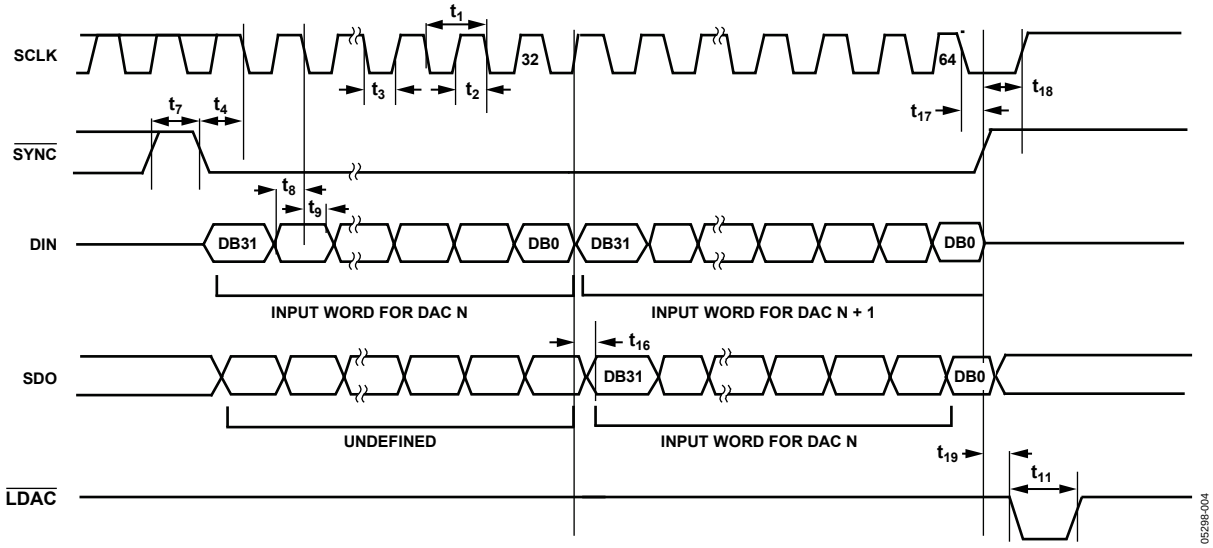

Figure 4. Daisy-Chain Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	+150°C
TSSOP Package	
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
θ_{JA} Thermal Impedance	150.4°C/W
Reflow Soldering Peak Temperature	
SnPb	240°C
Pb Free	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

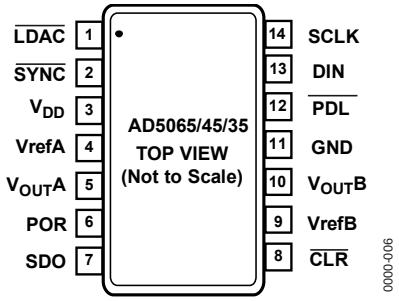

Figure 5. 14-Lead TSSOP (RU-14)

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
2	$\overline{\text{SYNC}}$	Active Low Control Input. This is the frame synchronization signal for the input data. When $\overline{\text{SYNC}}$ goes low, it powers on the SCLK and DIN buffers and enables the input shift register. Data is transferred in on the falling edges of the next 32 clocks. If $\overline{\text{SYNC}}$ is taken high before the 32nd falling edge, the rising edge of $\overline{\text{SYNC}}$ acts as an interrupt and the write sequence is ignored by the device.
3	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
4	V_{REFA}	Dac A reference input .This is the reference voltage input pin for Dac A.
5	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
6	POR	Power-on Reset Pin. Tying this pin to GND powers up the part to 0 V. Tying this pin to V_{DD} powers up the part to midscale.
7	SDO	Serial Data Output. Can be used for daisy-chaining a number of these devices together or for reading back the data in the shift register for diagnostic purposes. The serial data is transferred on the rising edge of SCLK and is valid on the falling edge of the clock.
8	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero, midscale, or full scale. Default setting clears the output to 0 V.
9	V_{REFB}	Dac B reference input .This is the reference voltage input pin for Dac B.
10	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
11	GND	Ground Reference Point for All Circuitry on the Part.
12	$\overline{\text{PDL}}$	The $\overline{\text{PDL}}$ pin is used to ensure hardware shutdown lockout of the device under any circumstance. A Logic 1 at the $\overline{\text{PLO}}$ pin will cause the device to behave as normal. The user may successfully enter software power down over the serial interface while logic 1 is applied to the $\overline{\text{PDL}}$ pin. If a logic 0 is applied to this pin, it will ensure that the device cannot enter software power down under any circumstances. If the device had previously been placed in software power down mode, a high to low transition at the $\overline{\text{PDL}}$ pin will cause the DAC(s) to exit power down and the output the last code in the dac register before the device entered software power down.
13	DIN	Serial Data Input. This device has a 32-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
14	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates of up to 50 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

TBD

Figure 6. INL

TBD

Figure 7. DNL

TBD

Figure 8. TUE

TBD

Figure 9. INL vs. Reference Input Voltag

TBD

Figure 10. DNL vs. Reference Input Voltage

TBD

Figure 11. TUE vs. Reference Input Voltage

TBD

Figure 12. Gain Error and Full-Scale Error vs. Temperature

TBD

Figure 13. Offset Error vs. Temperature

TBD

Figure 14. Gain Error and Full-Scale Error vs. Supply Voltage

TBD

Figure 15. Zero-Scale Error and Offset Error vs. Supply Voltage

TBD

Figure 16. I_{DD} Histogram V_{DD} = 3.0 V

TBD

Figure 17. I_{DD} Histogram V_{DD} = 5.0 V

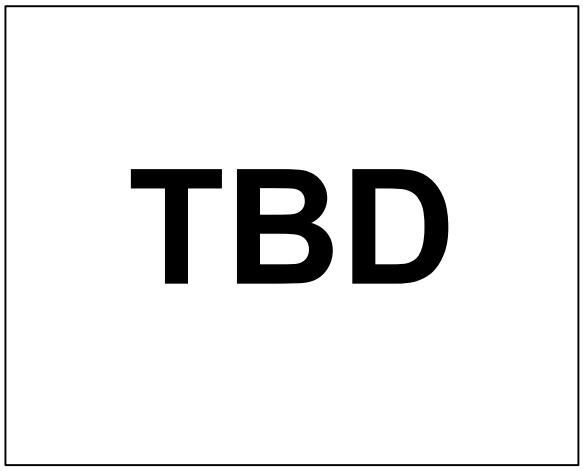

Figure 18. Headroom at Rails vs. Source and Sink

TBD

Figure 19. Source and Sink Current Capability with V_{DD} = 3 V

TBD

Figure 20. Source and Sink Current Capability with V_{DD} = 5 V

TBD

Figure 21. Supply Current vs. Code

TBD

Figure 22. Supply Current vs. Temperature

TBD

Figure 23. Supply Current vs. Supply Voltage

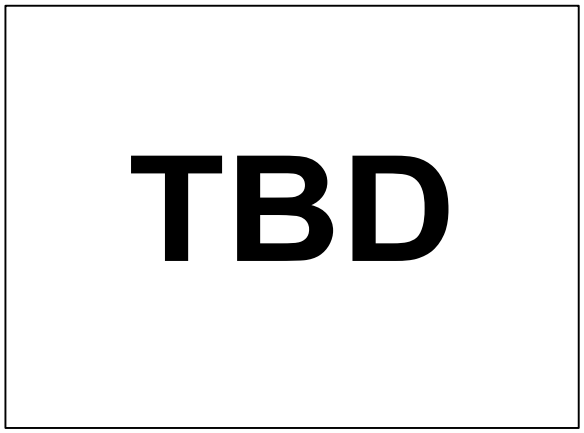

Figure 24. Supply Current vs. Logic Input Voltage

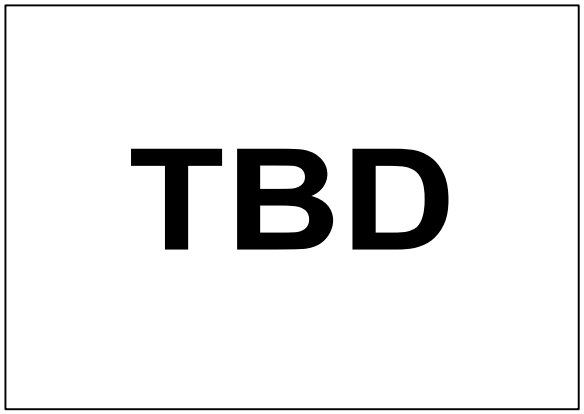

Figure 25. Full-Scale Settling Time

TBD

Figure 26. Power-On Reset to 0 V

TBD

Figure 27. Power-On Reset to Midscale

TBD

Figure 28. Exiting Power-Down to Midscale

TBD

Figure 29. Digital-to-Analog Glitch Impulse (See Figure 34)

TBD

Figure 30. Analog Crosstalk

TBD

Figure 31. DAC-to-DAC Crosstalk

TBD

Figure 32. 0.1 Hz to 10 Hz Output Noise Plot

TBD

Figure 33. Typical Supply Current vs. Frequency @ 5.5 V[1]

TBD

Figure 34. Digital-to-Analog Glitch Energy

TBD

Figure 35. Noise Spectral Density, Internal Reference

TBD

Figure 36. Total Harmonic Distortion

TBD

Figure 37. Settling Time vs. Capacitive Load

TBD

Figure 38. Hardware $\overline{CLR}$

TBD

Figure 39. Multiplying Bandwidth

TBD

Figure 40.Typical output slew rate

THEORY OF OPERATION

D/A SECTION

The AD5025/45/65 are single 12-/14 and 16-bit, serial input, voltage output DACs. The parts operate from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5025/45/65 in a 32-bit word format via a 3-wire serial interface. The AD5025/45 and AD5065 incorporate a power-on reset circuit that ensures the DAC output powers up to a known out-put state (midscale or zero-scale, see the Ordering Guide). The devices also have a software power-down mode that reduces the typical current consumption to less than 1 µa.

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

The ideal output voltage when using and internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:
D = decimal equivalent of the binary code that is loaded to the DAC register. 0 to 65,535 for AD5065 (16 bits).*N* = the DAC resolution.

DAC ARCHITECTURE

The DAC architecture of the AD5065 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 41. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either GND or V_{REF} buffer output. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

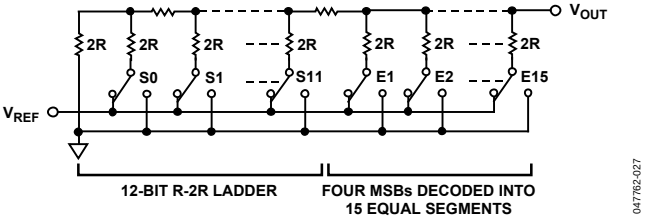

Figure 42. Dac Ladder Structure

REFERENCE BUFFER

The AD5025/45 and AD5065 operate with an external reference. Each of the two onboard dac's will have a dedicated voltage reference pin. In either case the reference input pin has an input range of 2 V to V_{DD}. This input voltage is then used to provide a buffered reference for the DAC core.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The amplifier is capable of driving a load of 2 kΩ in parallel with 1,000 pF to GND. The source and sink capabilities of the output amplifier can be seen in (TBD) and (TBD). The slew rate is 1.5 V/µs with a ¼ to ¾ scale settling time of 10 µs.

SERIAL INTERFACE

The AD5025/45/65 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN) that is compatible with SPI, QSPI, and MICROWIRE interface standards as well as most DSPs. See Figure 3 for a timing diagram of a typical write sequence.

STANDALONE MODE

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 32-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 50 MHz, making the AD5025/45/65 compatible with high speed DSPs. On the 32nd falling clock edge, the last data bit is clocked in and the programmed function is executed, that is, a change in DAC register contents and/or a change in the mode of operation. At this stage, the $\overline{SYNC}$ line can be kept low or be brought high. In either case, it must be brought high for a minimum of 15 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Because the $\overline{SYNC}$ buffer draws more current when V_{IN} = 2 V than it does when V_{IN} = 0.8 V, $\overline{SYNC}$ should be idled low between write sequences for even lower power operation of the part. As is mentioned previously, however, $\overline{SYNC}$ must be brought high again just before the next write sequence.

Table 7. Command Definitions

Command				
C3	C2	C1	C0	Description
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n, update all (software $\overline{LDAC}$)
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{LDAC}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up DCEN register (Daisy chain enable)
1	0	0	1	Set up DIO direction and Value
1	1	1	1	Reserved

Table 8. Address Commands

Address (n)				Selected DAC Channel
A3	**A2**	**A1**	**A0**	
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	Reserved
0	0	1	1	Reserved
1	1	1	1	All DACs

INPUT SHIFT REGISTER

The AD5025/45/65 input shift register is 32 bits wide (see Figure 43). The first four bits are don't cares. The next four bits are the command bits, C3 to C0 (see Table 8), followed by the 4-bit DAC address bits, A3 to A0 (see Table 9) and finally the bit data-word. The data-word comprises either 12-/14 or 16-bit input code followed by 8-/6 or 4 don't care bits for the AD5025/45/65 (see Figure 43). These data bits are transferred to the DAC register on the 32nd falling edge of SCLK.

$\overline{\text{SYNC}}$ INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 32 falling edges of SCLK, and the DAC is updated on the 32nd falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 32nd falling edge, this acts as an interrupt to the write sequence. The shift register is reset, and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs (see Figure 46).

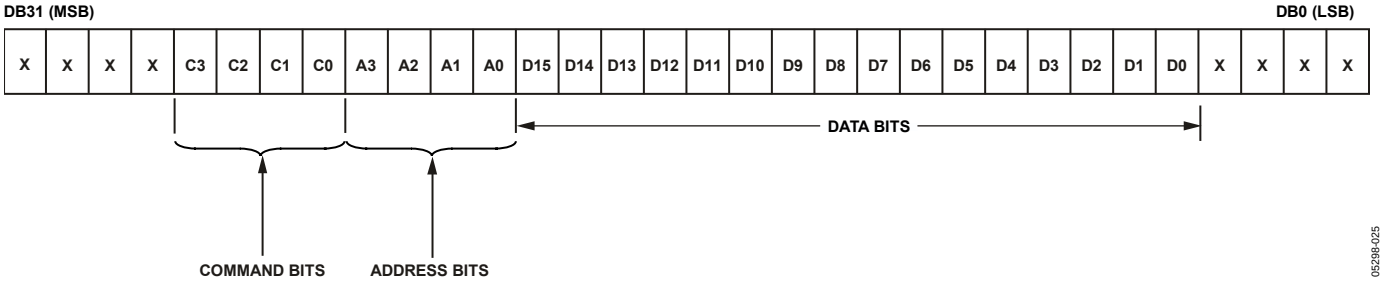

Figure 43. AD5065 Input Register Content

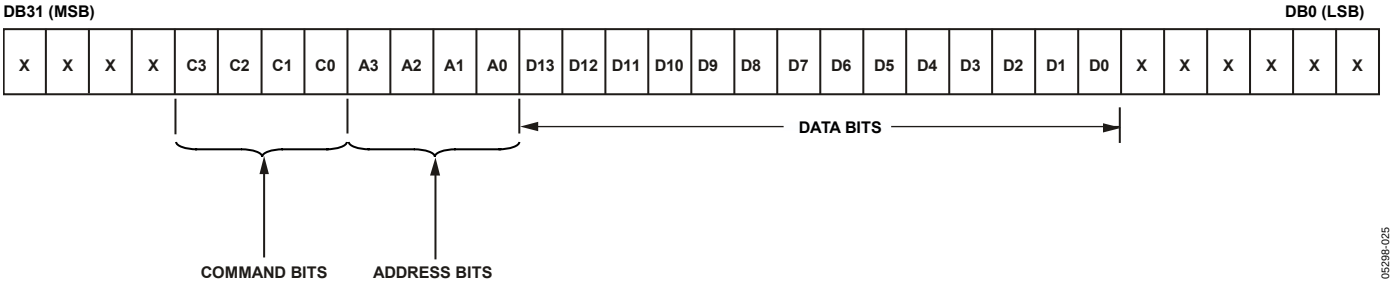

Figure 44. AD5045 Input Register Content

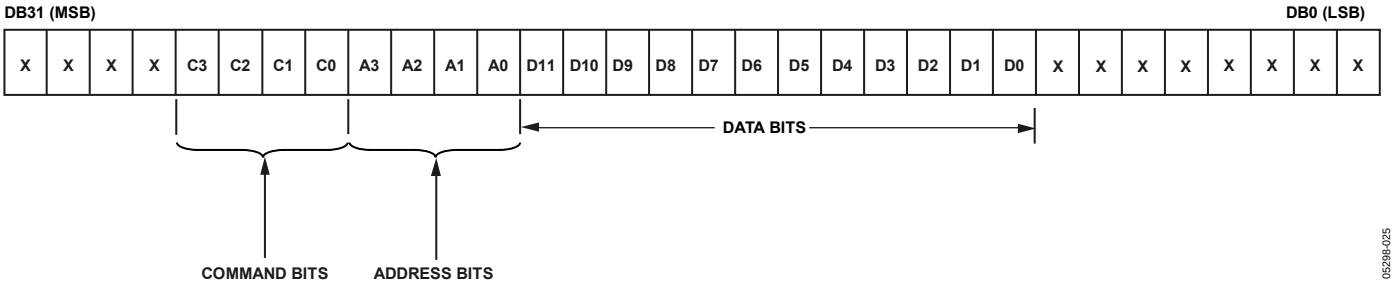

Figure 45. AD5025 Input Register Content

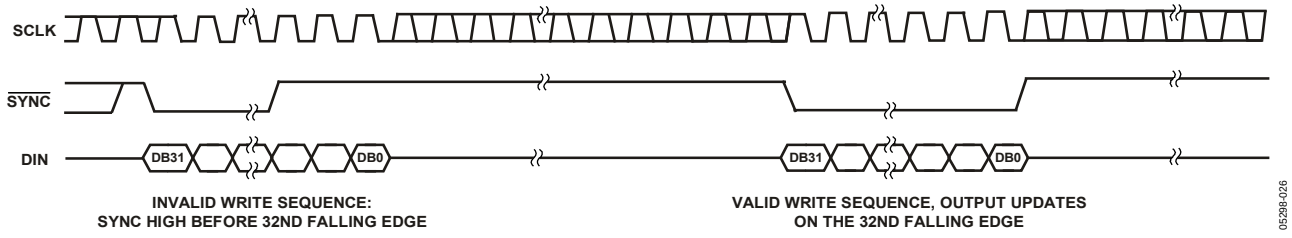

Figure 46. $\overline{\text{SYNC}}$ Interrupt Facility

DAISY-CHAINING

For systems that contain several DACs, or where the user wishes to read back the DAC contents for diagnostic purposes, the SDO pin can be used to daisy-chain several devices together and provide serial read-back.

The daisy-chain mode is enabled through a software executable DCEN (Daisy Chain Enable) command. Command 1000 is reserved for this DCEN function (see Table 7). The daisy-chain mode is enabled by setting a bit (DB1) in the DCEN register. The default setting is standalone mode, where Bit DCEN = 0. Table 9 shows how the state of the bits corresponds to the mode of operation of the device.

The SCLK is continuously applied to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 32 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting this line to the DIN input on the next DAC in the chain, a multi-DAC interface is constructed. Each DAC in the system requires 32 clock pulses; therefore, the total number of clock cycles must equal 32N, where N is the total number of devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ is taken high. This prevents any further data from being clocked into the input shift register.

If $\overline{\text{SYNC}}$ is taken high before 32 clocks are clocked into the part, it is considered an invalid frame and the data is discarded.

The serial clock can be continuous or a gated clock. A continuous SCLK source can be used only if the $\overline{\text{SYNC}}$ can be held low for the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and $\overline{\text{SYNC}}$ must be taken high after the final clock to latch the data.

POWER DOWN LOCKOUT

The AD5025/45/65 contains a 1-bit digital input pin $\overline{\text{PDL}}$. When activated, the power down lock out pin ($\overline{\text{PDL}}$) disables software shutdown under any circumstances The user should hardwire the $\overline{\text{PDL}}$ pin to a logic low (thus preventing subsequent software power down) or logic high (the part can be placed in power down mode over the serial interface). Should the user decide to transition the $\overline{\text{PDL}}$ pin from logic high to a logic low during a valid write sequence, the device will respond immediately and the current write sequence will be aborted. Points to note about the $\overline{\text{PDL}}$ feature is that

1. if a $\overline{\text{PDL}}$ is generated (i.e. a high to low transition) while a valid write sequence is ongoing then the write will be aborted. The user will need to re write the current write command again.
2. If a $\overline{\text{PDL}}$ is generated, whilst the DAC(s) are in power down mode, then the DAC (s) will come out of power down (i.e. all power down registers get reset to 0000) to the last valid stored DAC value. As long, as $\overline{\text{PDL}}$ remains active software power down is disabled.
3. After the $\overline{\text{PDL}}$ is taken from a low to a high state, then all DAC channels will remain in normal mode and the user will have to re-issue a software power down command to the control register in order to power down the required channels..
4. Transitioning the $\overline{\text{PDL}}$ from a low to a high will disable the feature immediately.
5. if $\overline{\text{PLO}}$ and $\overline{\text{CLR}}$ are generated at the same time, then $\overline{\text{CLR}}$ signal will cause the dac register to change as per the Clear Content Register and then DACs will come out of Power Down.
6. if$\overline{\text{PLO}}$, $\overline{\text{CLR}}$ and $\overline{\text{LDAC}}$ are generated at same time then $\overline{\text{CLR}}$ will have higher precedence over $\overline{\text{LDAC}}$ and $\overline{\text{PLO}}$ this case will be same as case 2 mentioned above.
7. The user is recommended to hardwire the pin to a logic high or low thereby either enabling or disabling the feature.

POWER-ON RESET

The AD5025/45/65 contains a power-on reset circuit that controls the output voltage during power-up. By connecting the POR pin low, the AD5025/45/65 output powers up to 0 V; by connecting the POR pin high, the AD5025/45/65 output powers up to mid-scale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is reserved for this reset function (see Table 7). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

POWER-DOWN MODES

The AD5025/45/65 contains four separate modes of operation. Command 0100 is reserved for the power-down function (see Table 7). These modes are software-programmable by setting two bits, Bit DB9 and Bit DB8, in the control register (refer to Table 12). Table 11 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC A and DAC B) can be powered down to the selected mode by setting the corresponding four bits (DB3, DB2, DB1, DB0) to 1. See Table 12 for the contents of the input shift register during power-down/power-up operation.

When both Bit DB9 and Bit DB8, in the control register are set to 0, the part works normally with its normal power consumption of TBD at 5 V. However, for the three power-down modes, the supply current falls to TBD at 5 V (TBD at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 47.

The bias generator, output amplifier, resistor string, and other associated linear circuitry are shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V and V_{DD} = 3 V (see Figure 28).

Any combination of DACs can be powered up by setting PD1 and PD0 to 0 (normal operation). The output powers up to the value in the input register ($\overline{\text{LDAC}}$ Low) or to the value in the DAC register before powering down ($\overline{\text{LDAC}}$ high).

Table 9. DCEN (Daisy-Chain Enable) Register

(DB1)	(DB0)	Action
0	0	Standalone mode (default)
1	0	DCEN mode

Table 10. 32-Bit Input Shift Register Contents for Daisy-Chain Enable and Reference Set-Up Function

MSB											LSB
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB2 to DB19**	**DB1**	**DB0**
X	1	0	0	0	X	X	X	X	X	1/0	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	DCEN register	

Table 11. Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

Table 12. 32-Bit Input Shift Register Contents for Power-Up/Power-Down Function

MSB																LSB
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB10 to DB19**	**DB9**	**DB8**	**DB4 to DB7**	**DB3**	**DB2**	**DB1**	**DB0**
X	0	1	0	0	X	X	X	X	X	PD1	PD0	X	X	X	DAC B	DAC A
Don't cares	Command bits (C2 to C0)				Address bits (A3 to A0)— don't cares				Don't cares	Power-down mode		Don't cares	Power-down/power-up channel selection— set bit to 1 to select			

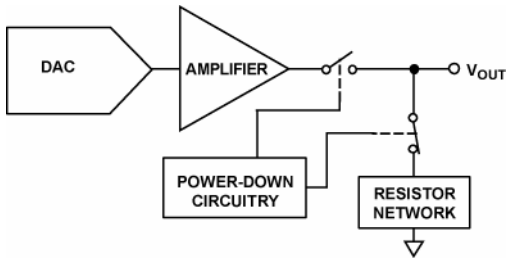

Figure 47. Output Stage During Power-Down

CLEAR CODE REGISTER

The AD5025/45/65 has a hardware $\overline{CLR}$ pin that is an asynchronous clear input. The $\overline{CLR}$ input is falling edge sensitive. Bringing the $\overline{CLR}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{CLR}$ register and sets the analog outputs accordingly. (see **Table 13**) This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting two bits, Bit DB1 and Bit DB0, in the control register (see **Table 13**). The default setting clears the outputs to 0 V. Command 0101 is reserved for loading the clear code register (see Table 7).

The part exits clear code mode on the 32nd falling edge of the next write to the part. If $\overline{CLR}$ is activated during a write sequence, the write is aborted.

The $\overline{CLR}$ pulse activation time—the falling edge of $\overline{CLR}$ to when the output starts to change—is typically TBD ns. However, if outside the DAC linear region, it typically takes TBD ns after executing $\overline{CLR}$ for the output to start changing (see Figure 38).

See Table 14 for contents of the input shift register during the loading clear code register operation

$\overline{LDAC}$ FUNCTION

The outputs of all DACs can be updated simultaneously using the hardware $\overline{LDAC}$ pin.

Synchronous $\overline{LDAC}$: After new data is read, the DAC registers are updated on the falling edge of the 32nd SCLK pulse. $\overline{LDAC}$ can be permanently low or pulsed as in Figure 3

Asynchronous $\overline{LDAC}$: The outputs are not updated at the same time that the input registers are written to. When $\overline{LDAC}$ goes low, the DAC registers are updated with the contents of the input register.

Alternatively, the outputs of all DACs can be updated simultaneously using the software $\overline{LDAC}$ function by writing to Input Register n and updating all DAC registers. Command 0010 is reserved for this software $\overline{LDAC}$ function.

An $\overline{LDAC}$ register gives the user extra flexibility and control over the hardware $\overline{LDAC}$ pin. This register allows the user to select which combination of channels to simultaneously update when the hardware $\overline{LDAC}$ pin is executed. Setting the $\overline{LDAC}$ bit register to 0 for a DAC channel means that this channel's update is controlled by the $\overline{LDAC}$ pin. If this bit is set to 1, this channel updates synchronously; that is, the DAC register is updated after new data is read, regardless of the state of the $\overline{LDAC}$ pin. It effectively sees the $\overline{LDAC}$ pin as being tied low. (See Table 15 for the $\overline{LDAC}$ register mode of operation.) This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating.

Writing to the DAC using command 0110 loads the 4-bit $\overline{LDAC}$ register (DB3 to DB0). The default for each channel is 0; that is, the $\overline{LDAC}$ pin works normally. Setting the bits to 1 means the DAC channel is updated regardless of the state of the $\overline{LDAC}$ pin. See Table 16 for the contents of the input shift register during the load $\overline{LDAC}$ register mode of operation.

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5666 should have separate analog and digital sections. If the AD5666 is in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5025/45/65.

The power supply to the AD5025/45/65 should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should physically be as close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

Table 13. Clear Code Register

Clear Code Register		
DB1	**DB0**	
CR1	**CR0**	**Clears to Code**
0	0	0x0000
0	1	0x8000
1	0	0xFFFF
1	1	No operation

Table 14. 32-Bit Input Shift Register Contents for Clear Code Function

MSB											**LSB**
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB2 to DB19**	**DB1**	**DB0**
X	0	1	0	1	X	X	X	X	X	1/0	1/0
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)				Don't cares	Clear code register (CR1 to CR0)	

Table 15. $\overline{\text{LDAC}}$ Overwrite Definition

Load DAC Register		
$\overline{\text{LDAC}}$ Bits (DB3 to DB0)	**$\overline{\text{LDAC}}$ Pin**	**$\overline{\text{LDAC}}$ Operation**
0	1/0	Determined by $\overline{\text{LDAC}}$ pin
1	X—don't care	DAC channels update, overrides the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 0.

Table 16. 32-Bit Input Shift Register Contents for $\overline{\text{LDAC}}$ Overwrite Function

MSB													**LSB**
DB31 to DB28	**DB27**	**DB26**	**DB25**	**DB24**	**DB23**	**DB22**	**DB21**	**DB20**	**DB4 to DB19**	**DB3**	**DB2**	**DB1**	**DB0**
X	0	1	1	0	X	X	X	X	X	X	X	DAC B	DAC A
Don't cares	Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Setting $\overline{\text{LDAC}}$ bit to 1 override $\overline{\text{LDAC}}$ pin			

MICROPROCESSOR INTERFACING

AD5025/45/65 to Blackfin® ADSP-BF53X Interface

Figure 48 shows a serial interface between the AD5025/45/65 and the Blackfin ADSP-BF53X microprocessor. The ADSP-BF53X processor family incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5025/45/65, the setup for the interface is as follows: DT0PRI drives the DIN pin of the AD5025/45/65, while TSCLK0 drives the SCLK of the parts. The SYNC is driven from TFS0.

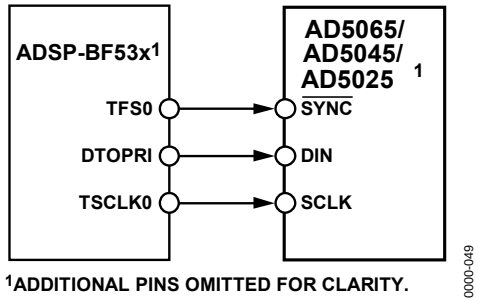

Figure 48. AD5025/45/65 to Blackfin ADSP-BF53X Interface

AD5025/45/65 to 68HC11/68L11 Interface

Figure 49 shows a serial interface between the AD5025/45/65 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK of the AD5025/45/65, and the MOSI output drives the serial data line of the DAC.

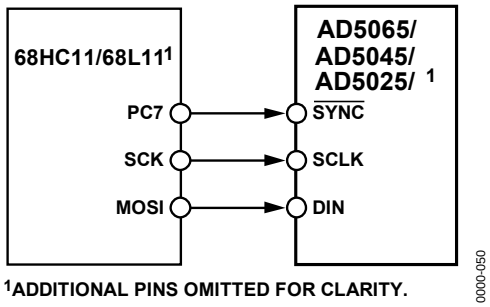

Figure 49. AD5025/45/65 to 68HC11/68L11 Interface

The SYNC signal is derived from a port line (PC7). The setup conditions for correct operation of this interface are as follows: The 68HC11/68L11 is configured with its CPOL bit as 0, and its CPHA bit as 1. When data is being transmitted to the DAC, the SYNC line is taken low (PC7). When the 68HC11/ 68L11 is configured as described previously, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5025/45/65, PC7 is left low after the first eight bits are transferred, and a second serial write operation is performed to the DAC. PC7 is taken high at the end of this procedure.

AD5024/44/64 to 80C51/80L51 Interface

Figure 50 shows a serial interface between the AD5024/44/64 and the 80C51/80L51 microcontroller. The setup for the interface is as follows: TxD of the 80C51/ 80L51 drives SCLK of the AD5025/45/65, and RxD drives the serial data line of the part. The SYNC signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is to be transmitted to the AD5025/45/65, P3.3 is taken low. The 80C51/80L51 transmit data in 8-bit bytes only; thus, only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 output the serial data in a format that has the LSB first. The AD5025/45/65 must receive data with the MSB first. The 80C51/80L51 transmit routine should take this into account.

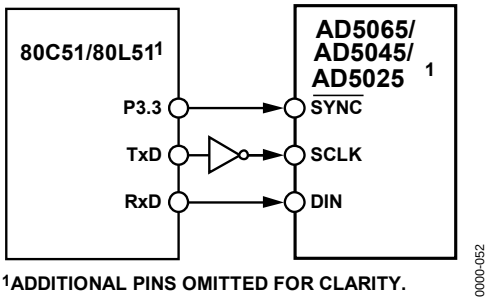

Figure 50. AD5025/45/65 to 80C512/80L51 Interface

AD5025/45/65 to MICROWIRE Interface

Figure 51 shows an interface between the AD5025/45/65 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5025/45/65 on the rising edge of the SCLK.

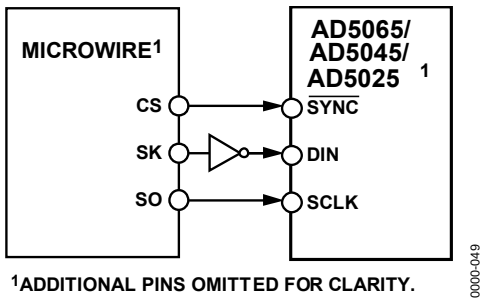

Figure 51. AD5025/45/654 to MICROWIRE Interface

APPLICATIONS

USING A REFERENCE AS A POWER SUPPLY FOR THE AD5025/45/65

Because the supply current required by the AD5025/45/65 is extremely low, an alternative option is to use a voltage reference to supply the required voltage to the parts (see Figure 52). This is especially useful if the power supply is quite noisy or if the system supply voltages are at some value other than 5 V or 3 V, for example, 15 V. The voltage reference outputs a steady supply voltage for the AD5025, AD5045 and AD5065. If the low dropout REF195 is used, it must supply 500 µA of current to the AD5025/ AD5045 / AD5065, with no load on the output of the DAC. When the DAC output is loaded, the REF195 also needs to supply the current to the load. The total current required (with a 5 kΩ load on the DAC output) is

500 µA + (5 V/5 kΩ) = 1.5 mA

The load regulation of the REF195 is typically 2 ppm/mA, which results in a 3 ppm (15 µV) error for the 1.5 mA current drawn from it. This corresponds to a 0.196 LSB error.

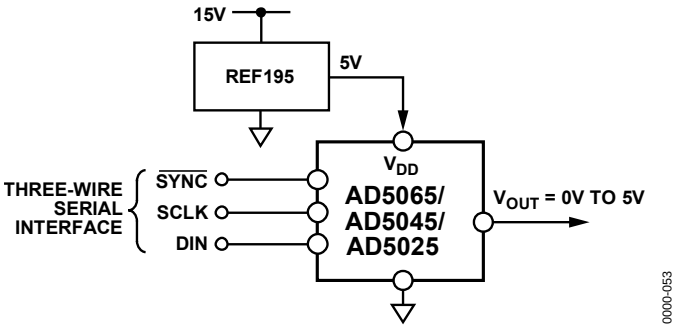

Figure 52. REF195 as Power Supply to the AD5025/45/65

BIPOLAR OPERATION USING THE AD5025/45/65

The AD5025/45/65 has been designed for single-supply operation, but a bipolar output range is also possible using the circuit in Figure 53. The circuit gives an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820 or an OP295 as the output amplifier.

The output voltage for any input code can be calculated as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65{,}536} \right) \times \left(\frac{R1 + R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65,535). With V_{DD} = 5 V, $R1 = R2$ = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65{,}536} \right) - 5 \text{ V}$$

This is an output voltage range of ±5 V, with 0x0000 corresponding to a −5 V output, and 0xFFFF corresponding to a +5 V output.

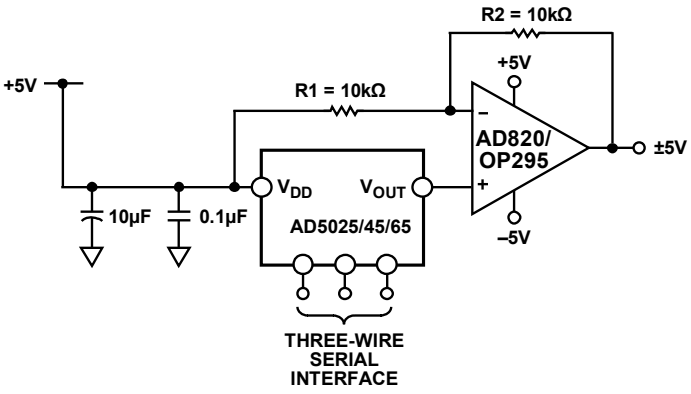

Figure 53. Bipolar Operation with the AD5025/45/65

USING THE AD5025/45/65 WITH A GALVANICALLY ISOLATED INTERFACE

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that can occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. The AD5025/45/65 uses a 3-wire serial logic interface, so the ADuM1300 three-channel digital isolator provides the required isolation (see Figure 54). The power supply to the part also needs to be isolated, which is done by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5025/45/65.

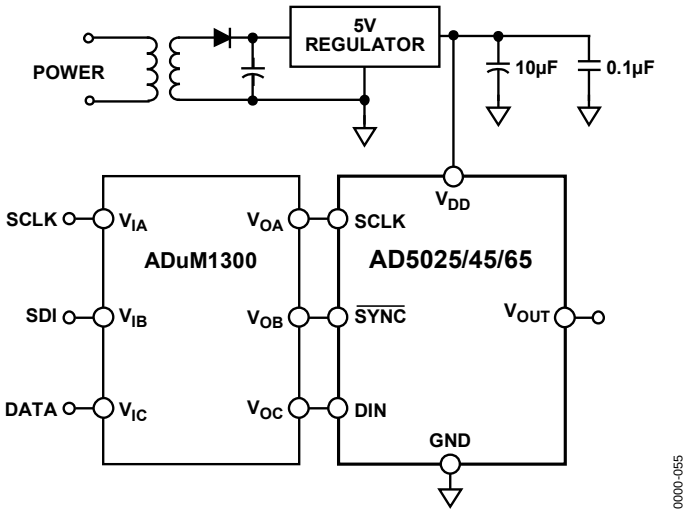

Figure 54. AD5025/45/65 with a Galvanically Isolated Interface

OUTLINE DIMENSIONS

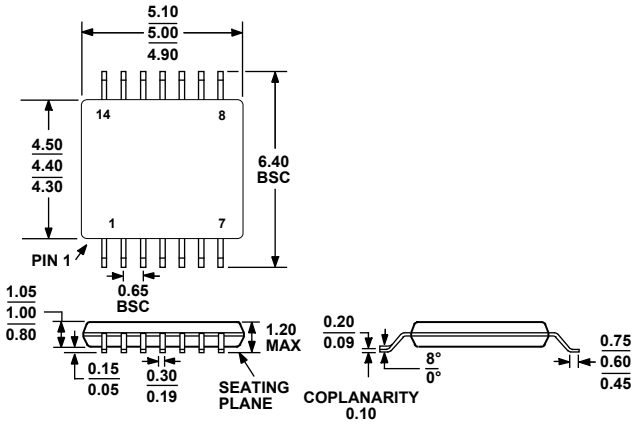

Figure 55. 14-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-14)
Dimensions shown in millimeters

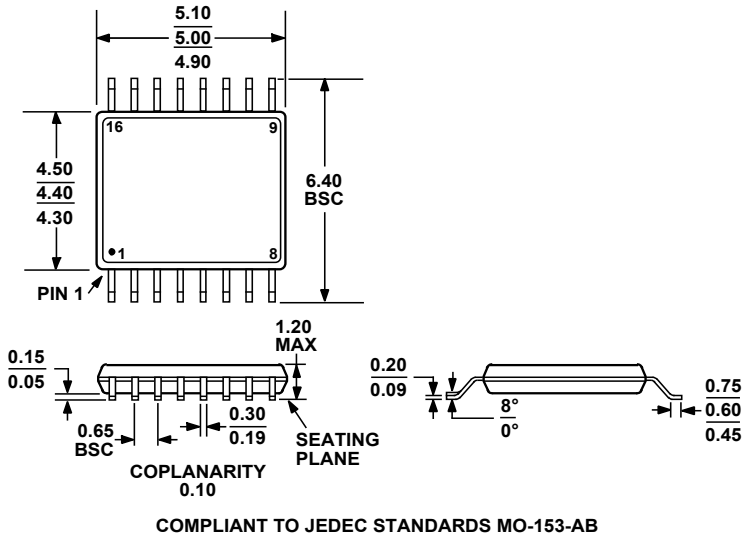

Figure 56. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Power-On Reset to Code	Accuracy	Resolution
AD5065BRUZ-1[1]	–40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±1 LSB INL	16 bits
AD5065BRUZ-1REEL7[1]	–40°C to +105°C	14-Lead TSSOP	RU-14	Zero	±1 LSB INL	16 bits
AD5045BRUZ[1]	–40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	14 bits
AD5045BRUZ-REEL7[1]	–40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	14 bits
AD5025BRUZ[1]	–40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	12 bits
AD5025BRUZ-REEL7[1]	–40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	12 bits
Eval-AD5065 EBZ[1]		Evaluation board				
Eval-AD5045 EBZ[1]		Evaluation board				
Eval-AD5025 EBZ[1]		Evaluation board				

[1] Z = Pb-free part.

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