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Internally Trimmed Precision IC Multiplier

AD534

FEATURES

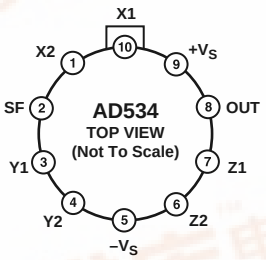
Pretrimmed to ±0.25% max 4-Quadrant Error (AD534L)
All Inputs (X, Y and Z) Differential, High Impedance for $[(X_1 - X_2)(Y_1 - Y_2)/10\ V] + Z_2$ Transfer Function
Scale-Factor Adjustable to Provide up to X100 Gain
Low Noise Design: 90 µV rms, 10 Hz–10 kHz
Low Cost, Monolithic Construction
Excellent Long Term Stability

APPLICATIONS

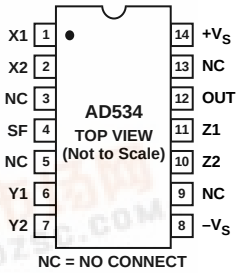
High Quality Analog Signal Processing
Differential Ratio and Percentage Computations
Algebraic and Trigonometric Function Synthesis
Wideband, High-Crest rms-to-dc Conversion
Accurate Voltage Controlled Oscillators and Filters
Available in Chip Form

PIN CONFIGURATIONS

TO-100 (H-10A) Package

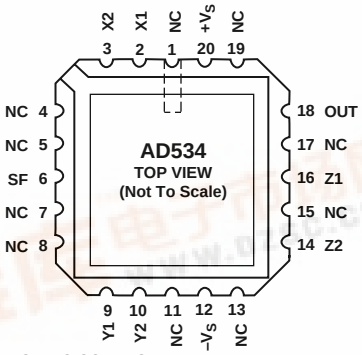


TO-116 (D-14) Package



NC = NO CONNECT

LCC (E-20A) Package



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD534 is a monolithic laser trimmed four-quadrant multiplier divider having accuracy specifications previously found only in expensive hybrid or modular products. A maximum multiplication error of ±0.25% is guaranteed for the AD534L without any external trimming. Excellent supply rejection, low temperature coefficients and long term stability of the on-chip thin film resistors and buried Zener reference preserve accuracy even under adverse conditions of use. It is the first multiplier to offer fully differential, high impedance operation on all inputs, including the Z-input, a feature which greatly increases its flexibility and ease of use. The scale factor is pretrimmed to the standard value of 10.00 V; by means of an external resistor, this can be reduced to values as low as 3 V.

The wide spectrum of applications and the availability of several grades commend this multiplier as the first choice for all new designs. The AD534J (±1% max error), AD534K (±0.5% max) and AD534L (±0.25% max) are specified for operation over the 0°C to +70°C temperature range. The AD534S (±1% max) and AD534T (±0.5% max) are specified over the extended temperature range, –55°C to +125°C. All grades are available in hermetically sealed TO-100 metal cans and TO-116 ceramic DIP packages. AD534J, K, S and T chips are also available.

PROVIDES GAIN WITH LOW NOISE

The AD534 is the first general purpose multiplier capable of providing gains up to X100, frequently eliminating the need for separate instrumentation amplifiers to precondition the inputs. The AD534 can be very effectively employed as a variable gain differential input amplifier with high common-mode rejection. The gain option is available in all modes, and will be found to simplify the implementation of many function-fitting algorithms such as those used to generate sine and tangent. The utility of this feature is enhanced by the inherent low noise of the AD534: 90 µV, rms (depending on the gain), a factor of 10 lower than previous monolithic multipliers. Drift and feedthrough are also substantially reduced over earlier designs.

UNPRECEDENTED FLEXIBILITY

The precise calibration and differential Z-input provide a degree of flexibility found in no other currently available multiplier. Standard MDSSR functions (multiplication, division, squaring, square-rooting) are easily implemented while the restriction to particular input/output polarities imposed by earlier designs has been eliminated. Signals may be summed into the output, with or without gain and with either a positive or negative sense. Many new modes based on implicit-function synthesis have been made possible, usually requiring only external passive components. The output can be in the form of a current, if desired, facilitating such operations as integration.

REV. B

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AD534—SPECIFICATIONS (@ T_A = + 25°C, $\pm V_S$ = 15 V, R ≥ 2 kΩ)

Model	AD534J Min	AD534J Typ	AD534J Max	AD534K Min	AD534K Typ	AD534K Max	AD534L Min	AD534L Typ	AD534L Max	Units
MULTIPLIER PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$		
Total Error[1] (–10 V ≤ X, Y ≤ +10 V)			**±1.0**			**±0.5**			**±0.25**	%
T_A = min to max		±1.5			±1.0			±0.5		%
Total Error vs. Temperature		±0.022			±0.015			±0.008		%/°C
Scale Factor Error (SF = 10.000 V Nominal)[2]		±0.25			±0.1			±0.1		%
Temperature-Coefficient of Scaling Voltage		±0.02			±0.01			±0.005		%/°C
Supply Rejection (±15 V ± 1 V)		±0.01			±0.01			±0.01		%
Nonlinearity, X (X = 20 V p-p, Y = 10 V)		±0.4			±0.2	**±0.3**		±0.10	**±0.12**	%
Nonlinearity, Y (Y = 20 V p-p, X = 10 V)		±0.2			±0.1	**±0.1**		±0.005	**±0.1**	%
Feedthrough[3], X (Y Nulled, X = 20 V p-p 50 Hz)		±0.3			±0.15	**±0.3**		±0.05	**±0.12**	%
Feedthrough[3], Y (X Nulled, Y = 20 V p-p 50 Hz)		±0.01			±0.01	**±0.1**		±0.003	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**		±2	**±10**	mV
Output Offset Voltage Drift		200			100			100		µV/°C
DYNAMICS										
Small Signal BW (V_{OUT} = 0.1 rms)		1			1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000 pF)		50			50			50		kHz
Slew Rate (V_{OUT} 20 p-p)		20			20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20 V)		2			2			2		µs
NOISE										
Noise Spectral-Density SF = 10 V		0.8			0.8			0.8		µV/√Hz
SF = 3 V[4]		0.4			0.4			0.4		µV/√Hz
Wideband Noise f = 10 Hz to 5 MHz		1			1			1		mV/rms
f = 10 Hz to 10 kHz		90			90			90		µV/rms
OUTPUT										
Output Voltage Swing	**±11**			**±11**			**±11**			V
Output Impedance (f ≤ 1 kHz)		0.1			0.1			0.1		Ω
Output Short Circuit Current (R_L = 0, T_A = min to max)		30			30			30		mA
Amplifier Open Loop Gain (f = 50 Hz)		70			70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]										
Signal Voltage Range (Diff. or CM		±10			±10			±10		V
Operating Diff.)		±12			±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			50			50		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**		±2	**±10**	mV
Offset Voltage Drift Z		200			100			100		µV/°C
CMRR	**60**	80		**70**	90		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1			0.05	**0.2**	µA
Differential Resistance		10			10			10		MΩ
DIVIDER PERFORMANCE										
Transfer Function ($X_1 > X_2$)		$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10 V, –10 V ≤ Z ≤ +10 V)		±0.75			±0.35			±0.2		%
(X = 1 V, –1 V ≤ Z ≤ +1 V)		±2.0			±1.0			±0.8		%
(0.1 V ≤ X ≤ 10 V, –10 V ≤ Z ≤ 10 V)		±2.5			±1.0			±0.8		%
SQUARE PERFORMANCE										
Transfer Function		$\frac{(X_1-X_2)^2}{10\,V}+Z_2$			$\frac{(X_1-X_2)^2}{10\,V}+Z_2$			$\frac{(X_1-X_2)^2}{10\,V}+Z_2$		
Total Error (–10 V ≤ X ≤ 10 V)		±0.6			±0.3			±0.2		%
SQUARE-ROOTER PERFORMANCE										
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10\,V(Z_2-Z_1)}+X_2$			$\sqrt{10\,V(Z_2-Z_1)}+X_2$			$\sqrt{10\,V(Z_2-Z_1)}+X_2$		
Total Error[1] (1 V ≤ Z ≤ 10 V)		±1.0			±0.5			±0.25		%
POWER SUPPLY SPECIFICATIONS										
Supply Voltage										
Rated Performance		±15			±15			±15		V
Operating	±8		**±18**	±8		**±18**	±8		**±18**	V
Supply Current										
Quiescent		4	**6**		4	**6**		4	**6**	mA
PACKAGE OPTIONS										
TO-100 (H-10A)		AD534JH			AD534KH			AD534LH		
TO-116 (D-14)		AD534JD			AD534KD			AD534LD		
Chips					AD534K Chips					

NOTES

[1]Figures given are percent of full scale, ±10 V (i.e., 0.01% = 1 mV).

[2]May be reduced down to 3 V using external resistor between $-V_S$ and SF.

[3]Irreducible component due to nonlinearity: excludes effect of offsets.

[4]Using external resistor adjusted to give SF = 3 V.

[5]See Functional Block Diagram for definition of sections.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those tests are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in boldface are tested on all production units.

Model	AD534S Min	AD534S Typ	AD534S Max	AD534T Min	AD534T Typ	AD534T Max	Units
MULTIPLIER PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$			$\frac{(X_1-X_2)(Y_1-Y_2)}{10\,V}+Z_2$		
Total Error[1] (–10 V ≤ X, Y ≤ +10 V)			**±1.0**			**±0.5**	%
T_A = min to max			**±2.0**		±1.0		%
Total Error vs. Temperature			**±0.02**			**±0.01**	%/°C
Scale Factor Error							
(SF = 10.000 V Nominal)[2]		±0.25			±0.1		%
Temperature-Coefficient of							
Scaling Voltage		±0.02				**±0.005**	%/°C
Supply Rejection (±15 V ± 1 V)		±0.01			±0.01		%
Nonlinearity, X (X = 20 V p-p, Y = 10 V)		±0.4			±0.2	**±0.3**	%
Nonlinearity, Y (Y = 20 V p-p, X = 10 V)		±0.2			±0.1	**±0.1**	%
Feedthrough[3], X (Y Nulled,							
X = 20 V p-p 50 Hz)		±0.3			±0.15	**±0.3**	%
Feedthrough[3], Y (X Nulled,							
Y = 20 V p-p 50 Hz)		±0.01			±0.01	**±0.1**	%
Output Offset Voltage		±5	**±30**		±2	**±15**	mV
Output Offset Voltage Drift			**500**			**300**	µV/°C
DYNAMICS							
Small Signal BW (V_{OUT} = 0.1 rms)		1			1		MHz
1% Amplitude Error (C_{LOAD} = 1000 pF)		50			50		kHz
Slew Rate (V_{OUT} 20 p-p)		20			20		V/µs
Settling Time (to 1%, ΔV_{OUT} = 20 V)		2			2		µs
NOISE							
Noise Spectral-Density SF = 10 V		0.8			0.8		µV/√Hz
SF = 3 V[4]		0.4			0.4		µV/√Hz
Wideband Noise f = 10 Hz to 5 MHz		1.0			1.0		mV/rms
f = 10 Hz to 10 kHz		90			90		µV/rms
OUTPUT							
Output Voltage Swing	**±11**			**±11**			V
Output Impedance (f ≤ 1 kHz)		0.1			0.1		Ω
Output Short Circuit Current							
(R_L = 0, T_A = min to max)		30			30		mA
Amplifier Open Loop Gain (f = 50 Hz)		70			70		dB
INPUT AMPLIFIERS (X, Y and Z)[5]							
Signal Voltage Range (Diff. or CM		±10			±10		V
Operating Diff.)		±12			±12		V
Offset Voltage X, Y		±5	**±20**		±2	**±10**	mV
Offset Voltage Drift X, Y		100			150		µV/°C
Offset Voltage Z		±5	**±30**		±2	**±15**	mV
Offset Voltage Drift Z			**500**			**300**	µV/°C
CMRR	**60**	80		**70**	90		dB
Bias Current		0.8	**2.0**		0.8	**2.0**	µA
Offset Current		0.1			0.1		µA
Differential Resistance		10			10		MΩ
DIVIDER PERFORMANCE							
Transfer Function ($X_1 > X_2$)		$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$			$10\,V\frac{(Z_2-Z_1)}{(X_1-X_2)}+Y_1$		
Total Error[1] (X = 10 V, –10 V ≤ Z ≤ +10 V)		±0.75			±0.35		%
(X = 1 V, –1 V ≤ Z ≤ +1 V)		±2.0			±1.0		%
(0.1 V ≤ X ≤ 10 V, –10 V ≤ Z ≤ 10 V)		±2.5			±1.0		%
SQUARE PERFORMANCE							
Transfer Function		$\frac{(X_1-X_2)^2}{10\,V}+Z_2$			$\frac{(X_1-X_2)^2}{10\,V}+Z_2$		
Total Error (–10 V ≤ X ≤ 10 V)		±0.6			±0.3		%
SQUARE-ROOTER PERFORMANCE							
Transfer Function ($Z_1 \le Z_2$)		$\sqrt{10\,V(Z_2-Z_1)}+X_2$			$\sqrt{10\,V(Z_2-Z_1)}+X_2$		
Total Error[1] (1 V ≤ Z ≤ 10 V)		±1.0			±0.5		%
POWER SUPPLY SPECIFICATIONS							
Supply Voltage							
Rated Performance		±15			±15		V
Operating	±8		**±22**	±8		**±22**	V
Supply Current							
Quiescent		4	**6**		4	**6**	mA
PACKAGE OPTIONS							
TO-100 (H-10A)		AD534SH			AD534TH		
TO-116 (D-14)		AD534SD			AD534TD		
E-20A		AD534SE					
Chips		AD534S Chips			AD534T Chips		

NOTES
[1]Figures given are percent of full scale, ±10 V (i.e., 0.01% = 1 mV).
[2]May be reduced down to 3 V using external resistor between $-V_S$ and SF.
[3]Irreducible component due to nonlinearity: excludes effect of offsets.
[4]Using external resistor adjusted to give SF = 3 V.
[5]See Functional Block Diagram for definition of sections.

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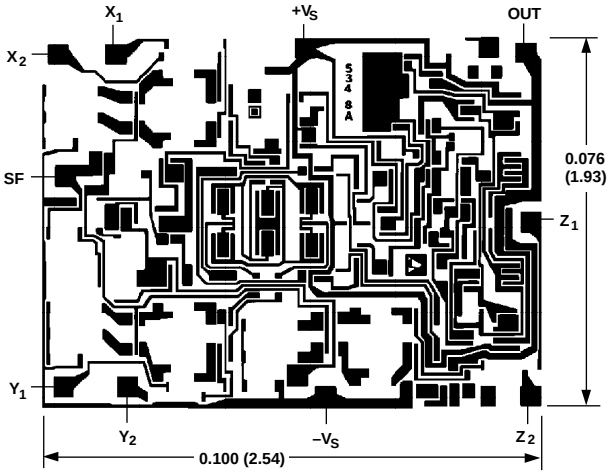
CHIP DIMENSIONS AND BONDING DIAGRAM

Dimensions shown in inches and (mm).
Contact factory for latest dimensions.



THE AD534 IS AVAILABLE IN LASER - TRIMMED CHIP FORM

ABSOLUTE MAXIMUM RATINGS

	AD534J, K, L	AD534S, T
Supply Voltage	±18 V	±22 V
Internal Power Dissipation	500 mW	*
Output Short-Circuit to Ground	Indefinite	*
Input Voltages, X_1 X_2 Y_1 Y_2 Z_1 Z_2	$\pm V_S$	*
Rated Operating Temperature Range	0°C to +70°C	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C	*
Lead Temperature Range, 60 s Soldering	+300°C	*

*Same as AD534J Specs.

Thermal Characteristics

Thermal Resistance θ_{JC} = 25°C/W for H-10A
θ_{JA} = 150°C/W for H-10A
θ_{JC} = 25°C/W for D-14 or E-20A
θ_{JA} = 95°C/W for D-14 or E-20A

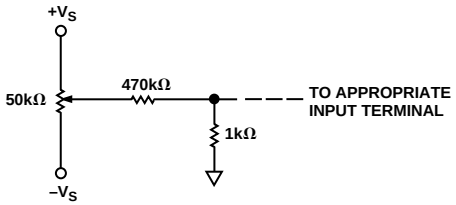


Figure 1. Optional Trimming Configuration

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD534JD	0°C to +70°C	Side Brazed DIP	D-14
AD534KD	0°C to +70°C	Side Brazed DIP	D-14
AD534LD	0°C to +70°C	Side Brazed DIP	D-14
AD534JH	0°C to +70°C	Header	H-10A
AD534JH/+	0°C to +70°C	Header	H-10A
AD534KH	0°C to +70°C	Header	H-10A
AD534KH/+	0°C to +70°C	Header	H-10A
AD534LH	0°C to +70°C	Header	H-10A
AD534K Chip	0°C to +70°C	Chip	
AD534SD	–55°C to +125°C	Side Brazed DIP	D-14
AD534SD/883B	–55°C to +125°C	Side Brazed DIP	D-14
AD534TD	–55°C to +125°C	Side Brazed DIP	D-14
AD534TD/883B	–55°C to +125°C	Side Brazed DIP	D-14
JM38510/13902BCA	–55°C to +125°C	Side Brazed DIP	D-14
JM38510/13901BCA	–55°C to +125°C	Side Brazed DIP	D-14
AD534SE	–55°C to +125°C	LCC	E-20A
AD534SE/883B	–55°C to +125°C	LCC	E-20A
AD534TE/883B	–55°C to +125°C	LCC	E-20A
AD534SH	–55°C to +125°C	Header	H-10A
AD534SH/883B	–55°C to +125°C	Header	H-10A
AD534TH	–55°C to +125°C	Header	H-10A
AD534TH/883B	–55°C to +125°C	Header	H-10A
JM38510/13902BIA	–55°C to +125°C	Header	H-10A
JM38510/13901BIA	–55°C to +125°C	Header	H-10A
AD534S Chip	–55°C to +125°C	Chip	
AD534T Chip	–55°C to +125°C	Chip	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD534 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

FUNCTIONAL DESCRIPTION

Figure 2 is a functional block diagram of the AD534. Inputs are converted to differential currents by three identical voltage-to-current converters, each trimmed for zero offset. The product of the X and Y currents is generated by a multiplier cell using Gilbert's translinear technique. An on-chip "Buried Zener" provides a highly stable reference, which is laser trimmed to provide an overall scale factor of 10 V. The difference between XY/SF and Z is then applied to the high gain output amplifier. This permits various closed loop configurations and dramatically reduces nonlinearities due to the input amplifiers, a dominant source of distortion in earlier designs. The effectiveness of the new scheme can be judged from the fact that under typical conditions as a multiplier the nonlinearity on the Y input, with X at full scale (±10 V), is ±0.005% of FS; even at its worst point, which occurs when X = ±6.4 V, it is typically only ±0.05% of FS Nonlinearity for signals applied to the X input, on the other hand, is determined almost entirely by the multiplier element and is parabolic in form. This error is a major factor in determining the overall accuracy of the unit and hence is closely related to the device grade.

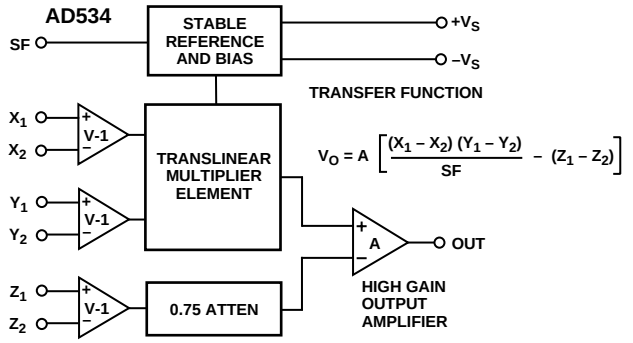


Figure 2. Functional Block Diagram

The generalized transfer function for the AD534 is given by:

$$V_{OUT} = A\left(\frac{(X_1 - X_2)(Y_1 - Y_2)}{SF} - (Z_1 - Z_2)\right)$$

where A = open loop gain of output amplifier, typically 70 dB at dc

X, Y, Z = input voltages (full scale = ±SF, peak = ±1.25 SF)

SF = scale factor, pretrimmed to 10.00 V but adjustable by the user down to 3 V.

In most cases the open loop gain can be regarded as infinite, and SF will be 10 V. The operation performed by the AD534, can then be described in terms of equation:

$$(X_1 - X_2)(Y_1 - Y_2) = 10\,V\,(Z_1 - Z_2)$$

The user may adjust SF for values between 10.00 V and 3 V by connecting an external resistor in series with a potentiometer between SF and $-V_S$. The approximate value of the total resistance for a given value of SF is given by the relationship:

$$R_{SF} = 5.4K\frac{SF}{10 - SF}$$

Due to device tolerances, allowance should be made to vary R_{SF}; by ±25% using the potentiometer. Considerable reduction in bias currents, noise and drift can be achieved by decreasing SF. This has the overall effect of increasing signal gain without the customary increase in noise. Note that the peak input signal is always limited to 1.25 SF (i.e., ±5 V for SF = 4 V) so the overall transfer function will show a maximum gain of 1.25. The performance with small input signals, however, is improved by using a lower SF since the dynamic range of the inputs is now fully utilized. Bandwidth is unaffected by the use of this option.

Supply voltages of ±15 V are generally assumed. However, satisfactory operation is possible down to ±8 V (see Figure 16). Since all inputs maintain a constant peak input capability of ±1.25 SF some feedback attenuation will be necessary to achieve output voltage swings in excess of ±12 V when using higher supply voltages.

OPERATION AS A MULTIPLIER

Figure 3 shows the basic connection for multiplication. Note that the circuit will meet all specifications without trimming.

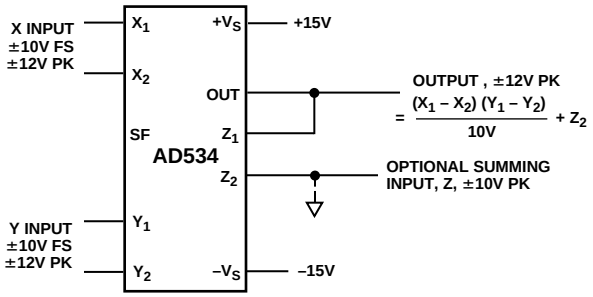


Figure 3. Basic Multiplier Connection

In some cases the user may wish to reduce ac feedthrough to a minimum (as in a suppressed carrier modulator) by applying an external trim voltage (±30 mV range required) to the X or Y input (see Figure 1). Figure 19 shows the typical ac feedthrough with this adjustment mode. Note that the Y input is a factor of 10 lower than the X input and should be used in applications where null suppression is critical.

The high impedance Z_2 terminal of the AD534 may be used to sum an additional signal into the output. In this mode the output amplifier behaves as a voltage follower with a 1 MHz small signal bandwidth and a 20 V/μs slew rate. This terminal should always be referenced to the ground point of the driven system, particularly if this is remote. Likewise, the differential inputs should be referenced to their respective ground potentials to realize the full accuracy of the AD534.

A much lower scaling voltage can be achieved without any reduction of input signal range using a feedback attenuator as shown in Figure 4. In this example, the scale is such that $V_{OUT} = XY$, so that the circuit can exhibit a maximum gain of 10. This connection results in a reduction of bandwidth to about 80 kHz without the peaking capacitor C_F = 200 pF. In addition, the output offset voltage is increased by a factor of 10 making external adjustments necessary in some applications. Adjustment is made by connecting a 4.7 MΩ resistor between Z_1 and the slider of a pot connected across the supplies to provide ±300 mV of trim range at the output.

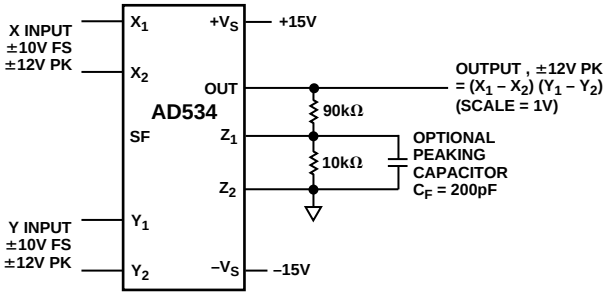


Figure 4. Connections for Scale-Factor of Unity

Feedback attenuation also retains the capability for adding a signal to the output. Signals may be applied to the high impedance Z_2 terminal where they are amplified by +10 or to the common ground connection where they are amplified by +1. Input signals may also be applied to the lower end of the 10 kΩ resistor, giving a gain of –9. Other values of feedback ratio, up to X100, can be used to combine multiplication with gain.

Occasionally it may be desirable to convert the output to a current, into a load of unspecified impedance or dc level. For example, the function of multiplication is sometimes followed by integration; if the output is in the form of a current, a simple capacitor will provide the integration function. Figure 5 shows how this can be achieved. This method can also be applied in squaring, dividing and square rooting modes by appropriate choice of terminals. This technique is used in the voltage-controlled low-pass filter and the differential-input voltage-to-frequency converter shown in the Applications section.

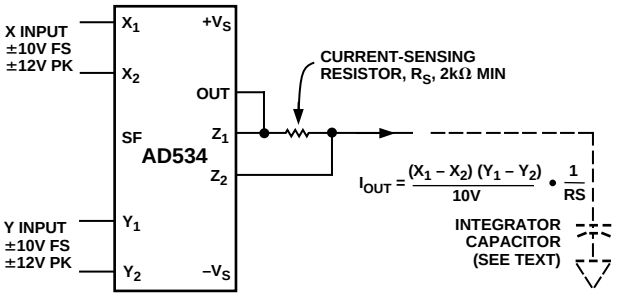


Figure 5. Conversion of Output to Current

OPERATION AS A SQUARER

Operation as a squarer is achieved in the same fashion as the multiplier except that the X and Y inputs are used in parallel. The differential inputs can be used to determine the output polarity (positive for $X_1 = Y_1$ and $X_2 = Y_2$, negative if either one of the inputs is reversed). Accuracy in the squaring mode is typically a factor of 2 better than in the multiplying mode, the largest errors occurring with small values of output for input below 1 V.

If the application depends on accurate operation for inputs that are always less than ±3 V, the use of a reduced value of SF is recommended as described in the Functional Description section (previous page). Alternatively, a feedback attenuator may be used to raise the output level. This is put to use in the difference-of-squares application to compensate for the factor of 2 loss involved in generating the sum term (see Figure 8).

The difference-of-squares function is also used as the basis for a novel rms-to-dc converter shown in Figure 15. The averaging filter is a true integrator, and the loop seeks to zero its input. For this to occur, $(V_{IN})^2 - (V_{OUT})^2 = 0$ (for signals whose period is well below the averaging time-constant). Hence V_{OUT} is forced to equal the rms value of V_{IN}. The absolute accuracy of this technique is very high; at medium frequencies, and for signals near full scale, it is determined almost entirely by the ratio of the resistors in the inverting amplifier. The multiplier scaling voltage affects only open loop gain. The data shown is typical of performance that can be achieved with an AD534K, but even using an AD534J, this technique can readily provide better than 1% accuracy over a wide frequency range, even for crest-factors in excess of 10.

OPERATION AS A DIVIDER

The AD535, a pin-for-pin functional equivalent to the AD534, has guaranteed performance in the divider and square-rooter configurations and is recommended for such applications.

Figure 6 shows the connection required for division. Unlike earlier products, the AD534 provides differential operation on both numerator and denominator, allowing the ratio of two floating variables to be generated. Further flexibility results from access to a high impedance summing input to Y_1. As with all dividers based on the use of a multiplier in a feedback loop, the bandwidth is proportional to the denominator magnitude, as shown in Figure 23.

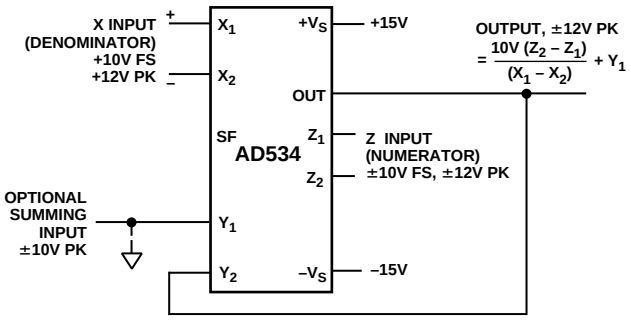


Figure 6. Basic Divider Connection

Without additional trimming, the accuracy of the AD534K and L is sufficient to maintain a 1% error over a 10 V to 1 V denominator range. This range may be extended to 100:1 by simply reducing the X offset with an externally generated trim voltage (range required is ±3.5 mV max) applied to the unused X input (see Figure 1). To trim, apply a ramp of +100 mV to +V at 100 Hz to both X_1 and Z_1 (if X_2 is used for offset adjustment, otherwise reverse the signal polarity) and adjust the trim voltage to minimize the variation in the output.*

Since the output will be near +10 V, it should be ac-coupled for this adjustment. The increase in noise level and reduction in bandwidth preclude operation much beyond a ratio of 100 to 1.

As with the multiplier connection, overall gain can be introduced by inserting a simple attenuator between the output and Y_2 terminal. This option, and the differential-ratio capability of the AD534 are utilized in the percentage-computer application shown in Figure 12. This configuration generates an output proportional to the percentage deviation of one variable (A) with respect to a reference variable (B), with a scale of one volt per percent.

OPERATION AS A SQUARE ROOTER

The operation of the AD534 in the square root mode is shown in Figure 7. The diode prevents a latching condition which could occur if the input momentarily changes polarity. As shown, the output is always positive; it may be changed to a negative output by reversing the diode direction and interchanging the X inputs. Since the signal input is differential, all combinations of input and output polarities can be realized, but operation is restricted to the one quadrant associated with each combination of inputs.

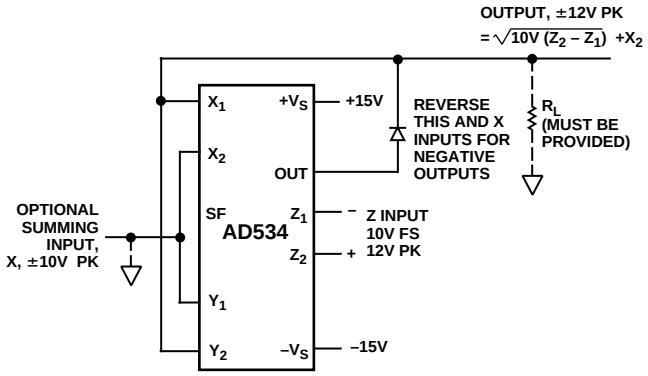


Figure 7. Square-Rooter Connection

In contrast to earlier devices, which were intolerant of capacitive loads in the square root modes, the AD534 is stable with all loads up to at least 1000 pF. For critical applications, a small adjustment to the Z input offset (see Figure 1) will improve accuracy for inputs below 1 V.

*See the AD535 data sheet for more details.

AD534–Applications Section

The versatility of the AD534 allows the creative designer to implement a variety of circuits such as wattmeters, frequency doublers and automatic gain controls to name but a few.

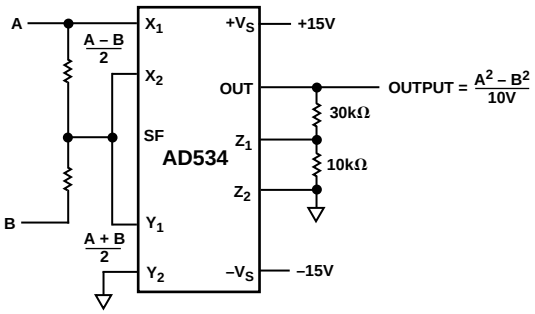
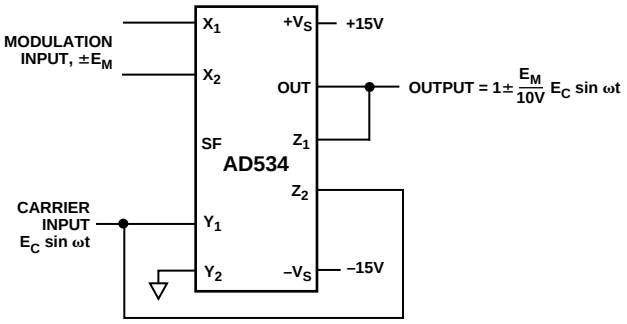
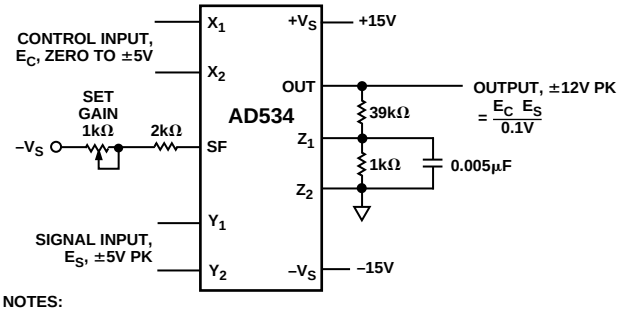


Figure 8. Difference-of-Squares



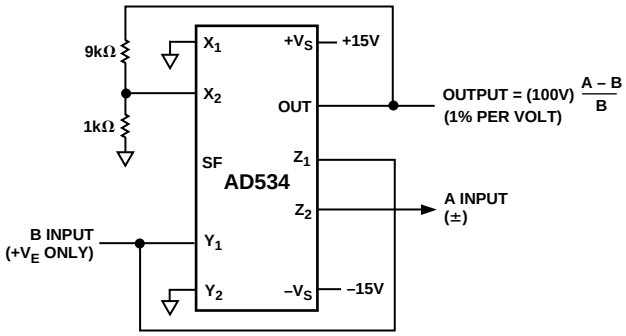
THE SF PIN OR A Z-ATTENUATOR CAN BE USED TO PROVIDE OVERALL SIGNAL AMPLIFICATION, OPERATION FROM A SINGLE SUPPLY POSSIBLE; BIAS Y_2 TO $V_S/2$.

Figure 11. Linear AM Modulator



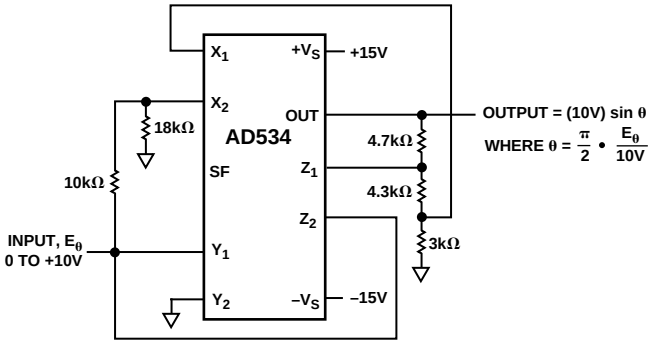
NOTES:
1) GAIN IS X 10 PER-VOLT OF E_C, ZERO TO X 50
2) WIDEBAND (10Hz – 30kHz) OUTPUT NOISE IS 3mV RMS, TYP CORRESPONDING TO A.F.S. S/N RATIO OF 70dB
3) NOISE REFERRED TO SIGNAL INPUT, WITH E_C = ±5V, IS 60µV RMS, TYP
4) BANDWITH IS DC TO 20kHz, –3dB, INDEPENDENT OF GAIN

Figure 9. Voltage-Controlled Amplifier



OTHER SCALES, FROM 10% PER VOLT TO 0.1% PER VOLT CAN BE OBTAINED BY ALTERING THE FEEDBACK RATIO.

Figure 12. Percentage Computer



USING CLOSE TOLERANCE RESISTORS AND AD534L, ACCURACY OF FIT IS WITHIN ±0.5% AT ALL POINTS. θ IS IN RADIANS.

Figure 10. Sine-Function Generator

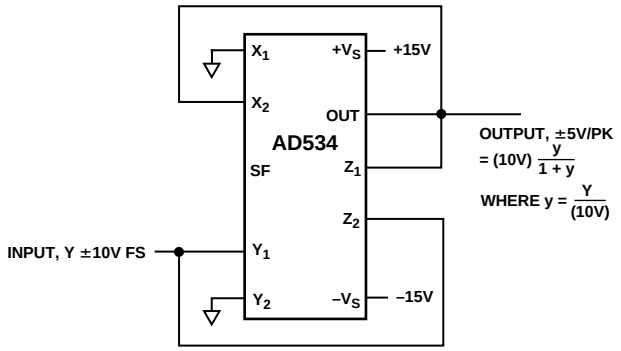
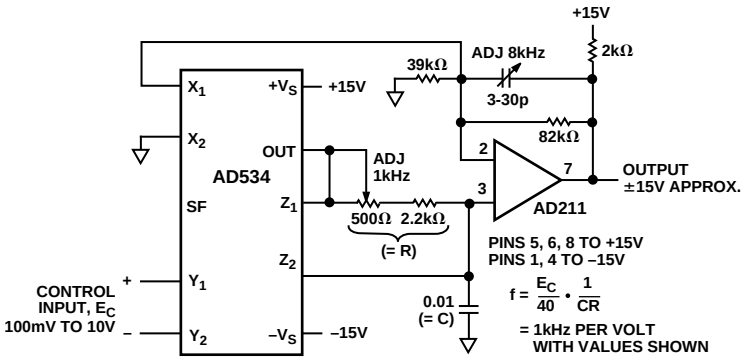


Figure 13. Bridge-Linearization Function



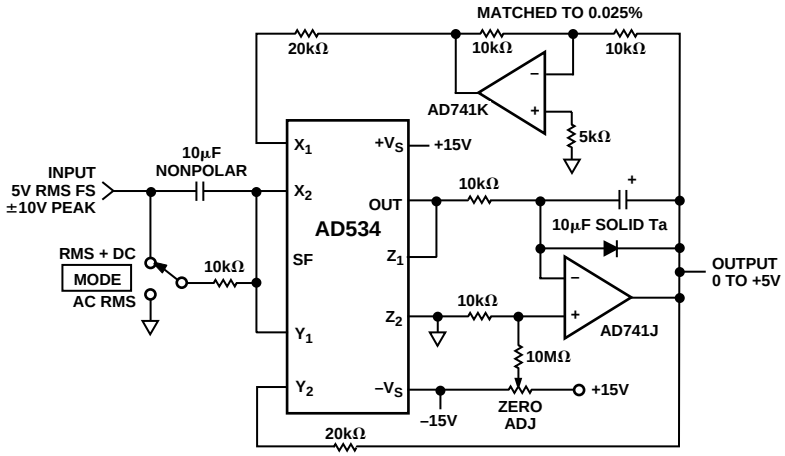
CALIBRATION PROCEDURE:

WITH E_C = 1.0V, ADJUST POT TO SET f = 1.000kHz. WITH E_C = 8.0V ADJUST TRIMMER CAPACITOR TO SET f = 8.000kHz. LINEARITY WILL TYPICALLY BE WITHIN ± 0.1% OF FS FOR ANY OTHER INPUT.

DUE TO DELAYS IN THE COMPARATOR, THIS TECHNIQUE IS NOT SUITABLE FOR MAXIMUM FREQUENCIES ABOVE 10kHz. FOR FREQUENCIES ABOVE 10kHz THE AD537 VOLTAGE-TO-FREQUENCY CONVERTER IS RECOMMENDED.

A TRIANGLE-WAVE OF ±5V PK APPEARS ACROSS THE 0.01μF CAPACITOR; IF USED AS AN OUTPUT, A VOLTAGE-FOLLOWER SHOULD BE INTERPOSED.

Figure 14. Differential-Input Voltage-to-Frequency Converter



CALIBRATION PROCEDURE:

WITH 'MODE' SWITCH IN 'RMS + DC' POSITION, APPLY AN INPUT OF +1.00VDC. ADJUST ZERO UNTIL OUTPUT READS SAME AS INPUT. CHECK FOR INPUTS OF ±10V; OUTPUT SHOULD BE WITHIN ±0.05% (5mV).

ACCURACY IS MAINTAINED FROM 60Hz TO 100kHz, AND IS TYPICALLY HIGH BY 0.5% AT 1MHz FOR V_{IN} = 4V RMS (SINE, SQUARE OR TRIANGULAR-WAVE).

PROVIDED THAT THE PEAK INPUT IS NOT EXCEEDED, CREST-FACTORS UP TO AT LEAST TEN HAVE NO APPRECIABLE EFFECT ON ACCURACY .

INPUT IMPEDANCE IS ABOUT 10kΩ; FOR HIGH (10MΩ) IMPEDANCE, REMOVE MODE SWITCH AND INPUT COUPLING COMPONENTS.

FOR GUARANTEED SPECIFICATIONS THE AD536A AND AD636 ARE OFFERED AS A SINGLE PACKAGE RMS-TO-DC CONVERTER.

Figure 15. Wideband, High-Crest Factor, RMS-to-DC Converter

AD534—Typical Performance Curves (typical at +25°C, with $V_S = \pm 15$ V dc, unless otherwise noted)

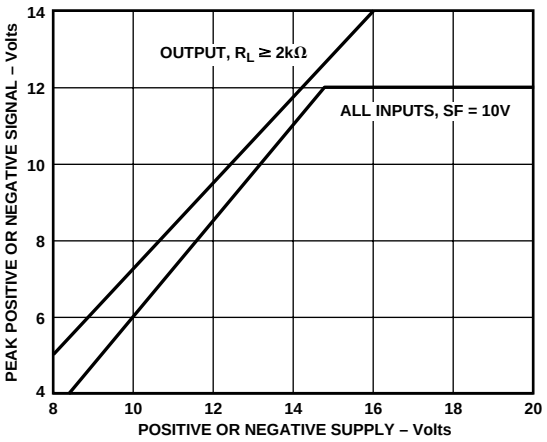


Figure 16. Input/Output Signal Range vs. Supply Voltages

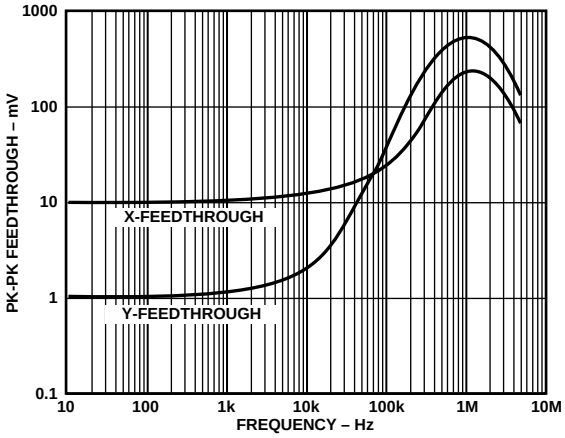


Figure 19. AC Feedthrough vs. Frequency

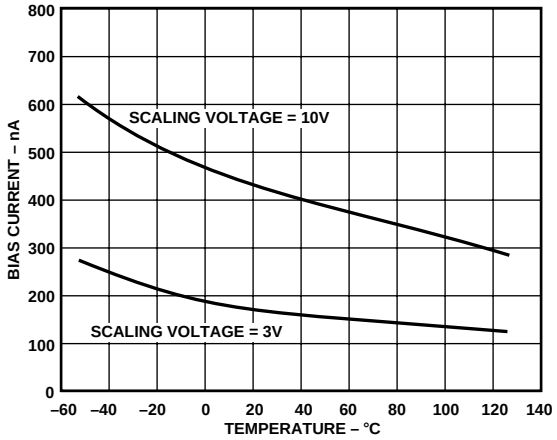


Figure 17. Bias Currents vs. Temperature (X, Y or Z Inputs)

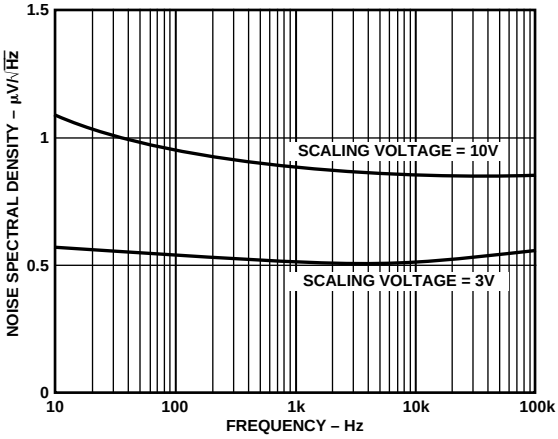


Figure 20. Noise Spectral Density vs. Frequency

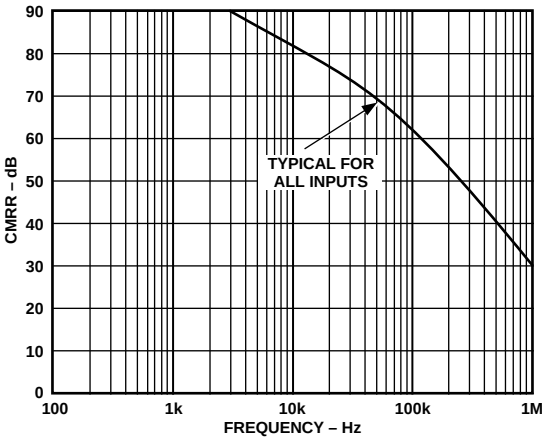


Figure 18. Common-Mode Rejection Ratio vs. Frequency

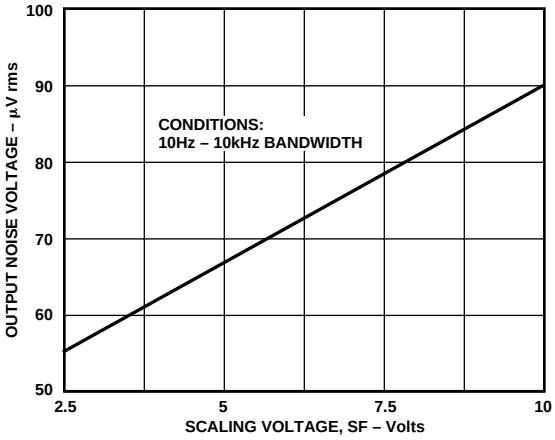


Figure 21. Wideband Noise vs. Scaling Voltage

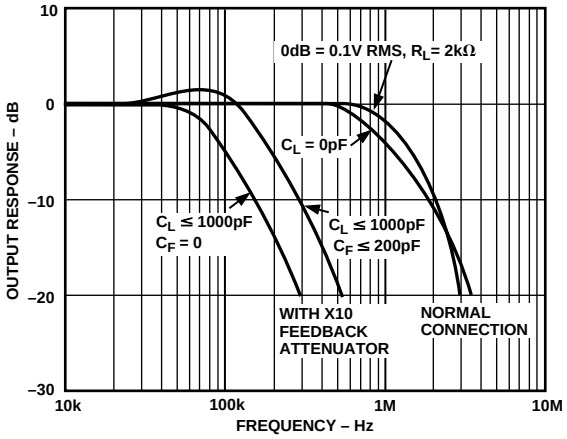


Figure 22. Frequency Response as a Multiplier

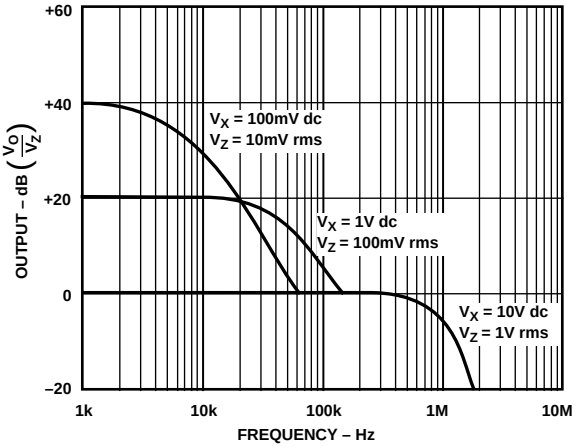
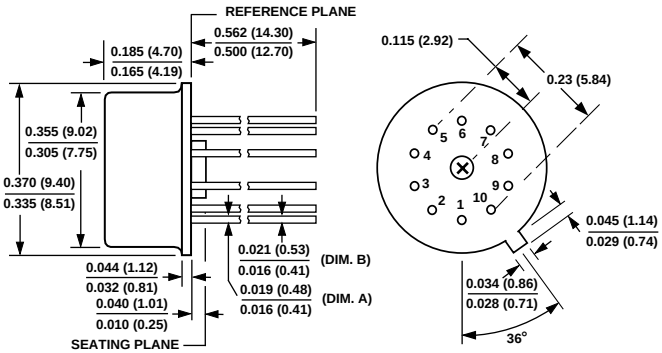


Figure 23. Frequency Response vs. Divider Denominator Input Voltage

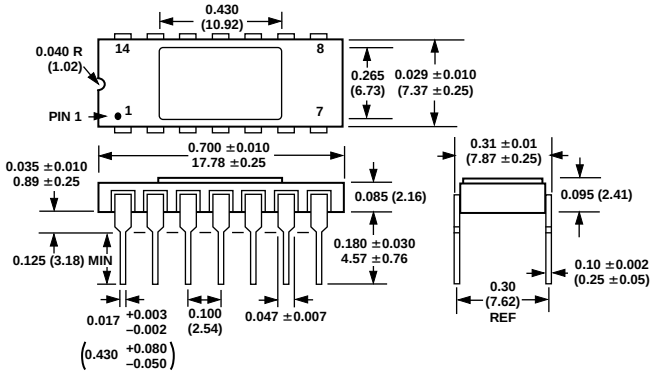
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

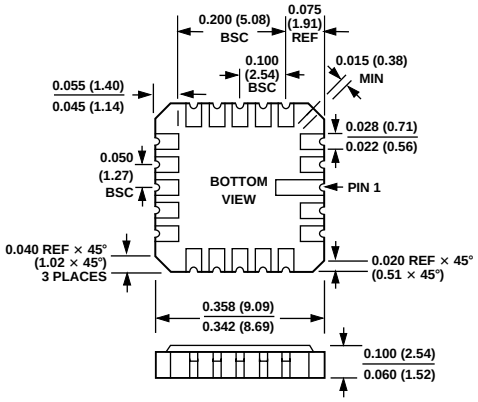
H-10A Package
TO-100



D-14 Package
TO-116



E-20A Package
LCC



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