MOTOROLA

AD562

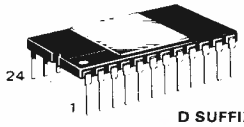
COMPLETE HIGH-SPEED 12-BIT MULTIPLYING D/A CONVERTER

The AD562 is a monolithic 12-bit resolution D/A converter. Active laser trimming of thin-film ladder network, span and bipolar offset resistors at wafer level provide linearity of better than ±1/2 LSB. An innovative bit switching scheme provides fast settling time yet enables selection of CMOS or TTL thresholds which are retained over a wide V_{CC} range from 4.5 to 16.5 volts. Internal precision span resistors allow output voltage options of 0 to 5.0 V, 0 to 10 V, ±2.5 V, ±5.0 V, and ±10 V. The AD562 multiplies in two quadrants when varying the reference input voltage. 12-bit accuracy and fast settling time make this converter ideal for applications such as fast A/D converters, CRT display generation waveform synthesis, precision instruments, and data acquisition systems.

- True 12-Bit Linearity: ±1/2 LSB Max
- Fast Settling Time: ±1/2 LSB in 200 ns Typ
- Fully Monotonic Over Temperature Range
- Low Gain Drift: 3 ppm/°C Max
- True Binary Coded Inputs
- Selectable Digital Thresholds
- Internal Span Resistors for Generating Output Voltage
- Low Power Consumption: 210 mW

LASER TRIMMED HIGH-SPEED 12-BIT MULTIPLYING D/A CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



D SUFFIX
CERAMIC PACKAGE
CASE 716-06

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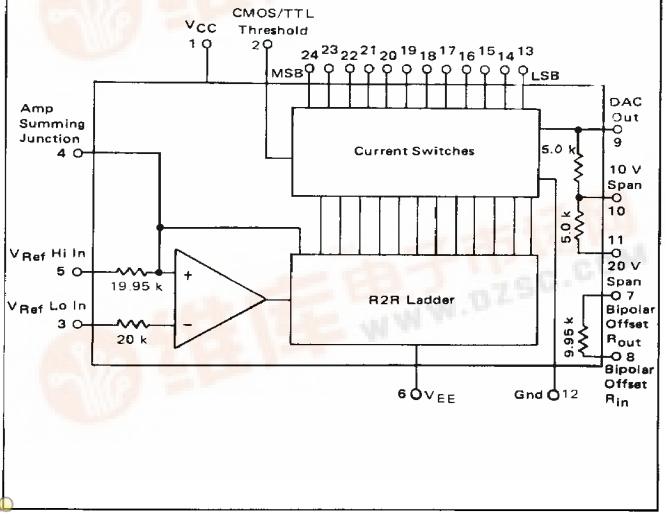
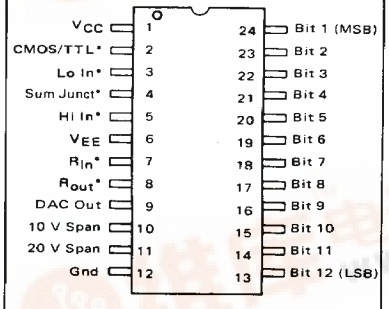
BLOCK DIAGRAM



PIN CONNECTIONS



Pin 2 = CMOS/TTL Threshold
Pin 3 = V_{Ref} Lo In
Pin 4 = Amp Summing Junction
Pin 5 = V_{Ref} Hi In
Pin 7 = Bipolar Offset R_{in}
Pin 8 = Bipolar Offset R_{out}

ORDERING INFORMATION

Device	Temperature Range	Accuracy @ 25°C
AD562KD	0°C to +70°C	±1/2 LSB
AD562AD	-25°C to +85°C	±1/2 LSB
AD562SD	-55°C to +125°C	±1/4 LSB

MAXIMUM RATING (T_A = 25°C, Ratings are referred to Ground [Pin 12] unless otherwise noted.)

Rating		Symbol	Value	Unit
Power Supply Voltage		V_{CC} V_{EE}	+18 −18	Vdc
Digital Input Voltage (Pins 13 to 24)		V_I	−5.0 to +18	Vdc
CMOS/TTL Threshold Select (Pin 2)		—	0 to V_{CC}	Vdc
V_{Ref} Hi In (Pin 5)		—	V_{EE} to V_{CC}	Vdc
V_{Ref} Lo In (Pin 3)		—	±1.0	Vdc
Applied Output Voltage (Pin 9)		V_O	−7.0 to V_{CC}	Vdc
Bipolar Offset to Analog Ground (Pin 7 or 8)		—	V_{EE} to V_{CC}	Vdc
Ten Volt Span Resistor to Analog Ground (Pin 10)		—	V_{EE} to V_{CC}	Vdc
Twenty Volt Span Resistor to Analog Ground (Pin 11)		—	V_{EE} to V_{CC}	Vdc
Power Dissipation		P_D	1000	mW
Operating Temperature Range	AD562KD AD562AD AD562SD	T_A	0 to +70 −25 to +85 −55 to +125	°C
Storage Temperature Range		T_{stg}	−65 to +150	°C
Junction Temperature		T_J	+175	°C

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TERMINOLOGY

Nonlinearity (Relative Accuracy) — Maximum output deviation from ideal straight line connecting zero and full-scale readings, expressed as a fraction of LSB or percent of full scale.

Differential Nonlinearity — Maximum deviation in the readings of any two adjacent input bit codes from the ideal LSB step, expressed in fractions of LSB or percentage of full scale. A differential nonlinearity value greater than 1 LSB may lead to nonmonotonic operation.

Monotonicity — For every increase in the input digital word, the output current either remains the same or increases.

The complete AD562 Series is guaranteed to be monotonic over temperature.

Settling Time — The elapsed time from the input transition until the output has settled within an error band about its final value.

The worst case switching condition occurs when all bits are switched "on", which corresponds to a low-to-high transition for all bits. This time is typically 200 ns for the output to settle to within ±1/2 LSB for 12-bit accuracy. The turn-off time is typically 120 ns. These times apply when the output swing is limited to a small (<0.5 V) swing and the external output capacitance is under 10 pF.

Gain Error — The difference between the actual full scale range (difference in output between all bits on, and all bits off) and the ideal full scale range. Based on a 0 to 10 V output configuration, the ideal FSR is $\frac{4095}{4096} \times 10 = 9.99756$ V.

Gain error is expressed in percentage of full scale (FS).

Unipolar Offset Error — Using the configuration shown in Figure 1, with R1 = 50 ohms and with all bits off, the output voltage reading compared to zero is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Offset Error — Using the configuration shown in Figure 2, with R2 = 50 ohms with all bits off, the output voltage reading compared to the ideal negative full scale value is expressed as a percentage of the full scale range. Offset voltage of the output op amp must be nulled.

Bipolar Zero Error — Using the configuration shown in Figure 2, with R1 = R2 = 50 Ω, with the MSB on and all other bits off, the output voltage reading compared to zero is expressed as a percentage of the full-scale range. Offset voltage of the output op amp must be nulled.

Temperature Coefficients — (Unipolar Offset, Bipolar Offset, Gain and Differential Nonlinearity). The maximum deviation of the particular parameter over the specified temperature range, divided by the temperature range, expressed in parts per million of Full Scale Range per degree C.

Compliance Voltage Range — The output terminal voltage range which will provide specified output resistance and current characteristics. The compliance voltage is specified with V_{EE} = −15. The compliance voltage range follows as V_{EE} is varied.

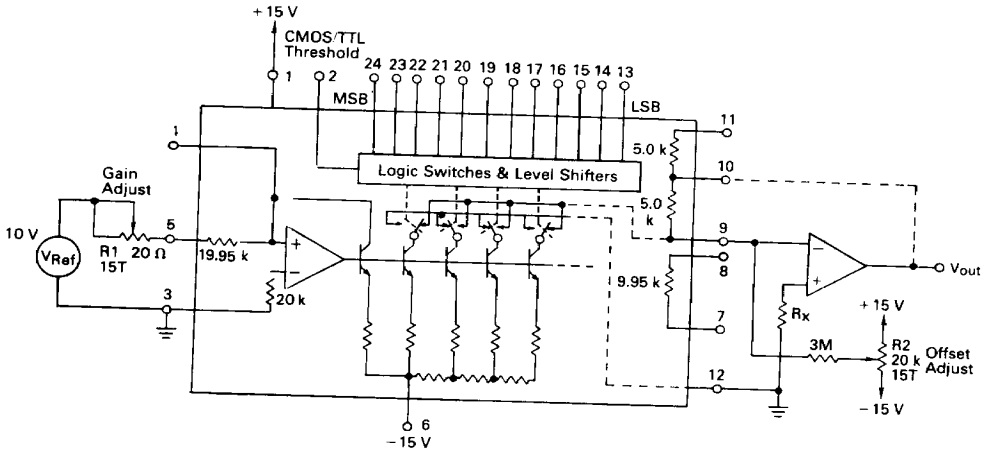
Power Supply Sensitivity — The change in full scale current caused by a change in V_{EE} or V_{CC} expressed in ppm of full scale current per percent change in V_{EE} or V_{CC}.

ELECTRICAL CHARACTERISTICS (V_{CC} = +15 V, V_{EE} = −15 V, V_{Ref} = 10 V, Pin 2 open, T_A = 25°C unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
TTL Digital Logic Levels (All Bits) (4.5 V ≤ V_{CC} ≤ 16.5 V, T_{low} to T_{high}, see Note 1) Bit On, Logic "1" Bit Off, Logic "0"	 V_{IH} V_{IL}	 2.0 —	 — —	 — 0.8	V
CMOS Digital Logic Levels (All Pins) (4.5 V ≤ V_{CC} ≤ 16.5 V, T_{low} to T_{high}, see Note 1, Pin 2 tied to Pin 1) Bit On, Logic "1" Bit Off, Logic "0"	 V_{IH} V_{IL}	 70% V_{CC} —	 — —	 — 30% V_{CC}	V
Digital Input Current, CMOS/TTL Levels — Bit On, Logic "1"	I_{IH}	—	+0.02	+0.1	μA
(T_{low} to T_{high}, see Note 1) Bit On, Logic "1" Bit Off, Logic "0"	 I_{IH} I_{IL}	 — —	 — -2.0	 +1.0 -75	
Programmable Output Range (See Figures 1 and 2)	—	— — — — —	0 to +5.0 -2.5 to +2.5 0 to +10 -5.0 to +5.0 -10 to +10	— — — — —	V
Output Current Unipolar (All Bits On) Bipolar (All Bits On or Off)	I_O	 -1.6 ±0.8	 -2.0 ±1.0	 -2.4 ±1.2	mA
Output Resistance (Exclusive of Span Resistors)	R_O	1.0	5.0	—	MΩ
Output Capacitance	C_O	—	25	—	pF
Output Compliance Voltage Range (T_{low} to T_{high}, see Note 1)	V_{OC}	-5.0	—	+10	V
Nonlinearity AD562KD/AD562AD AD562SD	NL	— — — —	±1/4 (0.006) ±1/8 (0.003)	±1/2 (0.012) ±1/4 (0.006)	LSB % of FS LSB % of FS
Differential Nonlinearity	—	—	—	±1/2	LSB
Differential Nonlinearity (T_{low} to T_{high}, see Note 1)	Monotonicity Guaranteed				
Gain Error — Figure 1, R1 = Fixed 50 Ω	—	—	±0.05	±0.15	% of FS
Offset Error Unipolar — Figure 1 Bipolar — Figure 2, R2 = Fixed 50 Ω	—	 — —	 ±0.01 ±0.05	 ±0.05 ±0.15	% of FS
Bipolar Zero Error — Figure 2, R1 = R2 = Fixed 50 Ω	—	—	±0.05	±0.15	% of FS
Gain Adjustment Range — Figure 1	—	±0.20	±0.25	—	% of FS
Bipolar Offset Adjustment Range — Figure 2	—	±0.20	±0.25	—	% of FS
Temperature Coefficients (T_{low} to T_{high}, see Note 1) Unipolar Zero — AD562KD/AD562AD AD562SD Bipolar Zero — All Devices Gain — All Devices Differential Nonlinearity — All Devices	—	 — — — — —	 — — — — 1.0	 1.0 2.0 4.0 3.0 	ppm/°C
Settling Time to 1/2 LSB All Bits On-to-Off or Off-to-On	t_s	—	0.2	1.0	μs
Reference Input Impedance	Z_{in}	15	20	25	kΩ
Power Supply Current (V_{CC} +4.5 to +16.5 Vdc) (V_{EE} -10.8 to -16.5 Vdc)	 I_{CC} I_{EE}	 — —	 6.0 -8.0	 10 -12	mA
Power Supply Gain Sensitivity (V_{CC} +4.5 to 5.5 Vdc) (V_{CC} +13.5 to +16.5 Vdc) (V_{EE} -10.8 to -16.5 Vdc)	 $PSSI_{FS+}$ $PSSI_{FS+}$ $PSSI_{FS-}$	 — — —	 — — —	 2.0 2.0 6.0	ppm of FS/%

Note 1. T_{low} = −55°C for AD562SD, −25°C for AD562AD, 0°C for AD562KD; T_{high} = +125°C for AD562SD, +85°C for AD562AD, +70°C for AD562KD

FIGURE 1 — AD562 IN TYPICAL UNIPOLAR CONNECTION SCHEME



UNIPOLAR DAC OPERATION

A typical circuit configuration for unipolar operation of AD562 is shown in Figure 1.

Step 1 — Output Range

Determine which output range is required. For +5.0 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier output and short Pin 9 to Pin 11. For +10 Volt FS range, connect Pin 10 to external operational amplifier output, Pin 11 remains unconnected.

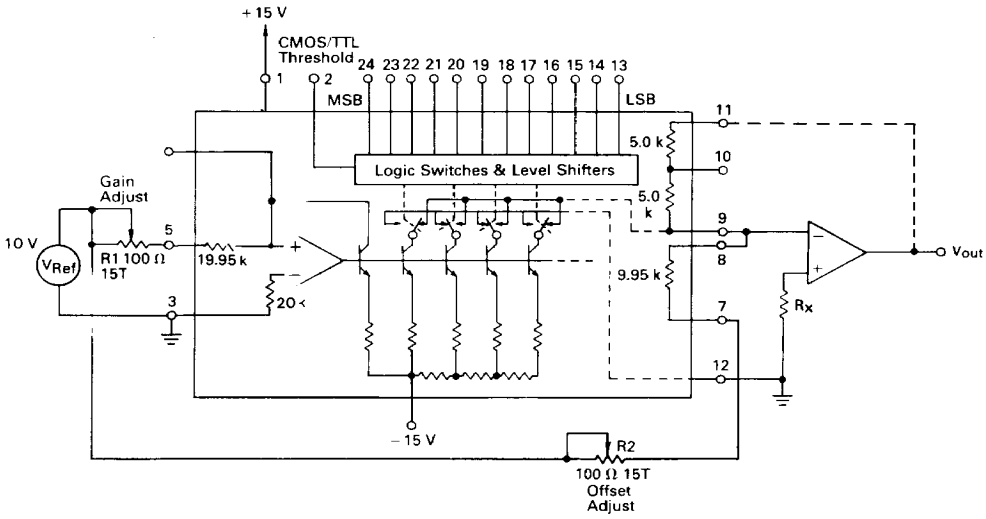
Step 2 — Zero Adjust

Turn all bits OFF and adjust R2 until external operational amplifier output is 0 Volts.

Step 3 — Gain Adjust

Turn all bits ON. Adjust R1 until operational amplifier output reaches 4.9988 Volts for +5.0 Volt range or 9.9976 for +10 Volt range.

FIGURE 2 — AD562 IN TYPICAL BIPOLAR CONNECTION SCHEME



BIPOLAR DAC OPERATION

A typical circuit configuration for bipolar operation of AD562 is shown in Figure 2.

Step 1 — Output Range

Determine which output range is required. For ±2.5 Volt full scale (FS) range, connect Pin 10 to output of external operational amplifier and short Pin 9 to Pin 11. For ±5.0 Volt FS range, connect Pin 10 to output of external operational amplifier, Pin 11 remains unconnected. For ±10 Volt FS range, connect Pin 11 to output of external operational amplifier, Pin 10 remains unconnected.

Step 2 — Offset Adjust

Turn all bits OFF and adjust R2 until operational amplifier output is:

-2.5000 Volt for ±2.5 Volt range
-5.0000 Volt for ±5.0 Volt range
-10.0000 Volt for ±10 Volt range

Step 3 — Gain Adjust (Bipolar Zero)

Turn MSB ON and all other bits OFF. Adjust R1 until operational amplifier output is 0 Volts.

NOTES:

1. For TTL and DTL compatibility, leave Pin 2 open.
2. For high voltage CMOS compatibility, short Pin 2 to Pin 1.
3. Supplies should be bypassed with 0.1 μF capacitors.
4. In unipolar operation, R_X should be made equal to the internal feedback resistor. In bipolar, R_X, equals the feedback resistor in parallel with 10 k.