24-Bit, 10mW, 125ksps Analog to Digital Converter in 16 lead TSSOP

Preliminary Technical Data

AD7766

FEATURES

High performance 24-bit ADC
- 114dB SNR at 31.25 KHz output data rate
- 111dB SNR at 62.5 KHz output data rate
- 108dB SNR at 125 KHz output data rate

Max 20mW Power Consumption
- 10mW typ at 31.25 KHz output data rate
- 12mW typ at 62.5 KHz output data rate
- 15 mW typ at 125 KHz output data rate

High DC accuracy
- 24 Bits No Missing Codes (NMC)
- Integral Non Linearity 15 ppm

Low temperature drift
- Offset Drift ±25 nV/°C

On Chip Low pass FIR filter
- Linear Phase Response
- Passband Ripple: ±0.005dB
- Stopband Attenuation: 100dB

2.5V Supply with 1.8V/2.5V/3V/3.6V logic interface

Flexible Interfacing options
- Synchronization of multiple devices
- Daisy Chain capability

Temp Range -40°C to 105°C

APPLICATIONS

Low-Power PCI/USB Data Acquisition Systems
Low-Power Wireless Acquisition Systems
Vibration Analysis
Instrumentation

FUNCTIONAL BLOCK DIAGRAM

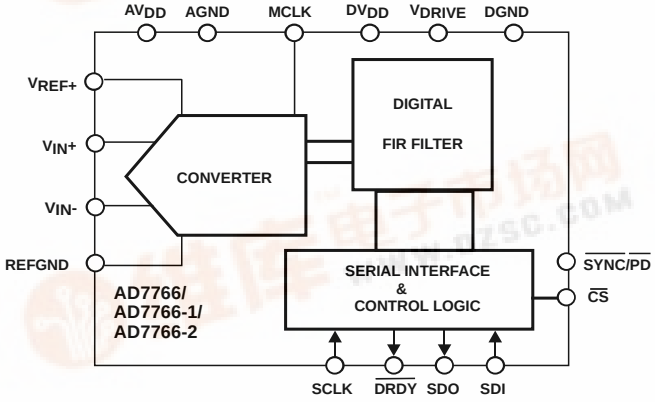

Figure 1.

PRODUCT OVERVIEW

The AD7766 is high performance 24-bit over-sampled analog to digital converter combining wide dynamic range and input bandwidth with an on chip FIR filter while consuming only 20mW max power in a 16 pin TSSOP package.

Specifically designed for ultra low power data acquisition, providing 24-bit resolution and high SNR makes the device ideal for measuring small signal changes over a wide dynamic range. This is particularly important in many data acquisition applications where small changes are measured on larger AC or DC signals. In addition the AD7766 provides excellent DC accuracy and drift specifications making the device suitable where DC data also needs to be acquired. The AD7766 improves SNR performance and simplifies anti aliasing requirements through over-sampling which is important in minimizing input signal distortion to the inputs of the ADC. A high performance on-chip FIR filter subsequently filters the over-sampled data and removes out of band noise. A $\overline{\text{SYNC}}/\overline{\text{PD}}$ (Synchronisation/Power down) pin is an added feature, allowing for easy synchronization of multiple devices. The device operates from -40°C to 105°C.

By combining wide dynamic range and high SNR at output data rates up to 125ksps with ultra low power the AD7766 provides a compact solution for low power data acquisition such as PCI or USB based systems.

RELATED DEVICES

Table 1. 24 bit Analog to Digital Converters

Part No	Speed	Description
AD7760	2.5MSPs	100dB Dynamic Range[1] On-board Diff Amp & Ref Buffer Parallel, Variable Decimation
AD7762/3	625KSPs	109dB Dynamic Range[1] On-Board Diff Amp & Ref buffer Parallel/Serial, Variable Decimation
AD7764	312KSps	109dB Dynamic Range[1] On-board Diff Amp & Ref Buffer Serial, Variable Decimation (pin)
AD7765	156KSPs	112dB Dynamic Range[1] On-board Diff Amp & Ref Buffer Serial,Variable Decimation (pin)
AD7767	125KSPs	109dB Dynamic Range[1] 10mW power dissipation Serial interface

[1] Dynamic Range at max output data rate.

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Parameter	Test Conditions/Comments	Specifcation	Unit
OUTPUT DATA RATE			
AD7766	Decimate × 8	125	KHz max
AD7766-1	Decimate × 16	62.5	KHz max
AD7766-2	Decimate × 32	31.25	KHz max
ANALOG INPUT[1]			
Differential Input Voltage	Vin(+) – Vin(-)	$\pm V_{REF}$	V pk-pk
Absolute Input Voltage	Vin(+)	-0.1 | $+V_{REF}$ + 0.1	V min | max
	Vin(-)	-0.1 | $+V_{REF}$ + 0.1	
Common mode Input Voltage		$V_{REF}/2 \pm 0.1$	V
Input Capacitance			pF typ
Differential Input Impedance			Ohms
DYNAMIC PERFORMANCE			
AD7766	Decimate by 8, ODR = 125 ksps		
Dynamic Range[2]	Shorted inputs		dB typ
Signal to Noise Ratio (SNR)[2]		108	dB typ
Spurious Free Dynamic Range (SFDR)[2]		TBD	dBFS typ
Total Harmonic Distortion (THD) [2]		-96	dB max
Intermodulation Distortion (IMD) [2]		TBD	dB typ
AD7766-1	Decimate by 16, ODR = 62.5 ksps		
Dynamic Range[2]	Shorted inputs		dB typ
Signal to Noise Ratio (SNR)[2]		111	dB typ
Spurious Free Dynamic Range[2] (SFDR)		TBD	dBFS typ
Total Harmonic Distortion (THD) [2]		-96	dB max
Intermodulation Distortion (IMD) [2]		TBD	dB typ
AD7766-2	Decimate by 32, ODR = 31.25 ksps		
Dynamic Range[2]	Shorted inputs		dB typ
Signal to Noise Ratio (SNR) [2]		114	dB typ
Spurious Free Dynamic Range (SFDR)[2]		TBD	dBFS typ
Total Harmonic Distortion (THD) [2]		-96	dB max
Intermodulation Distortion (IMD) [2]		TBD	dB typ
DC ACCURACY[1]			
Resolution	No Missing Codes	24	Bits
Differential Nonlinearity[2]	Guaranteed monotonic to 24 bits		
Integral Nonlinearity[2]	16 bit linearity	15	ppm
Zero Error[2]		TBD	% typ
Gain Error[2]		TBD	% typ
Zero Error Drift[2]		±25	nV/°C typ
Gain Error Drift[2]		±0.3	ppm/°C typ
Power Supply Rejection[2]	f = 50Hz, 60Hz	TBD	dB typ
Common mode rejection[2]		TBD	dB
DIGITAL FILTER RESPONSE[1]			
Group Delay		37/ODR	µs typ
Settling time (latency)	Complete Settling	74/ODR	µs typ
Passband ripple		±0.005	dB max
Passband		TBD	Hz
-3dB bandwidth		TBD	Hz
Stopband		TBD	Hz
Stopband Attenuation		100	dB min

Parameter	Test Conditions/Comments	Specifcation	Unit
REFERENCE INPUT[1]			
V_{REF+} Input Voltage		+2.4	V min
		2 x AV_{DD}	V max
Reference Input Impedance		TBD	Ohms
DIGITAL INPUTS (Logic Levels)[1]			
V_{IL}		-0.3	Vmin
		0.3 x V_{DRIVE}	Vmax
V_{IH}		0.7 x V_{DRIVE}	Vmin
V_{IH}		V_{DRIVE} + 0.3	Vmax
Input Current		TBD	uA max
Input leakage		TBD	uA/pin max
Input Capacitance		TBD	pF max
Master Clock rate		1	MHz typ
Serial Clock rate		30	MHz max
DIGITAL OUTPUTS[1]			
Data Format	Serial 24 bits Two's Complement (MSB 1st)		
V_{OL}	I_{SINK} = +500 µA	0.4	V max
V_{OH}	I_{SOURCE} = -500 µA	V_{DRIVE} – 0.3	V min
POWER REQUIREMENTS[1]			
AV_{DD}		+2.375/+2.625	V min/max
DV_{DD}		+2.375/+2.625	V min/max
V_{DRIVE}		+1.7/+3.6	V min/max
AD7766 Current Specifications	125 Khz Output Data Rate		
AI_{DD}		1.4	mA typ
DI_{DD}		3.2	mA typ
I_{REF}		0.7	mA typ
I_{DRIVE}	V_{DRIVE} = 3.6V, Full-scale code output, TBD pF load.	0.8	mA typ
AD7766-1 Current Specifications	62.5 Khz Output Data Rate		
AI_{DD}		1.4	mA typ
DI_{DD}		1.8	mA typ
I_{REF}		0.7	mA typ
I_{DRIVE}	V_{DRIVE} = 3.6V, Full-scale code output, TBD pF load.	0.8	mA typ
AD7766-2 Current Specifications	31.25 Khz Output Data Rate		
AI_{DD}		1.4	mA typ
DI_{DD}		1.1	mA typ
I_{REF}		0.7	mA typ
I_{DRIVE}	V_{DRIVE} = 3.6V Full-scale code output, TBD pF load.	0.8	mA typ
Power Dissapation			
AD7766	125 KHz Output Data Rate (Dec × 8)	15	mW typ
AD7766-1	62.5 KHz Output Data Rate (Dec × 16)	12	mW typ
AD7766-2	31.25 KHz Output Data Rate (Dec × 32)	10	mW typ
Power Down [1]	(All decimation rates)	TBD	mW typ

[1] Specifications for all devices, AD7766, AD7766-1 and AD7766-2.
[2] See Terminology

TIMIMG DIAGRAMS

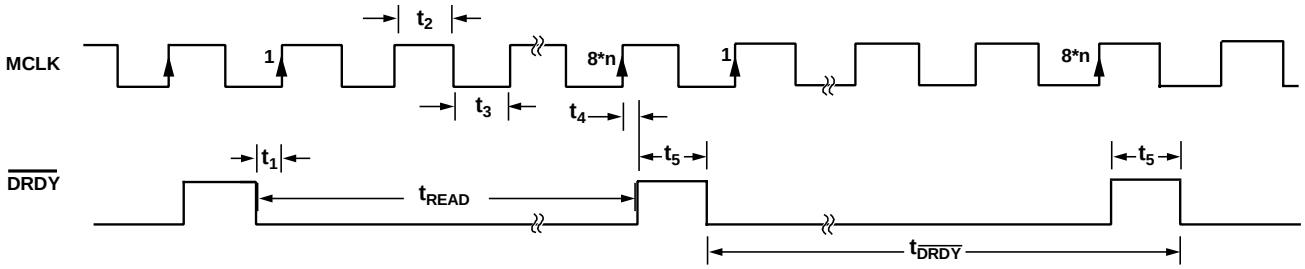

Figure 2.$\overline{DRDY}$ versus MCLK TimingDiagram. For AD7766 n=1(Decimate by8), AD7766-1 n=2(Decimate by 16), AD7766-2 n = 4(Decimate by 32).

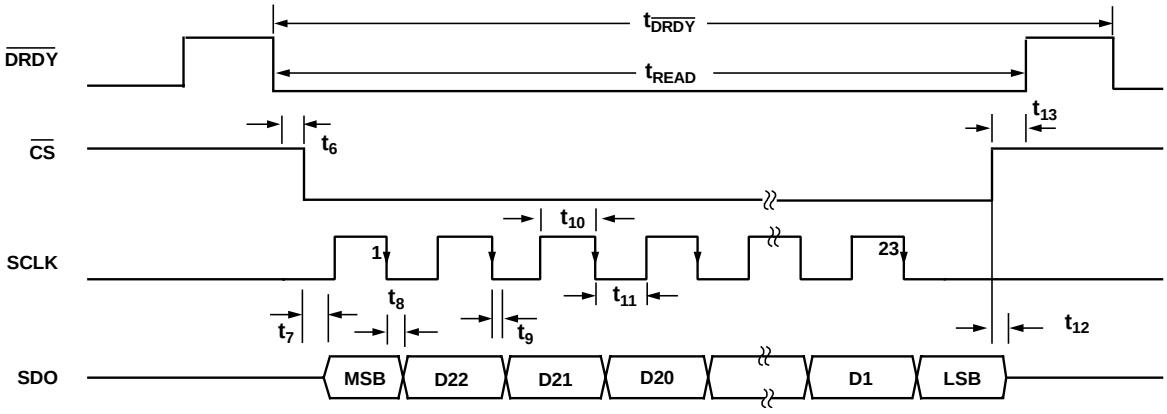

Figure 3.Serial timing diagram, reading data using $\overline{CS}$

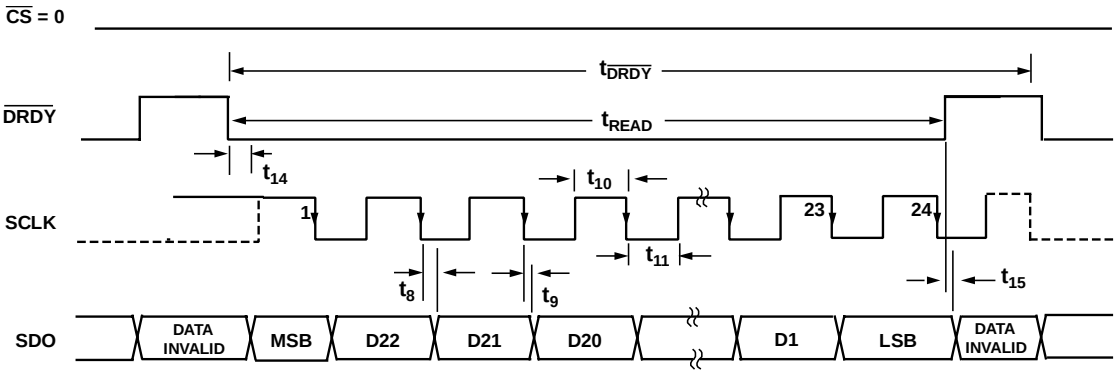

Figure 4.Serial timing diagram, reading data setting $\overline{CS}$ logic low.

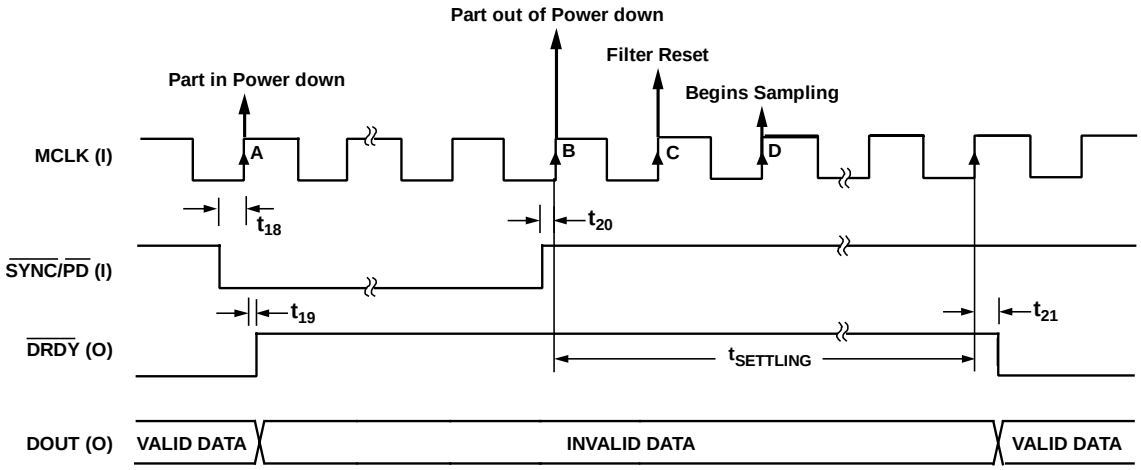

Figure 5.Reset and Synchronization and Power down timing diagram.

TIMING SPECIFICATIONS

Table 3. AV_{DD} = DV_{DD} = 2.5 V ± 5%, V_{DRIVE} = 1.7 V to 3.6 V, V_{REF} = 5 V, T_A = -40°C to +105°C, unless otherwise noted[1]

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DRDY Operation					
t_1		TBD		ns	$\overline{DRDY}$ Falling edge to MCLK rising edge
t_2		TBD		ns	MCLK High Pulsewidth
t_3		TBD		ns	MCLK Low Pulsewidth
t_4		TBD		ns	MCLK Rising edge to $\overline{DRDY}$Rising edge
t_5		TBD		ns	$\overline{DRDY}$ Pulse width
t_{READ} [2]		$t_{\overline{DRDY}}$ - t_5		ns	$\overline{DRDY}$ low period. Read data during this period.
$t_{\overline{DRDY}}$[2]		n×8×t_{MCLK}		ns	$\overline{DRDY}$ Period.
Read Operation					
t_6		0		ns	$\overline{DRDY}$ Falling Edge to $\overline{CS}$ Setup Time
t_7		TBD		ns	$\overline{CS}$ Falling Edge to SDO three-state disabled
t_8		TBD		ns	Data access time after SCLK falling edge
t_9		TBD		ns	SCLK Falling Edge to Data Valid hold time
t_{10}		TBD		ns	SCLK High Pulsewidth
t_{11}		TBD		ns	SCLK Low Pulsewidth
t_{12}		TBD		ns	Bus Relinquish Time after $\overline{CS}$ Rising Edge
t_{13}		0		ns	$\overline{CS}$ Rising Edge to $\overline{DRDY}$ Rising Edge
Read Operation with $\overline{CS}$ low					
t_{14}		TBD		ns	$\overline{DRDY}$ Falling Edge to Data valid Setup Time
t_{15}		0		ns	$\overline{DRDY}$ Rising Edge to Data Valid hold time
Daisy Chain Operation					
t_{16}		TBD		ns	SDI Valid to SCLK Falling Edge Setup Time
t_{17}		TBD		ns	SCLK Falling Edge to SDI Valid Hold Time
Synchronise Operation					
t_{18}		TBD		ns	$\overline{SYNC}$/$\overline{PD}$ Falling edge to MCLK Rising Edge
t_{19}		TBD		ns	MCLK Rising edge to $\overline{DRDY}$ Rising Edge
t_{20}		TBD		ns	$\overline{SYNC}$/$\overline{PD}$ Rising edge to MCLK Rising Edge
t_{21}		TBD		ns	MCLK Rising edge to $\overline{DRDY}$ Falling edge coming out of $\overline{SYNC}$/$\overline{PD}$
$t_{SETTLING}$[2]		592×n +2		t_{MCLK}	Filter Settling Time after a Reset or power down.

[1] Sample tested during initial release to ensure compliance. All input signals are specified with tr = tf = 5 ns (10% to 90% of DV_{DD}) and timed from a voltage level of 1.6 V

[2] n = 1 for AD7766, n= 2 for the AD7766-1, n=4 for the AD7766-2.

ABSOLUTE MAXIMUM RATINGS

Table 4. T_A = 25°C, unless otherwise noted.

Parameters	Rating
AV_{DD} to AGND	-0.3V to +3V
DV_{DD} to DGND	-0.3V to +3V
AV_{DD} to DV_{DD}	-0.3V to + 0.3V
V_{REF+} to V_{REF-}	-0.3V to +7V
V_{REF-} to AGND	-0.3V to + 0.3V
V_{DRIVE} to DGND	-0.3V to +6V
V_{IN+}, V_{IN-} to AGND	-0.3V to V_{REF} +0.3V
Digital inputs to DGND	-0.3V to V_{DRIVE} + 0.3V
Digital Outputs to DGND	-0.3V to V_{DRIVE} + 0.3V
AGND to DGND	-0.3V to + 0.3V
Input current to any pin except supplies[1]	±10mA
Operating temperature range	−40°C to +105°
Storage temperature range	−65°C to +150°C
Junction temperature	150°C
TSSOP Package	
θ_{JA} Thermal Impedance	150.4°C/W
θ_{JC} Thermal Impedance	27.6°C/W
Lead temperature, soldering	
Vapor phase (60 secs)	215°C
Infrared (15 secs)	220°C
ESD	TBD kV

[1]Transient currents of up to TBD mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

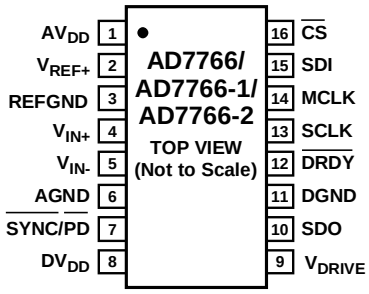

Figure 6.16-Lead TSSOP Pin Configuration

Table 5. Pin Function Descriptions

Pin Number	Pin Mnemonic	Description
1	AV_{DD}	+2.5V Analog power supply.
2	V_{REF+}	Reference Input for the AD7766. An external reference must be applied to this input pin. The VREF+ input can range from 2.4V to 5V. The reference voltage input is independent of the voltage magnitude applied to the AV_{DD} pin.
3	REFGND	Reference Ground. Ground Connection for the reference voltage. The input reference voltage (V_{REF+}) should be decoupled to this pin.
4	V_{IN}+	Positive input of the Differential Analog input.
5	V_{IN}-	Negative input of the Differential Analog input.
6	AGND	Power supply ground for Analog circuitry.
7	$\overline{SYNC}/\overline{PD}$	Synchronisation and Power Down Input pin. This pin has dual functionality. It can be used to synchronise multiple AD7766 devices and/or put the AD7766 device into power down mode. See the Power Down, Reset & Synchronization section for further details.
8	DVDD	Digital Power Supply input. This pin can be connected directly to V_{DRIVE}.
9	V_{DRIVE}	Logic power supply input, +1.8V to +3.6V. The voltage supplied at this pin will determine the operating voltage of the digital logic interface.
10	SDO	Serial Data Output (SDO). The conversion result from the AD7766 is output on the SDO pin as a 24 bit, two's complement, MSB first, serial data stream.
11	DGND	Digital logic power supply ground
12	$\overline{DRDY}$	Data Ready Output. A falling edge on the $\overline{DRDY}$ signal indicates that a new conversion data result is available in the output register of the AD7766. See the AD7766 Interface section for further details.
13	SCLK	Serial Clock Input. The SCLK input provides the serial clock for all serial data transfers with the AD7766 device. See the AD7766 Interface Section for further details.
14	MCLK	Master Clock Input. The AD7766 sampling frequency is directly proportional to the MCLK frequency.
15	SDI	Serial Data Input. This is the Daisy-Chain input of the AD7766. See the Daisy Chaining section for further details.
16	$\overline{CS}$	Chip Select Input. The $\overline{CS}$ input selects the AD7766 device, and acts as an enable on the SDO pin. In cases where $\overline{CS}$ is used, the MSB of the conversion result is clocked onto the SDO line on the $\overline{CS}$ falling edge. The $\overline{CS}$ input allows multiple AD7766 devices to share the same SDO line. This allows the user to select the appropriate device by supplying it with a logic low $\overline{CS}$ signal, which enables the SDO pin of the device concerned. See the AD7766 Interface section for further details.

TYPICAL PERFORMANCE CHARACTERISTICS

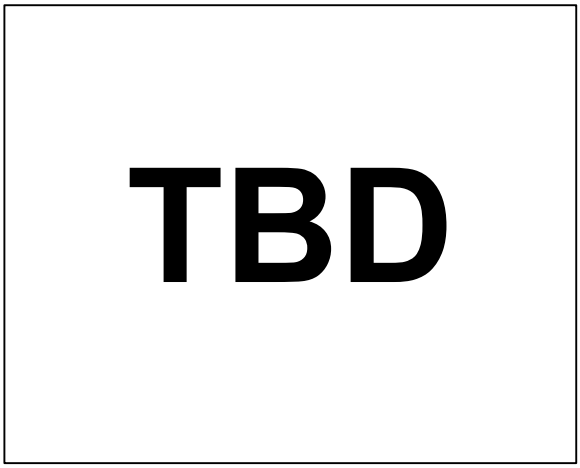

Figure 7

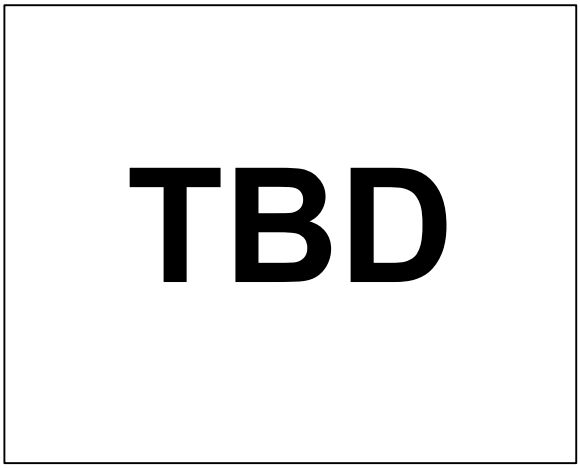

Figure 10

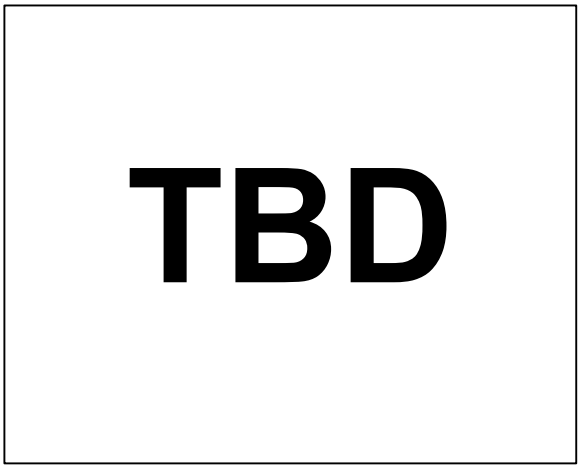

Figure 8

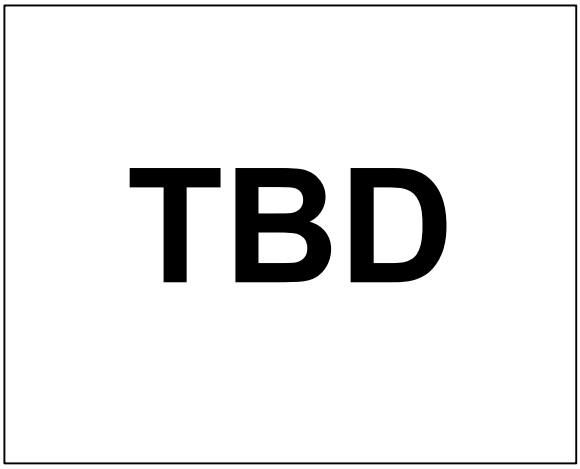

Figure 11

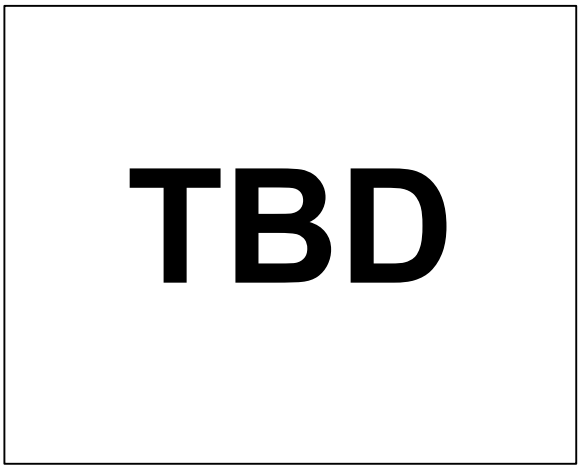

Figure 9

TERMINOLOGY

Signal-to-Noise Ratio (SNR)
SNR is the ratio of the rms value of the actual input signal to the ms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of harmonics to the fundamental. For the AD7766, it is defined as

$$THD\,(\mathrm{dB}) = 20 \log \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2 + V_6^2}}{V_1}$$

where:
V_1 is the rms amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the rms amplitudes of the second to the sixth harmonics.

Nonharmonic Spurious-Free Dynamic Range (SFDR)
SFDR is the ratio of the rms signal amplitude to the rms value of the peak spurious spectral component, excluding harmonics.

Dynamic Range
Dynamic range is the ratio of the rms value of the full scale to the rms noise measured with the inputs shorted together. The value for the dynamic range is expressed in decibels.

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities creates distortion products at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3, and so on. Intermodulation distortion terms are those for which neither m nor n are equal to 0. For example, the second-order terms include (fa + fb) and (fa − fb), and the third-order terms include (2fa + fb), (2fa − fb), (fa + 2fb), and (fa − 2fb).

The AD7766 is tested using the CCIF standard, where two input frequencies near the top end of the input bandwidth are used.

In this case, the second-order terms are usually distanced in frequency from the original sine waves, and the third-order terms are usually at a frequency close to the input frequencies. As a result, the second- and third-order terms are specified separately. The calculation of the intermodulation distortion is as per the THD specification, where it is the ratio of the rms sum of the individual distortion products to the rms amplitude of the sum of the fundamentals expressed in decibels.

Integral Nonlinearity (INL)
INL is the maximum deviation from a straight line passing through the endpoints of the ADC transfer function.

Differential Nonlinearity (DNL)
DNL is the difference between the measured and the ideal 1 LSB change between any two adjacent codes in the ADC.

Zero Error
Zero error is the difference between the ideal midscale input voltage (when both inputs are shorted together) and the actual voltage producing the midscale output code.

Zero Error Drift
Zero error drift is the change in the actual zero error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

Gain Error
The first transition (from 100 … 000 to 100 … 001) should occur for an analog voltage ½ LSB above the nominal negative full scale. The last transition (from 011 … 110 to 011 … 111) should occur for an analog voltage 1½ LSB below the nominal full scale. The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition, from the difference between the ideal levels.

Gain Error Drift
Gain error drift is the change in the actual gain error value due to a temperature change of 1°C. It is expressed as a percentage of full scale at room temperature.

THEORY OF OPERATION

The AD7766 is high performance 24-bit over-sampled analog to digital converter combining wide dynamic range and input bandwidth with an on chip FIR filter while consuming only 20mW max power in a 16 pin TSSOP package. The AD7766 is available with 3 preset decimation rates, 8, 16 and 32. Table 6 shows the three available models of the AD7766. The three models differ in the preset decimation rate employed. The output data rates of the AD7766, AD7766-1 and the AD7766-2 are relative to each of their preset decimation rates.

Table 6. AD7766 Models.

	Decimation Rate	Output Data Rate (ODR)
AD7766	8	125 KHz
AD7766-1	16	62.5 KHz
AD7766-2	32	31.25 KHz

In decimate × 8 mode the output will be updated every 8 MCLK periods, offering a maximum output data rate of 125KHz for the AD7766 device. The AD7766-1 model is set in decimate × 16 mode, and the AD7766-2 is preset to decimate × 32. The decimation ratio of each model indicates the level of filtering employed in the on-board digital FIR filter. The higher filter decimation rates provide the user with increased dynamic specifications; however, there is a trade-off on throughput as the filter delay increases as higher decimation rates are introduced.

AD7766 TRANSFER FUNCTION

The AD7766 outputs its conversion results in a 2's complement, 24-bit serial format. The fully differential inputs VIN+ and VIN- are scaled by the AD7766 relative to the reference voltage input (VREF+) as shown in Figure 12.

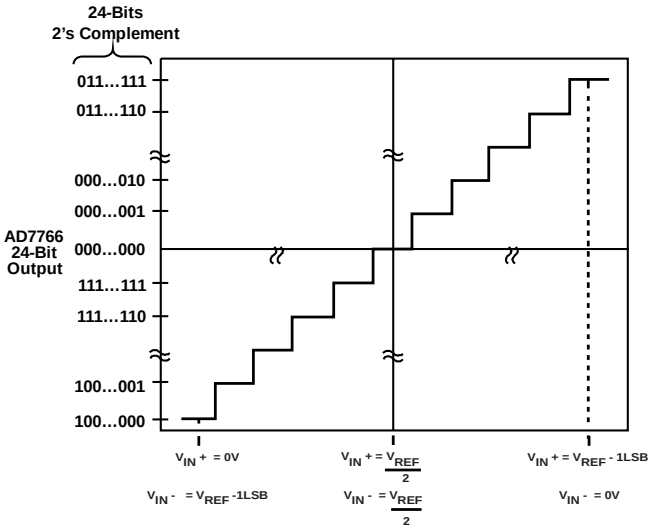

Figure 12.AD7766 TransferFunction

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AD7766 INTERFACE

The AD7766 provides the user with a flexible serial interface enabling the user to implement the most desireable interfacing scheme for their application. The AD7766 interface is comprised of seven different signals. Five of these signals are inputs : MCLK $\overline{CS}$, $\overline{SYNC}/\overline{PD}$, SCLK, and SDI. There are two output signals, $\overline{DRDY}$ and SDO.

INITIAL POWER-UP

On initial power up, apply a continuous MCLK signal. Iit is recommended that the user reset the AD7766 to clear the filters and ensure correct operation. The reset is completed as described in Figure 5, with all events occurring relative to the rising edge of MCLK. A negative pulse on the $\overline{SYNC}/\overline{PD}$ input initiates the reset and the $\overline{DRDY}$ output will switch to logic high and will remain high until valid data is available.. Following the power up of the AD7766 by transitioning the $\overline{SYNC}/\overline{PD}$ pin to logic high, a settling time is required before valid data is output by the device. This settling time, $t_{SETTLING}$, is a function of the MCLK frequency and the decimation rate. Table 7 lists the settling time of each of the AD7766 models, and should be referenced to Figure 5..

Table 7. Filter settling time after $\overline{SYNC}/\overline{PD}$

	Decimation Rate	$t_{SETTLING}$ [1]
AD7766	8	$594 \times t_{MCLK} + t_{21}$
AD7766-1	16	$1,186 \times t_{MCLK} + t_{21}$
AD7766-2	32	$2,370 \times t_{MCLK} + t_{21}$

[1] $t_{SETTLING}$ is measured from the first MCLK rising edge after the rising edge of $\overline{SYNC}/\overline{PD}$ to the falling edge of $\overline{DRDY}$.

READING DATA

The AD7766 outputs its data conversion results in an MSB first, 2's complement 24-bit format on the Serial Data Output Pin (SDO). MCLK is the master clock, which controls all the AD7766 conversions. The SCLK is the serial clock input for the device. All data transfers take place with respect to the SCLK signal

The $\overline{DRDY}$ line is used as a status signal to indicate when the data is available to be read from the AD7766. The falling edge of $\overline{DRDY}$ indicates that a new data word is available in the output register of the device. $\overline{DRDY}$ stays low during the period that output data is permitted to be read from the SDO pin. The $\overline{DRDY}$ signal returns to logic high to indicate when *not* to read from the device. Ensure that a data read is not attempted during this period as the output register is being updated

The AD7766 offers the user the option of using a chip select input signal ($\overline{CS}$) in its data read cycle. The $\overline{CS}$ signal is a gate for the SDO pin and allows many AD7766 devices to share the same serial bus acting as an instruction signal to each of these devices indicating permission to use the bus. When $\overline{CS}$ logic high, the SDO line of the AD7766 is is tri-stated.

There are two distinct patterns that can be initiated to read data from the AD7766 device, these are for the cases when $\overline{CS}$ falling edge occurs after the DRDY falling edge and for the case when the $\overline{CS}$ falling edge occurs before the DRDY falling edge (when $\overline{CS}$ is set to logic low.

When the CS falling edge occurs after DRDY falling edge the MSB of the conversion result is becomes available on the SDO line on this CS falling edge. The remaining bits of the conversion result (MSB-1, MSB-2 ..etc) are clocked onto the SDO line by the falling edges of SCLK which follow the CS falling edge. Figure 3 details this interfacing scheme.

When CS is tied low the AD7766 serial interface can operate in 3-wire mode as shown in Figure 4. In this case the MSB of the conversion result is available on the SDO line on the falling edge of $\overline{DRDY}$. The remaining bits of the data conversion result (MSB-1, MSB-2 etc..) are clocked onto the SDO line by the subsequent SCLK falling edges.

POWER DOWN, RESET & SYNCHRONIZATION

The AD7766's $\overline{SYNC}/\overline{PD}$ pin allows the user to synchronise multiple AD7766 devices. This pin also allows the user to reset and power down the AD7766 device. These features are implemented relative to the rising edges of MCLK and are shown in Figure 5

To power down, reset or synchronise a device the AD7766 $\overline{SYNC}/\overline{PD}$ pin should be taken low. On the first rising edge of MCLK the AD7766 is powered down. The $\overline{DRDY}$ pin transitions to logic high indicating that the data in the output register is no longer valid. The status of the $\overline{SYNC}/\overline{PD}$ pin is checked on each subsequent rising edge of MCLK. On the first rising edge of MCLK after the $\overline{SYNC}/\overline{PD}$ pin is taken high the AD7766 is taken out of power down. On the next rising edge, the filter of the AD7766 is reset. On the following rising edge, the first new sample is taken.

A settling time, $t_{SETTLING}$, from the filter reset, must pass before valid data is output by the device (as listed in Table 7). The $\overline{DRDY}$ output goes logic low after $t_{SETTLING}$ to indicate when valid data is available on SDO for readback.

DAISY CHAINING

Daisy chaining devices allows numerous devices to use the same digital interface lines by cascading the outputs of multiple ADC's on a single data line. This feature is especially useful for reducing component count and wiring connections, e.g. in isolated multi-converter applications or for systems with a limited interfacing capacity. Data read-back is analogous to clocking a shift register where data is clocked on the falling edge of SCLK.

The block diagram in Figure 13 shows the way in which devices must be connected in order to achieve daisy chain functionality. This scheme operates by passing the output data of the SDO pin of an AD7766 device to the SDI input of the next AD7766 device in the chain. The data then continues through the chain until it is clocked onto the SDO pin of the first device on the chain.

READING DATA IN DAISY CHAIN MODE

An example of a daisy chain of four AD7766 devices is shown in Figure 13 and Figure 14. In the case illustrated in Figure 13 the output of AD7766 (A) is the output of the full daisy chain. The last device in the chain (AD7764(D)) will have its Serial Data In (SDI) pin connected to ground. All the devices in the chain must use common MCLK, SCLK, $\overline{CS}$ and $\overline{SYNC}/\overline{PD}$ signals.

To enable the daisy chain conversion process, apply a common $\overline{SYNC}/\overline{PD}$ pulse to all devices synchronizing all the devices in the chain (see Power Down, Reset & Synchronization section).

After applying a $\overline{SYNC}/\overline{PD}$ pulse to all the devices there is a delay (as listed in Table 7) before valid conversion data appears at the output of the chain of devices. As shown in Figure 14 the first conversion result is output from the device labeled AD7766(A). This 24-bit conversion result is then followed by the conversion results from the devices B, C and D respectively with all conversion results output in an MSB first sequence. The stream of conversion results are clocked through each device in the chain and are eventually clocked onto the SDO pin of the AD7766 (A) device. The conversion results of the all the devices in the chain must be clocked onto the SDO pin of the final device in the chain while its $\overline{DRDY}$ signal is active low. This is illustrated in the example shown where the conversion results from devices A, B, C, & D are be clocked onto SDO (A) in the time between the falling edge of $\overline{DRDY}$ (A) and the rising edge of $\overline{DRDY}$ (A).

CHOOSING THE SCLK FREQUENCY

As shown in Figure 13 the number of SCLK falling edges that occur during the period when $\overline{DRDY}$ (A) is active low must match the number of devices in the chain multiplied by 24 (the number of bits that must be clocked through onto SDO (A) for each device).

The period of SCLK (t_{SCLK}) required for a known daisy chain length using a known common MCLK frequency must therefore be established in advance. In the case where $\overline{CS}$ is tied logic low:

Equation 1

$$t_{SCLK} = \left[\frac{\{n \times 8 \times t_{MCLK}\} - \{t_{\overline{DRDY}\,Hi}\}}{24 \times K} \right]$$

Where K = Number of AD7766 devices in the chain
n is the AD7766 model number being used, where for AD7766 n= 1, AD7766-1 n= 2, AD7766-2 n= 4.
t_{MCLK} is the period of the MCLK.
$t_{\overline{DRDY}\ Hi}$ ~ Where $\overline{DRDY}$ is logic high between conversion results.

In the case where $\overline{CS}$ is used in the daisy chain interface:

Equation 2

$$t_{SCLK} = \left[\frac{\{n \times 8 \times t_{MCLK}\} - \{t_6 + t_7 + t_{13} + t_{\overline{DRDY}\,Hi}\}}{24 \times K} \right]$$

K = Number of AD7766 devices in the chain
n = AD7766 model number being used,
{AD7766 n= 1, AD7766-1 n= 2, AD7766-2 n= 4}
t_{MCLK} is the period of the MCLK.
$t_{\overline{CS}}$ = Time when $\overline{CS}$ is logic low (SDO is active).

If it is the case that the SCLK frequency is chosen firstly then it is the SCLK for any given MCLK, which determines the limit of the number of AD7766 devices that can be successfully daisy-chained.

Table 8 SCLK Frequency required for a given number of daisy-chained devices using a 1MCLK frequency.

No. Of Devices	MCLK (MHz)	SCLK Frequency (MHz)[1]
2	1	TBD/(n)
4	1	TBD/(n)
8	1	TBD/(n)
16	1	TBD/(n)

[1]n = 1 for AD7766, n= 2 for the AD7766-1, n=4 for the AD7766-2.

DAISY CHAIN MODE CONFIGURATION & TIMING DIAGRAMS

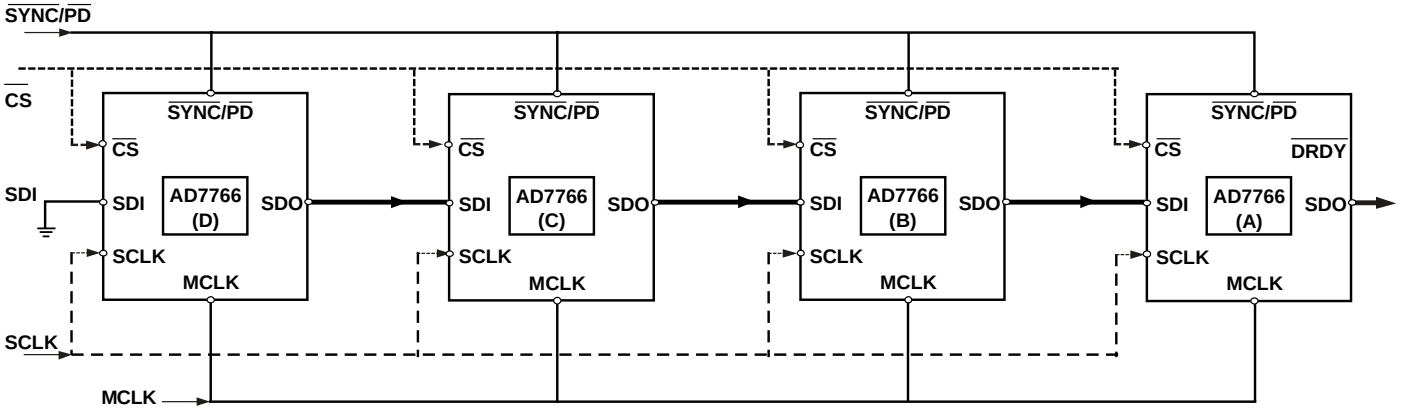


Figure 13 AD7766 Daisy chain configuration with 4 ×AD7766 devices..

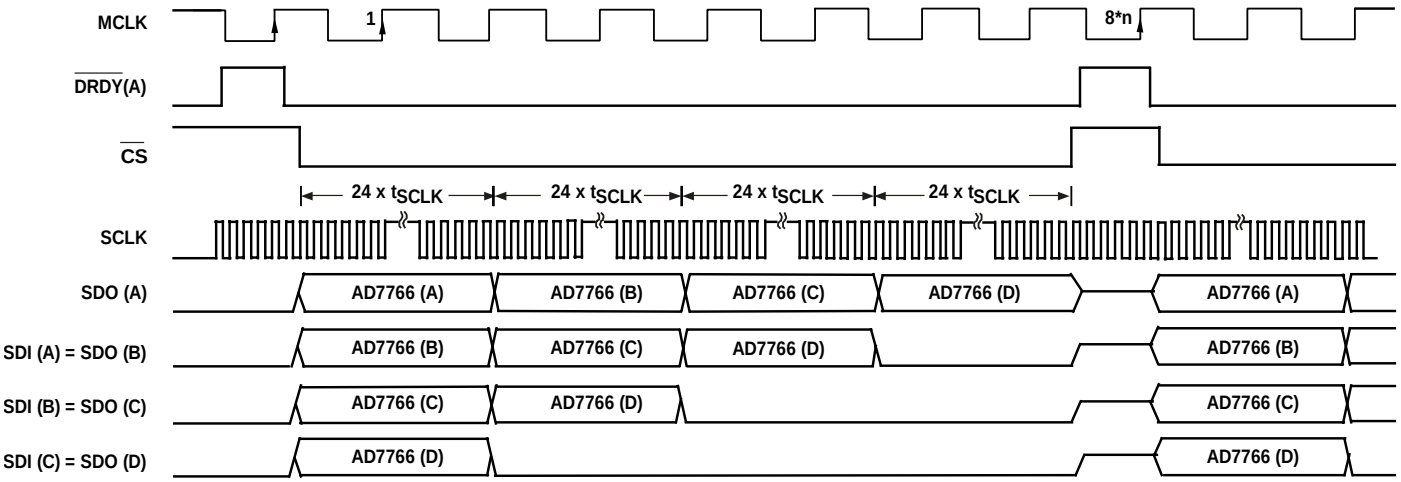


Figure 14 AD7766 Daisy chain Timing diagram. For AD7766 n=1, AD7766-1 n =2, AD7766-2 n= 4. Driving the AD7766

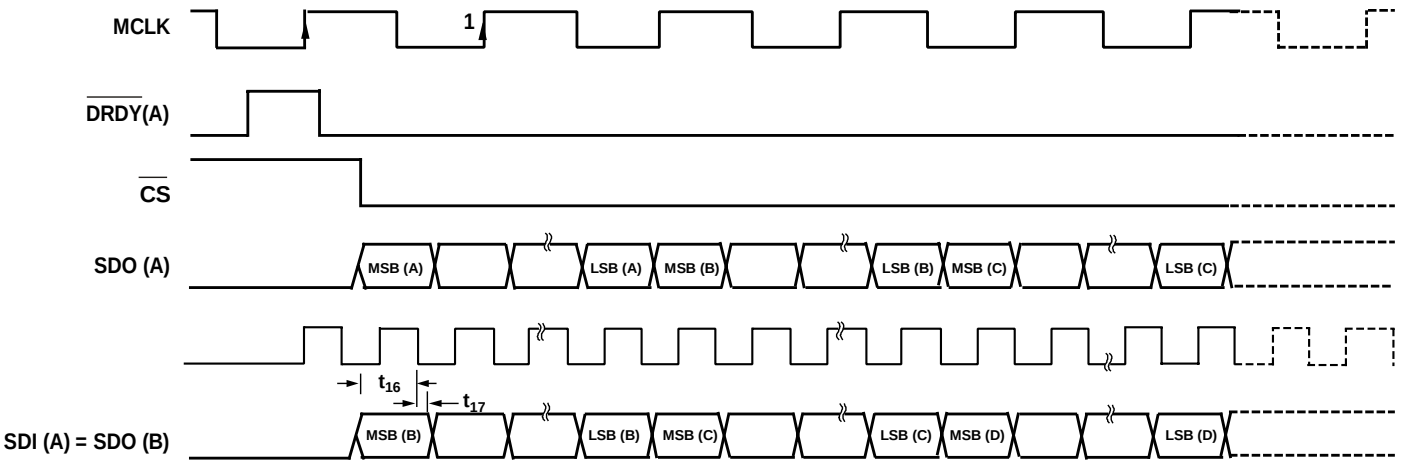


Figure 15 AD7766 Daisychain SDI Set-up and hold timing .

DRIVING THE AD7766

The AD7766 must be driven with fully differential inputs. The common mode voltage of the differential inputs to the AD7766 device and thus the limits on the differential inputs are set by the reference voltage V_{REF} applied to the device. The common mode voltage of the AD7766 is $V_{REF}/2$. Where the AD7766 V_{REF} pin is supplied with a 5V supply (the ADR435 is reccommended) the common mode is at 2.5V. This means that the max inputs that can be applied on the AD7766 differential inputs are a 5V pk-pk input around 2.5V.

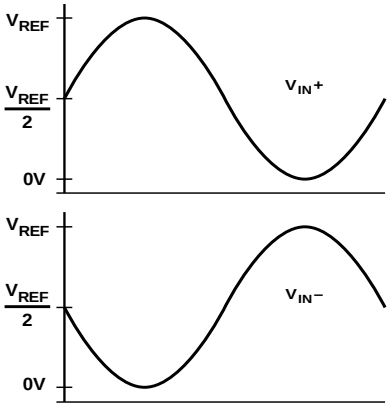


Figure 16 Maximum differential inputs to the AD7766

An analog voltage of 2.5V supplies the AD7766 AV_{DD} pin. However, the AD7766 allows the user to apply a reference voltage of up to 5V. This provides the user with an increased full-scale range, offering the user the option of using the AD7766 with a larger LSB voltage size Figure 16 shows the maximum and minimum inputs to the AD7766.

DIFFERENTIAL SIGNAL SOURCE

An example of some recommended driving circuitry that can be employed in conjunction with the AD7766 is shown in Figure 17. Figure 17 shows how the ADA4841 device can be used to drive an input to the AD7766 from a differential source. Each of the differential is driven by an ADA4841 device.

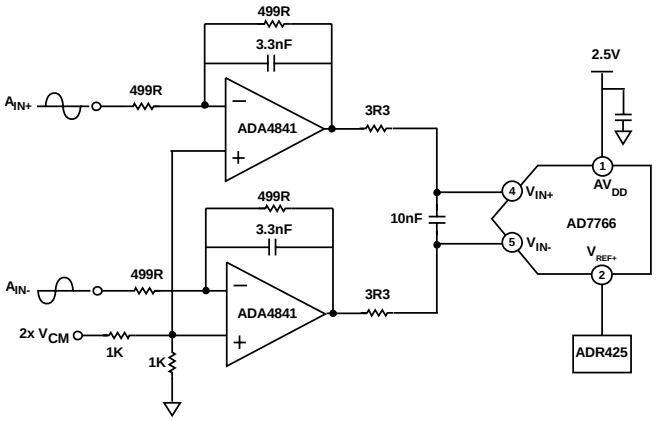


Figure 17. Driving the AD7766 from a fully differential source

SINGLE-ENDED SIGNAL SOURCE

In the case where the AD7766 is being supplied from a single-ended source the following application circuit can be used to drive the AD7766 device. Figure 18 shows how the ADA4941 single to differential amplifier can be used to create a fully differential input to the AD7766. The single-ended signal input is applied to the positive input of the ADA4941 device

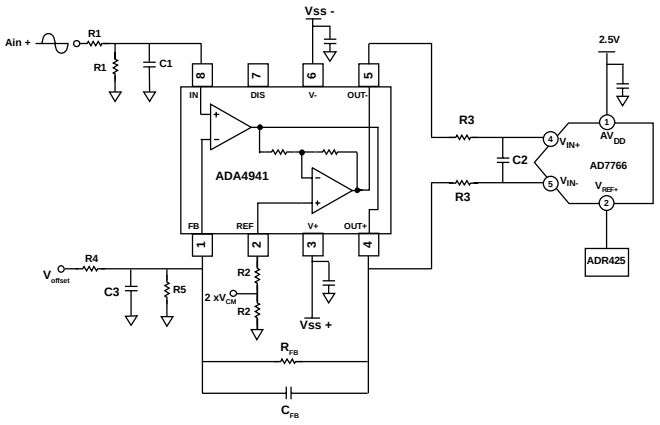


Figure 18. Driving the AD7766 from a single- ended source.

DIGITAL FILTERING

The AD7766 has an on-board digital FIR filter. The FIR filter's decimation rate is preset for each AD7766 model (See Table 6 for details). The digital filter consists of three separate filter blocks. Figure 19 shows the three constituent blocks of the filter. The order of decimation of the first filter block is either set as either 2, 4 or 8. The remaining sections have a decimation rate of 2. The settling time of the filter implemented on the AD7766, AD7766-1 and AD7766-2 is related to the amount of decimation employed, the filter settling time of each device is shown in Table 7.

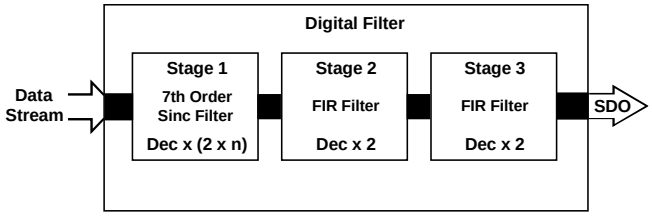


Figure 19.FIR filter stages
(n = 1 for AD7766, n= 2 for AD7766-1, n = 4 for AD7766-2)

The response of the digital filter on board the AD7766 is shown in Figure 20.. The filter provides stop-band attenuation of 100dB and passband ripple of ± 0.005dB.

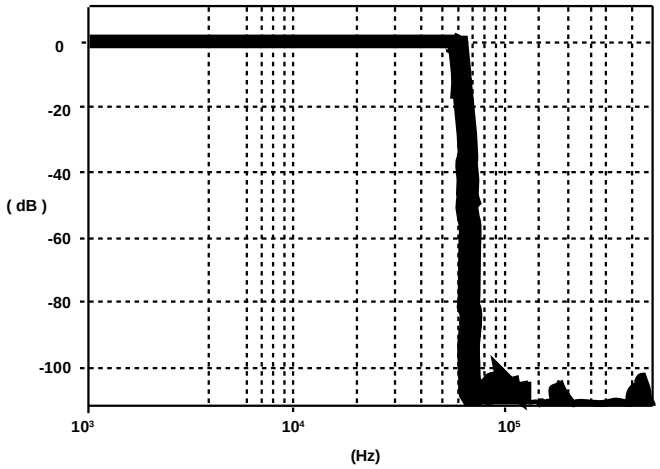
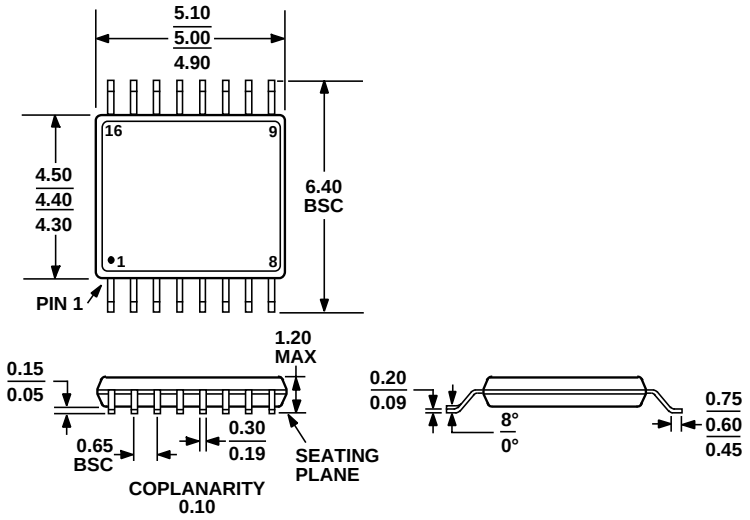


Figure 20.AD7766 Filter Response for AD7766 (MCLK =1Mhz, ODR = 125Khz)

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 21 16-Lead Thin Shrink Small Outline Package

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD7766BRUZ[1]	−40°C to +105°	16-Lead Thin Shrink Small Outline Package	RU-16
AD7766BRUZ-1[1]	−40°C to +105°	16-Lead Thin Shrink Small Outline Package	RU-16
AD7766BRUZ-2[1]	−40°C to +105°	16-Lead Thin Shrink Small Outline Package	RU-16

[1] Z = Pb-free part.

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