# Precision Instrumentation Amplifier

# AD8221

## FEATURES

- Available in space-saving MSOP package
- Gain set with 1 external resistor (gain range 1 to 1000)
- Wide power supply range: ±2.3 V to ±18 V
- Temperature range for specified performance:
  - –40°C to +85°C
- Operational up to 125°C[1]
- EXCELLENT AC SPECIFICATONS
  - 80 dB min CMRR to 10 kHz ( G = 1)
  - 825 kHz –3 dB bandwidth (G = 1)
  - 2 V/µs slew rate
- LOW NOISE
  - 8 nV/√Hz, @ 1 kHz, max input voltage noise
  - 0.25 µV p-p input noise (0.1 Hz to 10 Hz)
- HIGH ACCURACY DC PERFORMANCE (AD8221BR)
  - 90 dB min CMRR (G = 1)
  - 25 µV max input offset voltage
  - 0.3 µV/°C max input offset drift
  - 0.4 nA max input bias current

## APPLICATIONS

- Weigh scales
- Industrial process controls
- Bridge amplifiers
- Precision data acquisition systems
- Medical instrumentation
- Strain gages
- Transducer interfaces

## GENERAL DESCRIPTION

The AD8221 is a gain programmable, high performance instrumentation amplifier that delivers the industry's highest CMRR over frequency. The CMRR of instrumentation amplifiers on the market today falls off at 200 Hz. In contrast, the AD8221 maintains a minimum CMRR of 80 dB to 10 kHz for all grades at G = 1. High CMRR over frequency allows the AD8221 to reject wideband interference and line harmonics, greatly simplifying filter requirements. Possible applications include precision data acquisition, biomedical analysis, and aerospace instrumentation.

Low voltage offset, low offset drift, low gain drift, high gain accuracy, and high CMRR make this part an excellent choice in applications that demand the best dc performance possible, such as bridge signal conditioning.

## CONNECTION DIAGRAM

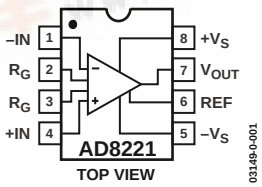


*Figure 1. SOIC and MSOP Connection Diagram*

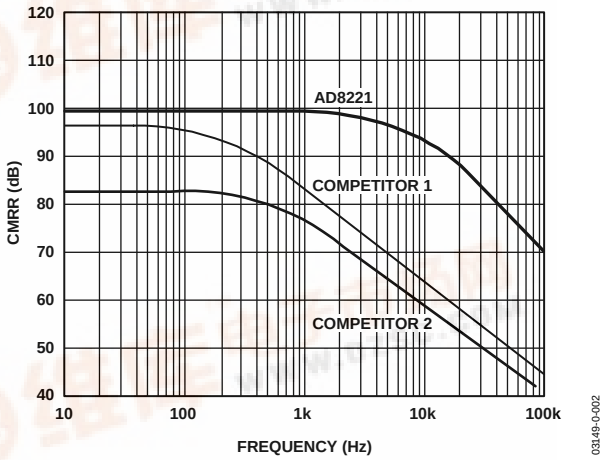


*Figure 2. Typical CMRR vs. Frequency for G = 1*

Programmable gain affords the user design flexibility. A single resistor sets the gain from 1 to 1000. The AD8221 operates on both single and dual supplies, and is well suited for applications where ±10 V input voltages are encountered.

The AD8221 is available in low cost 8-lead SOIC and MSOP packages, both of which offer the industry's best performance. The MSOP requires half the board space of the SOIC, making it ideal for multichannel or space-constrained applications.

Performance is specified over the entire industrial temperature range of –40°C to +85°C for all grades. Furthermore, the AD8221 is operational from –40°C to +125°C[1].

[1] See Typical Performance Curves for expected operation from 85°C to 125°C.



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.326.8703 

# TABLE OF CONTENTS



## REVISION HISTORY

**Revision A**
**11/03—Data Sheet Changed from Rev. 0 to Rev. A**

| Change | Page |
|---|---|
| Changes to Features | 1 |
| Changes to Specifications section | 4 |
| Change to Theory of Operation section | 13 |
| Change to Gain Selection section | 14 |

# SPECIFICATIONS

**Table 1. $V_S$ = ±15 V, $V_{REF}$ = 0 V, $T_A$ = +25°C, G = 1, $R_L$ = 2 kΩ, unless otherwise noted**

| | | AR Grade | | | BR Grade | | | ARM Grade | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | **Conditions** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Min** | **Typ** | **Max** | **Unit** |
| COMMON-MODE REJECTION RATIO (CMRR) | | | | | | | | | | | |
| CMRR DC to 60 Hz with 1 kΩ Source Imbalance | $V_{CM}$ = −10 V to +10 V | | | | | | | | | | |
| G = 1 | | 80 | | | 90 | | | 80 | | | dB |
| G = 10 | | 100 | | | 110 | | | 100 | | | dB |
| G = 100 | | 120 | | | 130 | | | 120 | | | dB |
| G = 1000 | | 130 | | | 140 | | | 130 | | | dB |
| CMRR at 10 kHz | $V_{CM}$ = −10 V to +10 V | | | | | | | | | | |
| G = 1 | | 80 | | | 80 | | | 80 | | | dB |
| G = 10 | | 90 | | | 100 | | | 90 | | | dB |
| G = 100 | | 100 | | | 110 | | | 100 | | | dB |
| G = 1000 | | 100 | | | 110 | | | 100 | | | dB |
| NOISE | $RTI\ noise = \sqrt{e_{NI}^2 + (e_{NO}/G)^2}$ | | | | | | | | | | |
| Voltage Noise, 1 kHz | | | | | | | | | | | |
| Input Voltage Noise, $e_{NI}$ | $V_{IN+}$, $V_{IN-}$, $V_{REF}$ = 0 | | | 8 | | | 8 | | | 8 | nV/√Hz |
| Output Voltage Noise, $e_{NO}$ | | | | 75 | | | 75 | | | 75 | nV/√Hz |
| RTI | f = 0.1 Hz to 10 Hz | | | | | | | | | | |
| G = 1 | | | 2 | | | 2 | | | 2 | | µV p-p |
| G = 10 | | | 0.5 | | | 0.5 | | | 0.5 | | µV p-p |
| G = 100 to 1000 | | | 0.25 | | | 0.25 | | | 0.25 | | µV p-p |
| Current Noise | f = 1 kHz | | 40 | | | 40 | | | 40 | | fA/√Hz |
| | f = 0.1 Hz to 10 Hz | | 6 | | | 6 | | | 6 | | pA p-p |
| VOLTAGE OFFSET[1] | | | | | | | | | | | |
| Input Offset, $V_{OSI}$ | $V_S$ = ±5 V to ±15 V | | | 60 | | | 25 | | | 70 | µV |
| Over Temperature | T = −40°C to +85°C | | | 86 | | | 45 | | | 135 | µV |
| Average TC | | | | 0.4 | | | 0.3 | | | 0.9 | µV/°C |
| Output Offset, $V_{OSO}$ | $V_S$ = ±5 V to ±15 V | | | 300 | | | 200 | | | 600 | µV |
| Over Temperature | T = −40°C to +85°C | | | 0.66 | | | 0.45 | | | 1.00 | mV |
| Average TC | | | | 6 | | | 5 | | | 9 | µV/°C |
| Offset RTI vs. Supply (PSR) | $V_S$ = ±2.3 V to ±18 V | | | | | | | | | | |
| G = 1 | | 90 | 110 | | 94 | 110 | | 90 | 100 | | dB |
| G = 10 | | 110 | 120 | | 114 | 130 | | 100 | 120 | | dB |
| G = 100 | | 124 | 130 | | 130 | 140 | | 120 | 140 | | dB |
| G = 1000 | | 130 | 140 | | 140 | 150 | | 120 | 140 | | dB |
| INPUT CURRENT | | | | | | | | | | | |
| Input Bias Current | | | 0.5 | 1.5 | | 0.2 | 0.4 | | 0.5 | 2 | nA |
| Over Temperature | T = −40°C to +85°C | | | 2.0 | | | 1 | | | 3 | nA |
| Average TC | | | 1 | | | 1 | | | 3 | | pA/°C |
| Input Offset Current | | | 0.2 | 0.6 | | 0.1 | 0.4 | | 0.3 | 1 | nA |
| Over Temperature | T = −40°C to +85°C | | | 0.8 | | | 0.6 | | | 1.5 | nA |
| Average TC | | | 1 | | | 1 | | | 3 | | pA/°C |
| REFERENCE INPUT | | | | | | | | | | | |
| $R_{IN}$ | | | 20 | | | 20 | | | 20 | | kΩ |
| $I_{IN}$ | $V_{IN+}$, $V_{IN-}$, $V_{REF}$ = 0 | | 50 | 60 | | 50 | 60 | | 50 | 60 | µA |
| Voltage Range | | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | $-V_S$ | | $+V_S$ | V |
| Gain to Output | | | 1 ± 0.0001 | | | 1 ± 0.0001 | | | 1 ± 0.0001 | | V/V |
| POWER SUPPLY | | | | | | | | | | | |
| Operating Range | $V_S$ = ±2.3 V to ±18 V | ±2.3 | | ±18 | ±2.3 | | ±18 | ±2.3 | | ±18 | V |
| Quiescent Current | | | 0.9 | 1 | | 0.9 | 1 | | 0.9 | 1 | mA |
| Over Temperature | T = −40°C to +85°C | | 1 | 1.2 | | 1 | 1.2 | | 1 | 1.2 | mA |

| Parameter | Conditions | AR Grade | | | BR Grade | | | ARM Grade | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| DYNAMIC RESPONSE | | | | | | | | | | | |
| Small Signal −3 dB | | | | | | | | | | | |
| Bandwidth | | | | | | | | | | | |
| G = 1 | | | 825 | | | 825 | | | 825 | | kHz |
| G = 10 | | | 562 | | | 562 | | | 562 | | kHz |
| G = 100 | | | 100 | | | 100 | | | 100 | | kHz |
| G = 1000 | | | 14.7 | | | 14.7 | | | 14.7 | | kHz |
| Settling Time 0.01% | 10 V Step | | | | | | | | | | |
| G = 1 to 100 | | | 10 | | | 10 | | | 10 | | µs |
| G = 1000 | | | 80 | | | 80 | | | 80 | | µs |
| Settling Time 0.001% | 10 V Step | | | | | | | | | | |
| G = 1 to 100 | | | 13 | | | 13 | | | 13 | | µs |
| G = 1000 | | | 110 | | | 110 | | | 110 | | µs |
| Slew Rate | G = 1 | 1.5 | 2 | | 1.5 | 2 | | 1.5 | 2 | | V/µs |
| | G = 5–100 | 2 | 2.5 | | 2 | 2.5 | | 2 | 2.5 | | V/µs |
| GAIN | G = 1 + (49.4 kΩ/$R_G$) | | | | | | | | | | |
| Gain Range | | 1 | | 1000 | 1 | | 1000 | 1 | | 1000 | V/V |
| Gain Error | $V_{OUT}$ ±10 V | | | | | | | | | | |
| G = 1 | | | | 0.03 | | | 0.02 | | | 0.1 | % |
| G = 10 | | | | 0.3 | | | 0.15 | | | 0.3 | % |
| G = 100 | | | | 0.3 | | | 0.15 | | | 0.3 | % |
| G = 1000 | | | | 0.3 | | | 0.15 | | | 0.3 | % |
| Gain Nonlinearity | $V_{OUT}$ = −10 V to +10 V | | | | | | | | | | |
| G = 1 to 10 | $R_L$ = 10 kΩ | | 3 | 10 | | 3 | 10 | | 5 | 15 | ppm |
| G = 100 | $R_L$ = 10 kΩ | | 5 | 15 | | 5 | 15 | | 7 | 20 | ppm |
| G = 1000 | $R_L$ = 10 kΩ | | 10 | 40 | | 10 | 40 | | 10 | 50 | ppm |
| G = 1 to 100 | $R_L$ = 2 kΩ | | 10 | 95 | | 10 | 95 | | 15 | 100 | ppm |
| Gain vs. Temperature | | | | | | | | | | | |
| G = 1 | | | 3 | 10 | | 2 | 5 | | 3 | 10 | ppm/°C |
| G > 1[2] | | | | −50 | | | −50 | | | −50 | ppm/°C |
| INPUT | | | | | | | | | | | |
| Input Impedance | | | | | | | | | | | |
| Differential | | | 100‖2 | | | 100‖2 | | | 100‖2 | | GΩ‖pF |
| Common Mode | | | 100‖2 | | | 100‖2 | | | 100‖2 | | GΩ‖pF |
| Input Operating Voltage Range[3] | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.9 | | $+V_S$ − 1.1 | $-V_S$ + 1.9 | | $+V_S$ − 1.1 | $-V_S$ + 1.9 | | $+V_S$ − 1.1 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | V |
| Input Operating Voltage Range | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.9 | | $+V_S$ − 1.2 | $-V_S$ + 1.9 | | $+V_S$ − 1.2 | $-V_S$ + 1.9 | | $+V_S$ − 1.2 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | $-V_S$ + 2.0 | | $+V_S$ − 1.2 | V |
| OUTPUT | $R_L$ = 10 kΩ | | | | | | | | | | |
| Output Swing | $V_S$ = ±2.3 V to ±5 V | $-V_S$ + 1.1 | | $+V_S$ − 1.2 | $-V_S$ + 1.1 | | $+V_S$ − 1.2 | $-V_S$ + 1.1 | | $+V_S$ − 1.2 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 1.4 | | +Vs − 1.3 | $-V_S$ + 1.4 | | +Vs − 1.3 | $-V_S$ + 1.4 | | +Vs − 1.3 | V |
| Output Swing | $V_S$ = ±5 V to ±18 V | $-V_S$ + 1.2 | | $+V_S$ − 1.4 | $-V_S$ + 1.2 | | $+V_S$ − 1.4 | $-V_S$ + 1.2 | | $+V_S$ − 1.4 | V |
| Over Temperature | T = −40°C to +85°C | $-V_S$ + 1.6 | | $+V_S$ − 1.5 | $-V_S$ + 1.6 | | $+V_S$ − 1.5 | $-V_S$ + 1.6 | | $+V_S$ − 1.5 | V |
| Short-Circuit Current | | | 18 | | | 18 | | | 18 | | mA |
| TEMPERATURE RANGE | | | | | | | | | | | |
| Specified Performance | | −40 | | +85 | −40 | | +85 | −40 | | +85 | °C |
| Operational[4] | | −40 | | +125 | −40 | | +125 | −40 | | +125 | °C |

[1] Total RTI $V_{OS}$ = ($V_{OSI}$) + ($V_{OSO}$/G).
[2] Does not include the effects of external resistor $R_G$.
[3] One input grounded. G = 1.
[4] See Typical Performance Curves for expected operation between 85°C to 125°C.

# ABSOLUTE MAXIMUM RATINGS

**Table 2. AD8221 Absolute Maximum Ratings**

| Parameter | Rating |
|---|---|
| Supply Voltage | ±18 V |
| Internal Power Dissipation | 200 mW |
| Output Short Circuit Current | Indefinite |
| Input Voltage (Common-Mode) | $\pm V_S$ |
| Differential Input Voltage | ±Vs |
| Storage Temperature | –65°C to +150°C |
| Operational* Temperature Range | –40°C to +125°C |

*Temperature range for specified performance is –40°C to +85°C. See Typical Performance Curves for expected operation from +85°C to +125°C.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Specification is for device in free air:

SOIC $\theta_{JA}$ (4 Layer JEDEC Board) = 121°C/W.
MSOP $\theta_{JA}$ (4 Layer JEDEC Board) = 135°C/W.

## ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

**(@+25°C, $V_S$ = ±15 V, $R_L$ = 10 kΩ, unless otherwise noted.)**

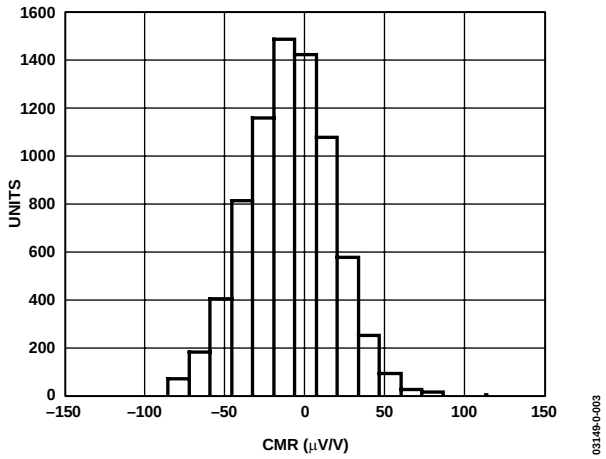


*Figure 3. Typical Distribution for CMR (G = 1)*

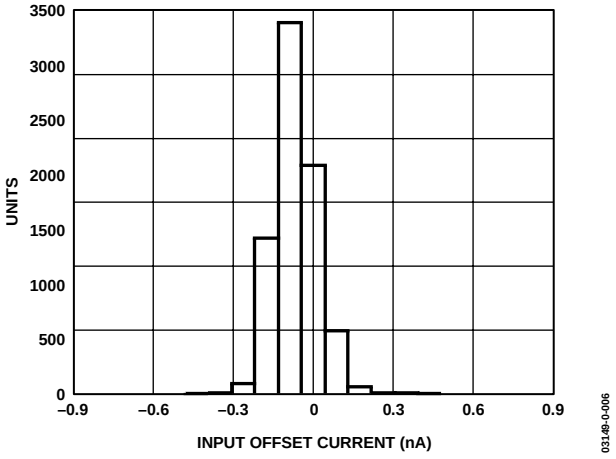


*Figure 6. Typical Distribution of Input Offset Current*

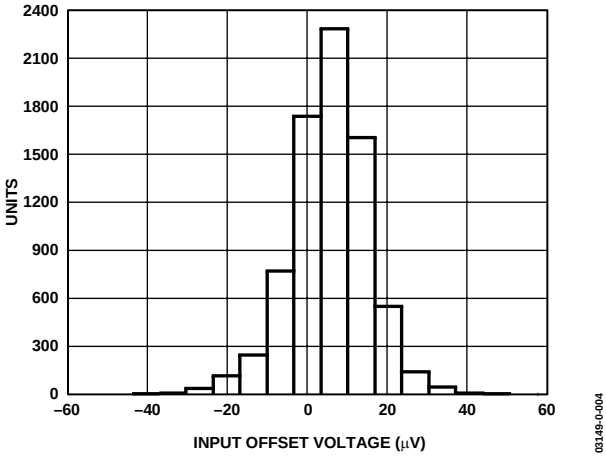


*Figure 4. Typical Distribution of Input Offset Voltage*

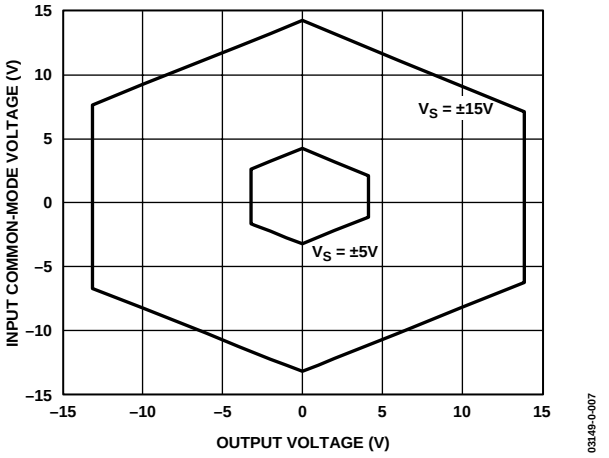


*Figure 7. Input Common-Mode Range vs. Output Voltage, G = 1*

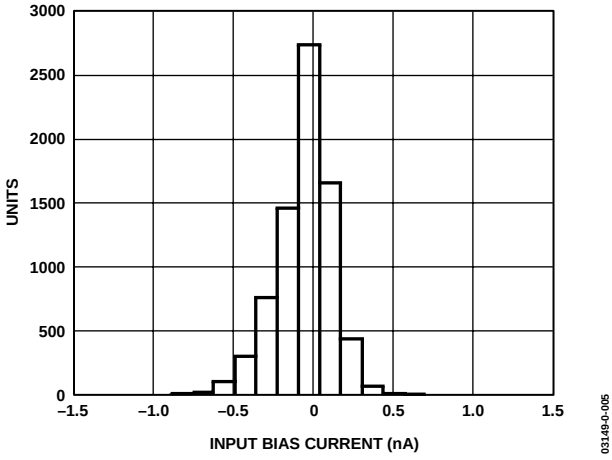


*Figure 5. Typical Distribution of Input Bias Current*

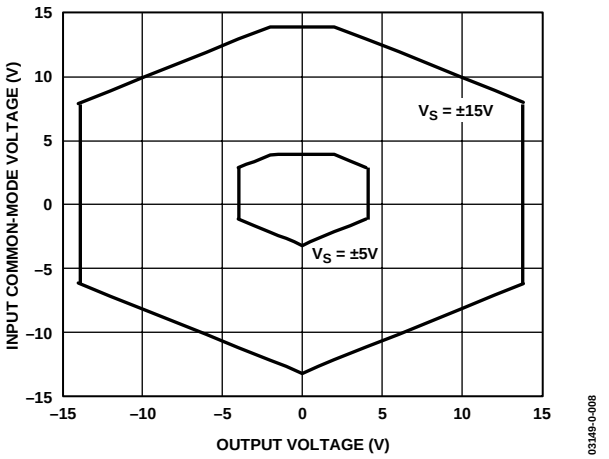


*Figure 8. Input Common-Mode Range vs. Output Voltage, G = 100*

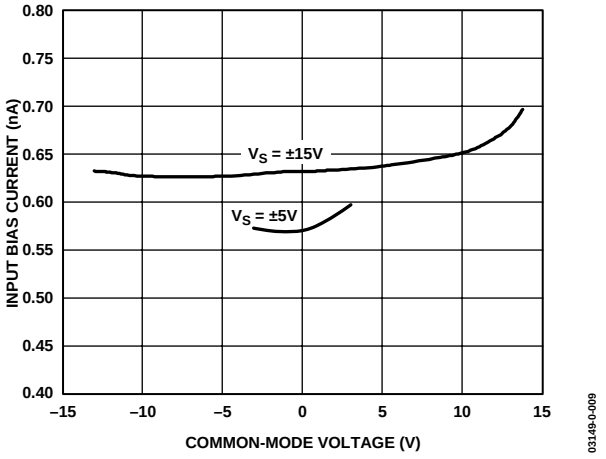


Figure 9. $I_{BIAS}$ vs. CMV

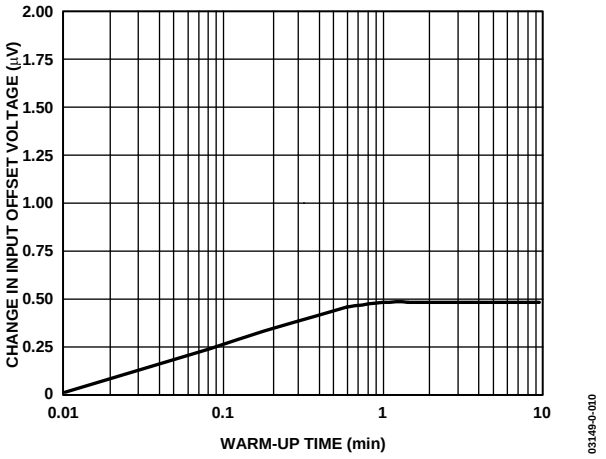


Figure 10. Change in Input Offset Voltage vs. Warm-Up Time

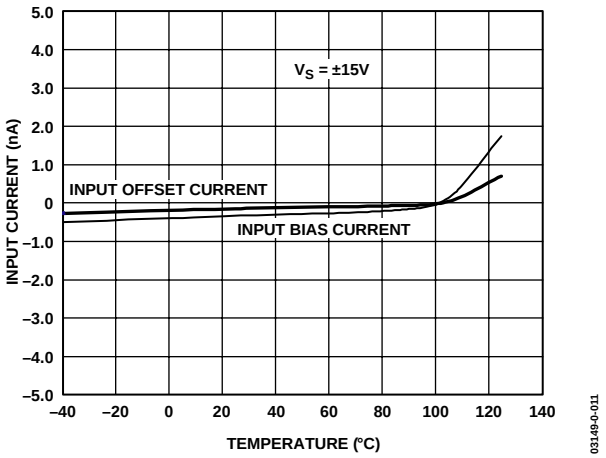


Figure 11. Input Bias Current and Offset Current vs. Temperature

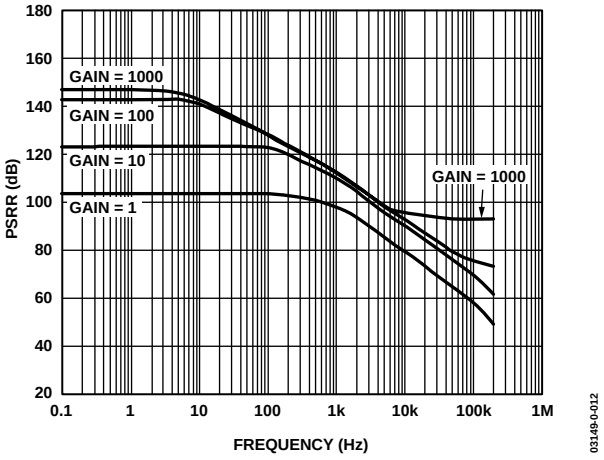


Figure 12. Positive PSRR vs. Frequency, RTI (G = 1 to 1000)

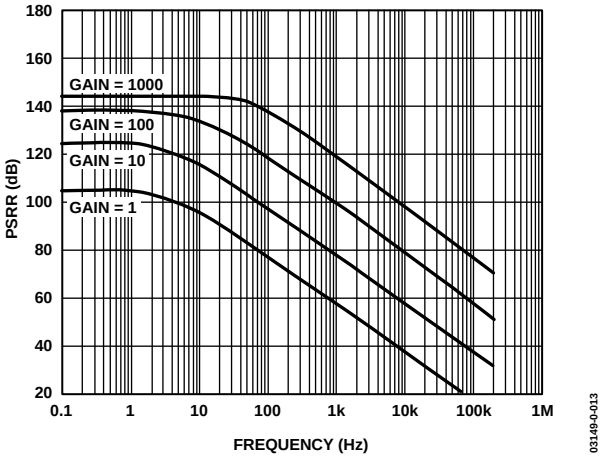


Figure 13. Negative PSRR vs. Frequency, RTI (G = 1 to 1000)

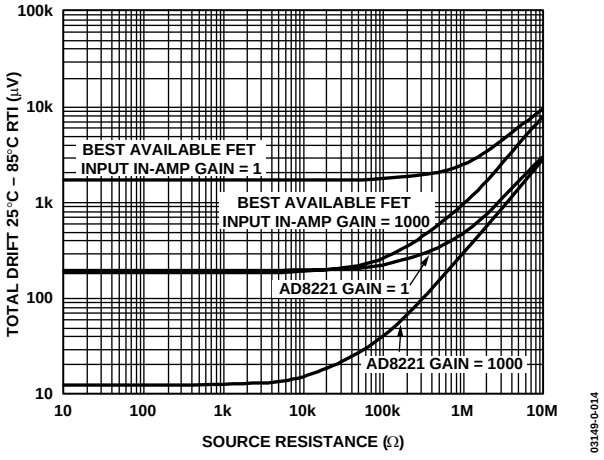


Figure 14. Total Drift vs. Source Resistance

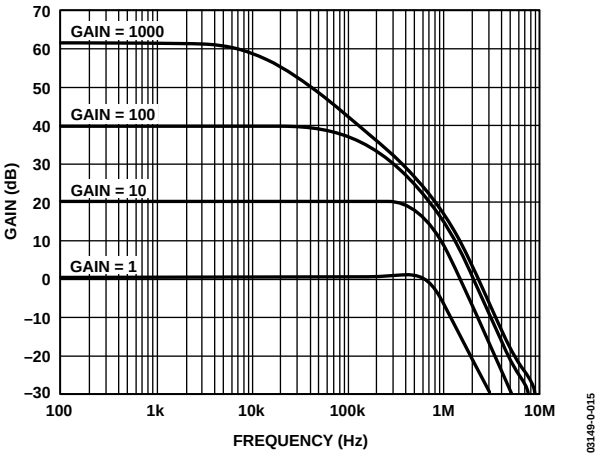


Figure 15. Gain vs. Frequency

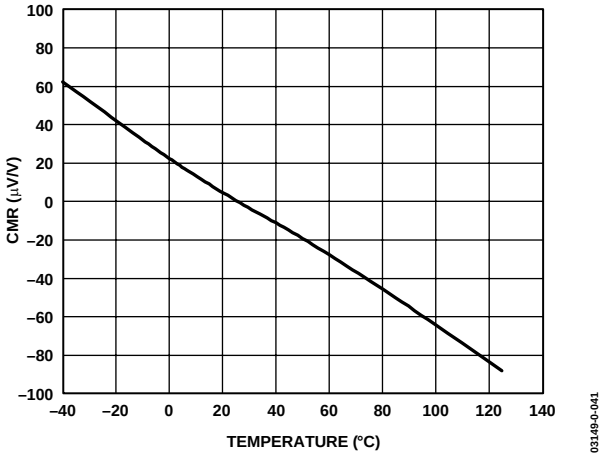


Figure 18. CMR vs. Temperature

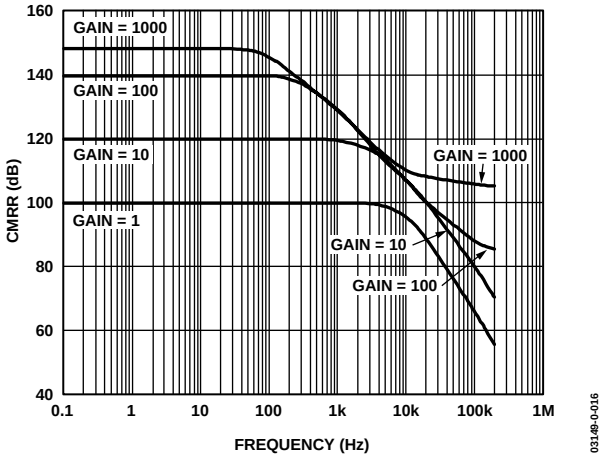


Figure 16. CMRR vs. Frequency, RTI

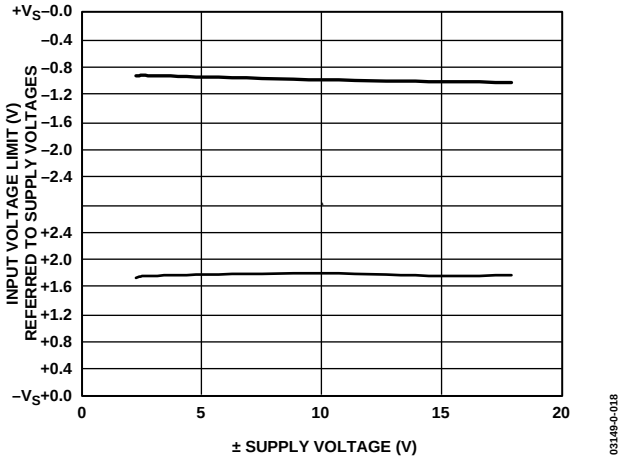


Figure 19. Input Voltage Limit vs. Supply Voltage, G = 1

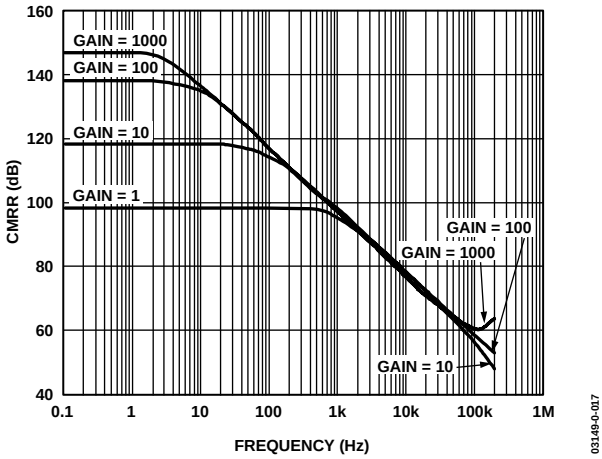


Figure 17. CMRR vs. Frequency, RTI, 1 kΩ Source Imbalance

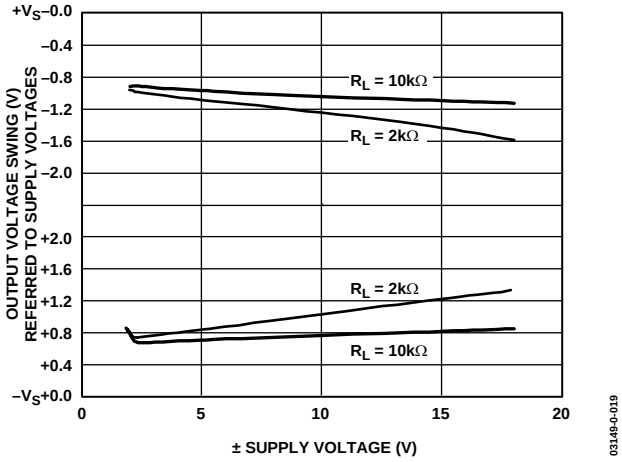


Figure 20. Output Voltage Swing vs. Supply Voltage, G = 1

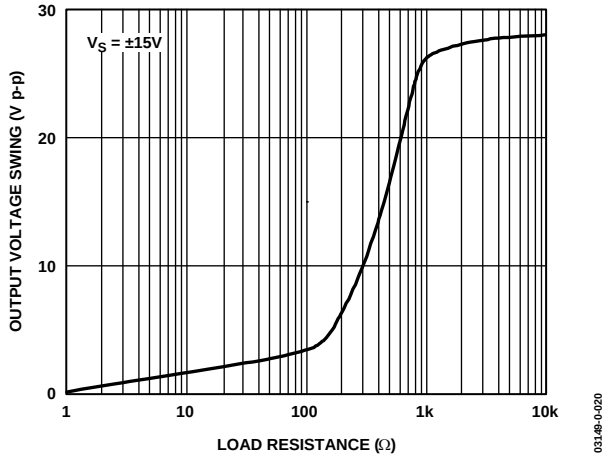


Figure 21. Output Voltage Swing vs. Load Resistance

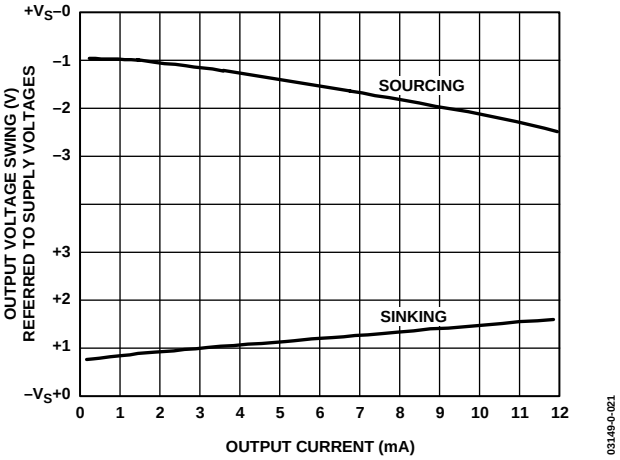


Figure 22. Output Voltage Swing vs. Output Current, G = 1

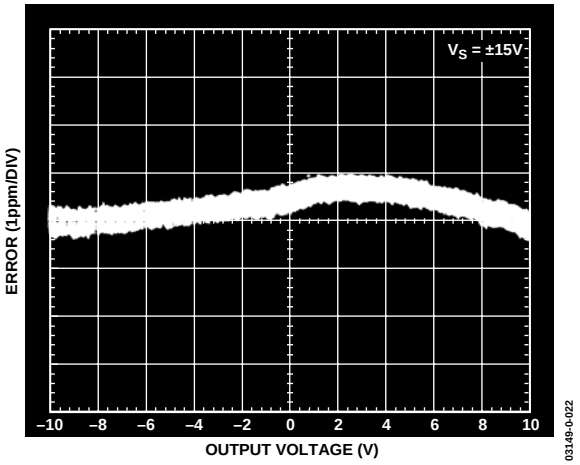


Figure 23. Gain Nonlinearity, G = 1, $R_L$ = 10 kΩ

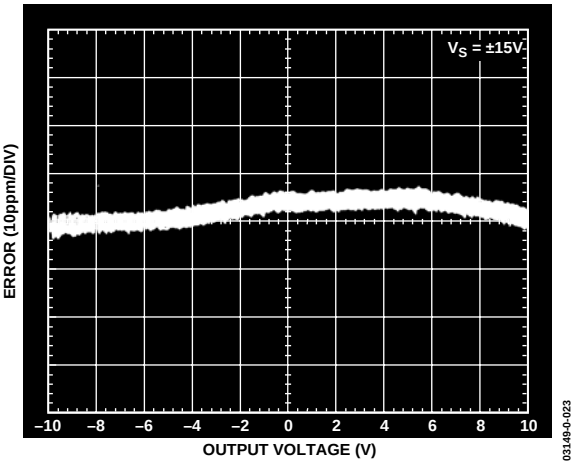


Figure 24. Gain Nonlinearity, G = 100, $R_L$ = 10 kΩ

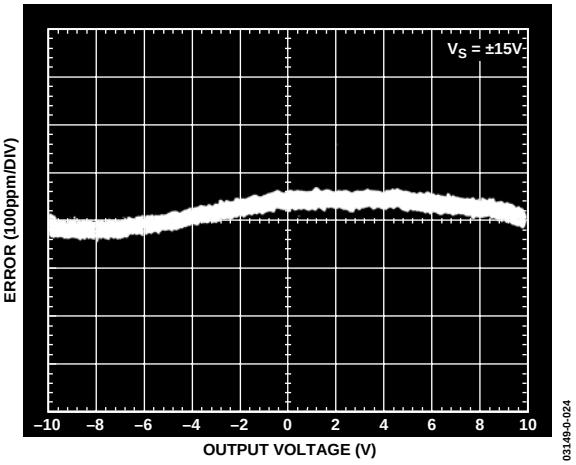


Figure 25. Gain Nonlinearity, G = 1000, $R_L$ = 10 kΩ

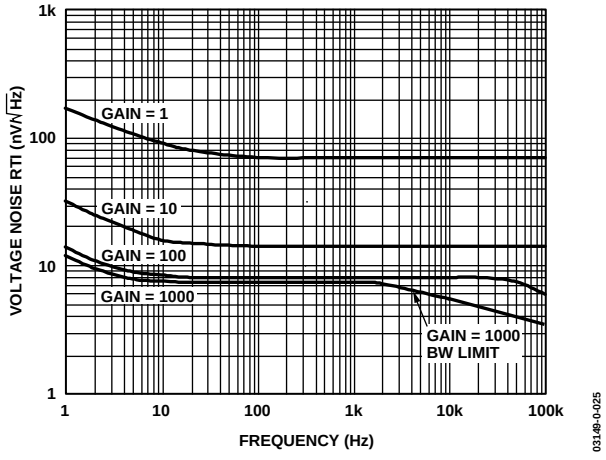


Figure 26. Voltage Noise Spectral Density vs. Frequency (G = 1 to 1000)

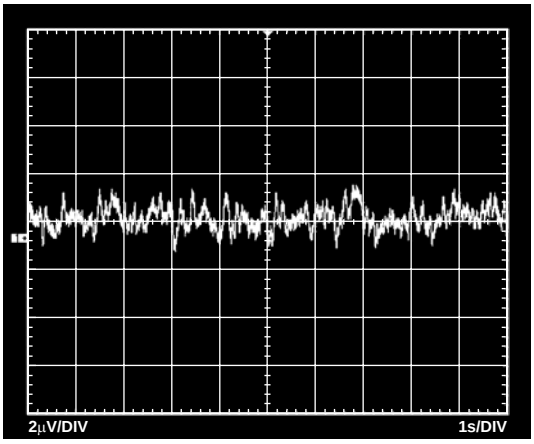


Figure 27. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1)

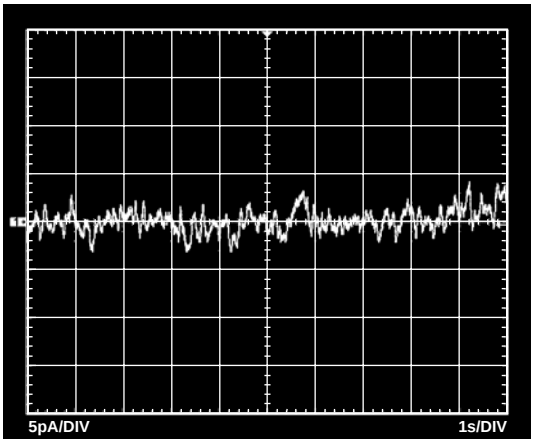


Figure 30. 0.1 Hz to 10 Hz Current Noise

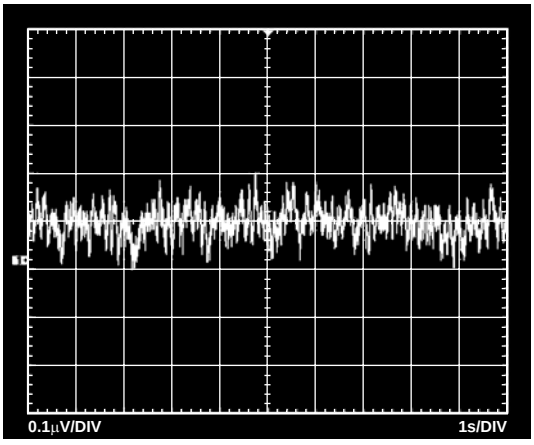


Figure 28. 0.1 Hz to 10 Hz RTI Voltage Noise (G = 1000)

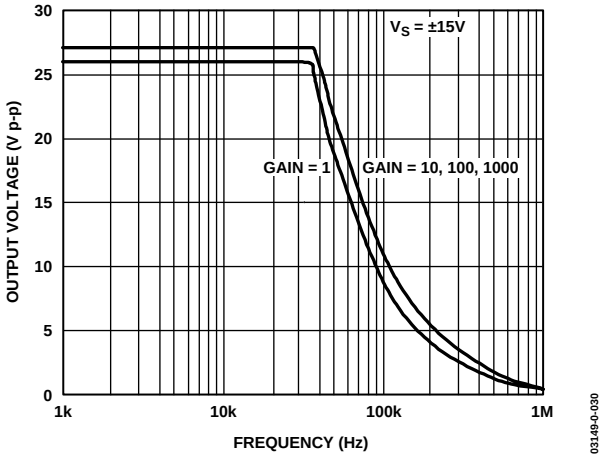


Figure 31. Large Signal Frequency Response

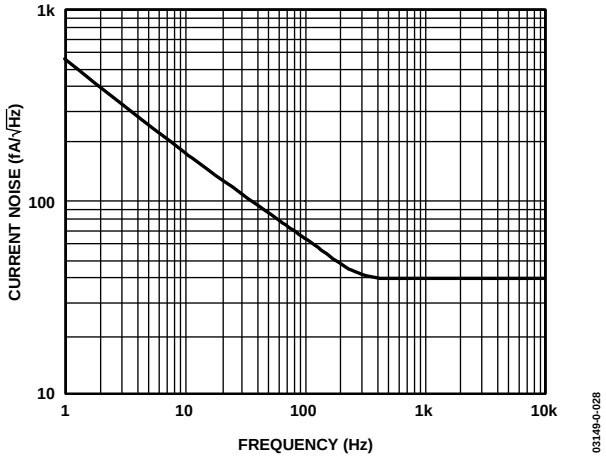


Figure 29. Current Noise Spectral Density vs. Frequency

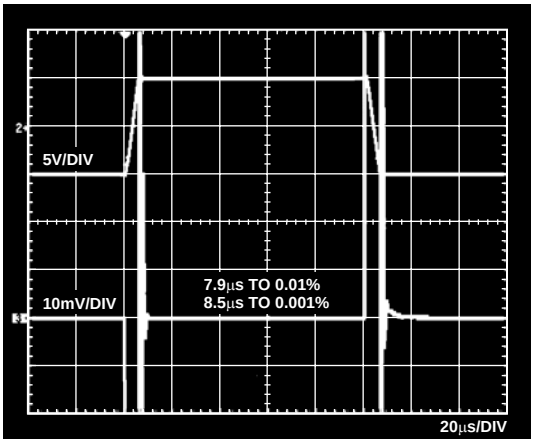


Figure 32. Large Signal Pulse Response and Settling Time (G = 1), 0.002%/div

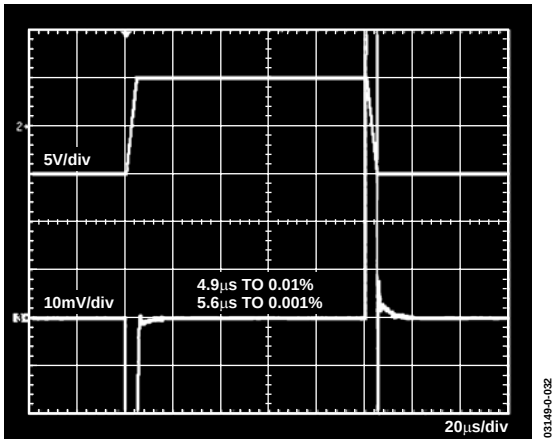


Figure 33. Large Signal Pulse Response and Settling Time (G = 10), 0.002%/div

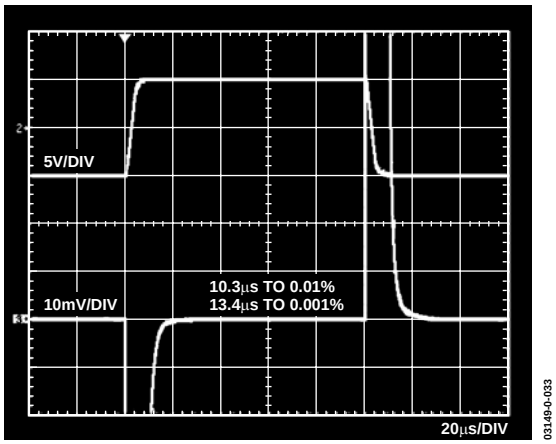


Figure 34. Large Signal Pulse Response and Settling Time (G = 100), 0.002%/div

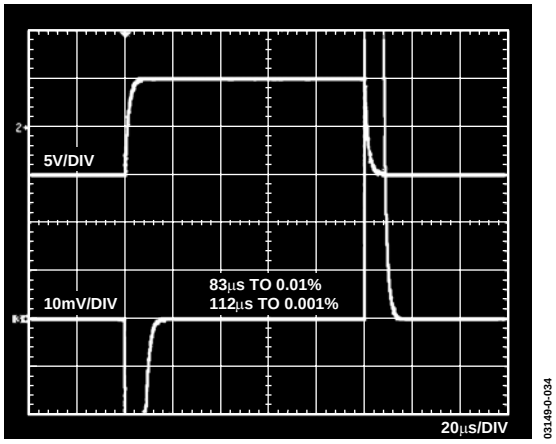


Figure 35. Large Signal Pulse Response and Settling Time (G = 1000), 0.002%/div

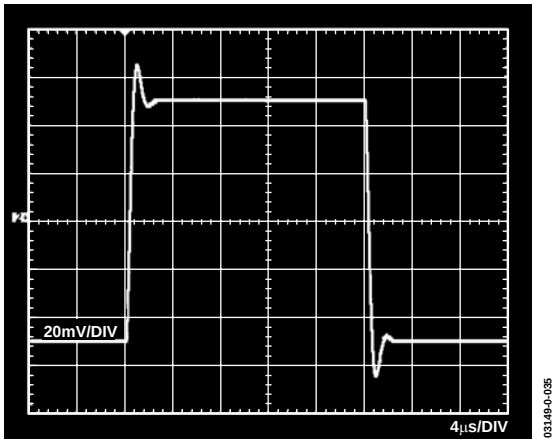


Figure 36. Small Signal Response, G = 1, $R_L$ = 2 kΩ, $C_L$ = 100 pF

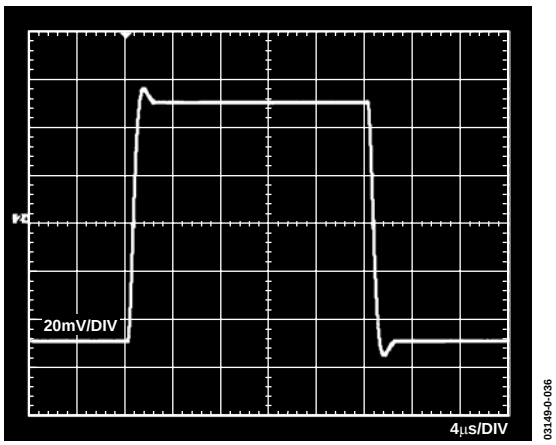


Figure 37. Small Signal Response, G = 10, $R_L$ = 2 kΩ, $C_L$ = 100 pF

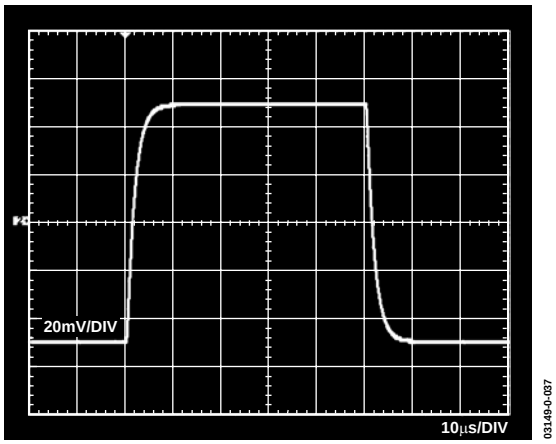


Figure 38. Small Signal Response, G = 100, $R_L$ = 2 kΩ, $C_L$ = 100 pF

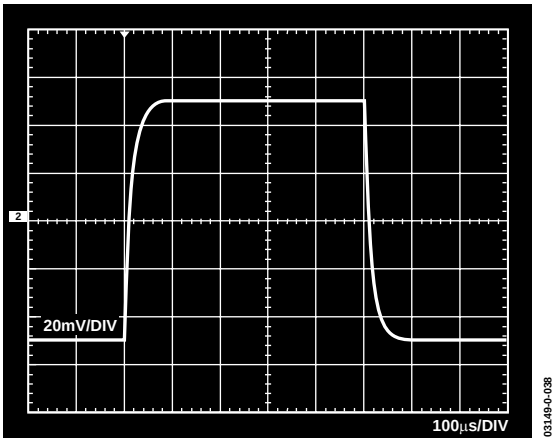


Figure 39. Small Signal Response, G = 1000, $R_L$ = 2 kΩ, $C_L$ = 100 pF

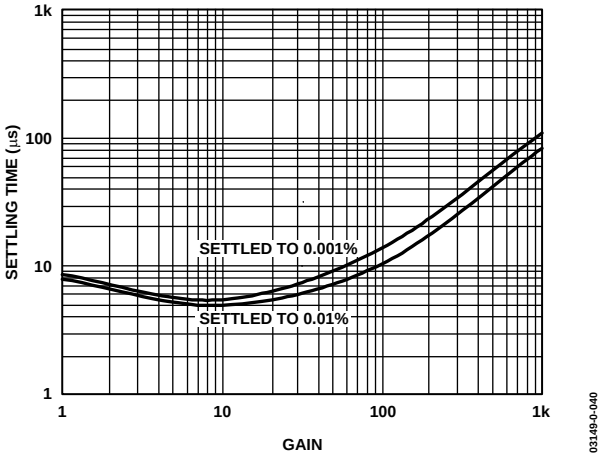


Figure 41. Settling Time vs. Gain for a 10 V Step

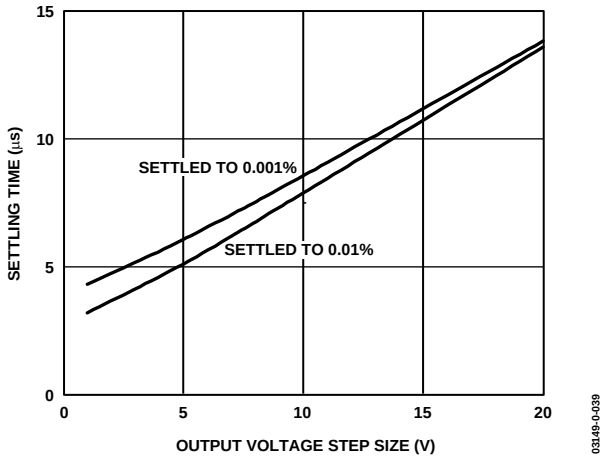


Figure 40. Settling Time vs. Step Size (G = 1)

# THEORY OF OPERATION

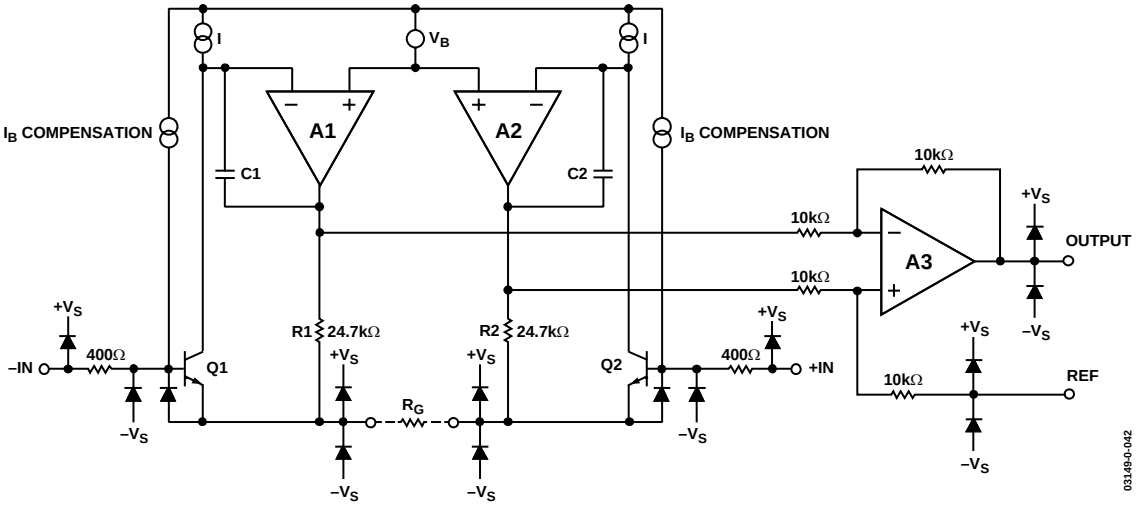


*Figure 42. Simplified Schematic*

The AD8221 is a monolithic instrumentation amplifier based on the classic 3-op amp topology. Input transistors Q1 and Q2 are biased at a fixed current, so that any differential input signal will force the output voltages of A1 and A2 to change accordingly. A signal applied to the input creates a current through $R_G$, R1, and R2, such that the outputs of A1 and A2 deliver the correct voltage. Topologically, Q1, A1, R1 and Q2, A2, R2 can be viewed as precision current feedback amplifiers. The amplified differential and common-mode signals are applied to a difference amplifier that rejects the common-mode voltage but amplifies the differential voltage. The difference amplifier employs innovations that result in low output offset voltage as well as low output offset voltage drift. Laser-trimmed resistors allow for a highly accurate in-amp with gain error typically less than 20 ppm and CMRR that exceeds 90 dB (G = 1).

Using superbeta input transistors and an $I_B$ compensation scheme, the AD8221 offers extremely high input impedance, low $I_B$, low $I_B$ drift, low $I_{OS}$, low input bias current noise, and extremely low voltage noise of 8 nV/√Hz.

The transfer function of the AD8221 is

$$G = 1 + \frac{49.4\text{k}\Omega}{R_G}$$

Users can easily and accurately set the gain using a single, standard resistor.

Since the input amplifiers employ a current feedback architecture, the AD8221's gain-bandwidth product increases with gain, resulting in a system that does not suffer from the expected bandwidth loss of voltage feedback architectures at higher gains.

In order to maintain precision even at low input levels, special attention was given to the AD8221's design and layout, resulting in an in-amp whose performance satisfies the most demanding applications.

A unique pinout enables the AD8221 to meet a CMRR specification of 80 dB at 10 kHz (G = 1) and 110 dB at 1 kHz (G = 1000). The balanced pinout, shown in Figure 43, reduces the parasitics that had, in the past, adversely affected CMRR performance. In addition, the new pinout simplifies board layout because associated traces are grouped together. For example, the gain setting resistor pins are adjacent to the inputs, and the reference pin is next to the output.

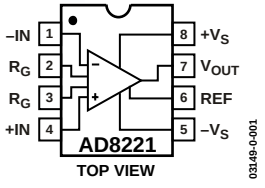


*Figure 43. Pinout Diagram*

## GAIN SELECTION

Placing a resistor across the $R_G$ terminals will set the AD8221's gain, which may be calculated by referring to Table 3 or by using the gain equation

$$R_G = \frac{49.4\text{k}\Omega}{G-1}$$

**Table 3. Gains Achieved Using 1% Resistors**

| 1% Std Table Value of $R_G$ (Ω) | Calculated Gain |
|---|---|
| 49.9 k | 1.990 |
| 12.4 k | 4.984 |
| 5.49 k | 9.998 |
| 2.61 k | 19.93 |
| 1.00 k | 50.40 |
| 499 | 100.0 |
| 249 | 199.4 |
| 100 | 495.0 |
| 49.9 | 991.0 |

The AD8221 defaults to G = 1 when no gain resistor is used. Gain accuracy is determined by the absolute tolerance of $R_G$. The TC of the external gain resistor will increase the gain drift of the instrumentation amplifier. Gain error and gain drift are kept to a minimum when the gain resistor is not used.

## LAYOUT

Careful board layout maximizes system performance. Traces from the gain setting resistor to the $R_G$ pins should be kept as short as possible to minimize parasitic inductance. To ensure the most accurate output, the trace from the REF pin should either be connected to the AD8221's local ground as shown in Figure 47, or connected to a voltage that is referenced to the AD8221's local ground.

### *Common-Mode Rejection*

One benefit of the AD8221's high CMRR over frequency is that it has greater immunity to disturbances such as line noise and its associated harmonics than do typical in-amps. These, typically, have CMRR fall-off at 200 Hz; common-mode filters are often used to compensate for this shortcoming. The AD8221 is able to reject CMRR over a greater frequency range, reducing the need for filtering.

A well implemented layout helps to maintain the AD8221's high CMRR over frequency. Input source impedance and capacitance should be closely matched. In addition, source resistance and capacitance should be placed as close to the inputs as permissible.

### *Grounding*

The AD8221's output voltage is developed with respect to the potential on the reference terminal. Care should be taken to tie REF to the appropriate "local ground."

In mixed-signal environments, low level analog signals need to be isolated from the noisy digital environment. Many ADCs have separate analog and digital ground pins. Although it is convenient to tie both grounds to a single ground plane, the current traveling through the ground wires and PC board may cause hundreds of millivolts of error. Therefore, separate analog and digital ground returns should be used to minimize the current flow from sensitive points to the system ground. An example layout is shown in Figure 44 and Figure 45.

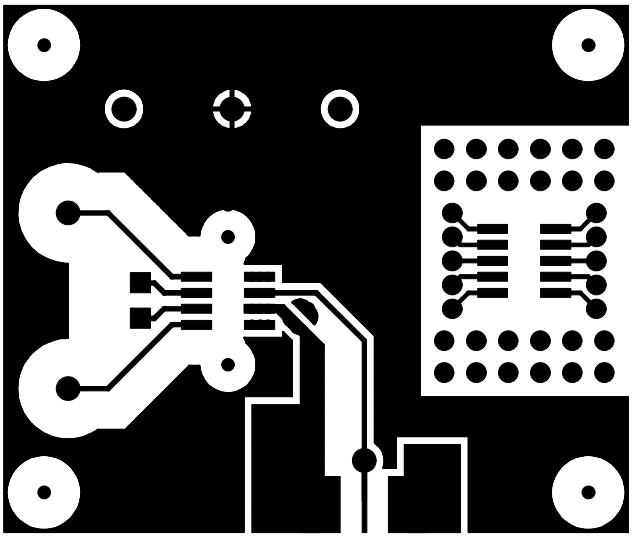

*Figure 44.Top Layer of the AD8221-EVAL*

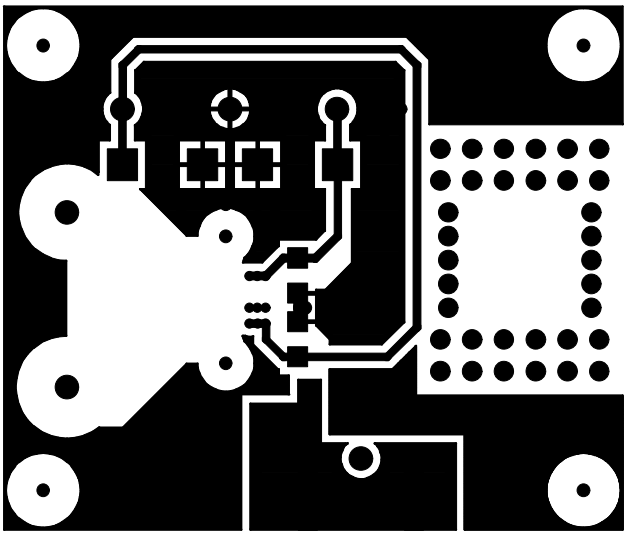

*Figure 45.Bottom Layer of the AD8221-EVAL*

## REFERENCE TERMINAL

As shown in Figure 42, the reference terminal, REF, is at one end of a 10 kΩ resistor. The instrumentation amplifier's output is referenced to the voltage on the REF terminal; this is useful when the output signal needs to be offset to a precise midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8221 can interface with an ADC. The allowable reference voltage range is a function of the gain, input and supply voltage. The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

For best performance, source impedance to the REF terminal should be kept low, since parasitic resistance can adversely affect CMRR and gain accuracy.

## POWER SUPPLY REGULATION AND BYPASSING

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins may adversely affect performance. Bypass capacitors should be used to decouple the amplifier.

A 0.1 μF capacitor should be placed close to each supply pin. As shown in Figure 47, a 10 μF tantalum capacitor may be used further away from the part. In most cases, it may be shared by other precision integrated circuits.

*Figure 46*

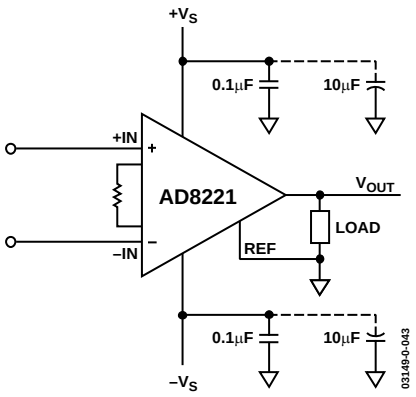


*Figure 47. Supply Decoupling,. REF and Output Referred to Local Ground*

## INPUT BIAS CURRENT RETURN PATH

The AD8221's input bias current must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 48.

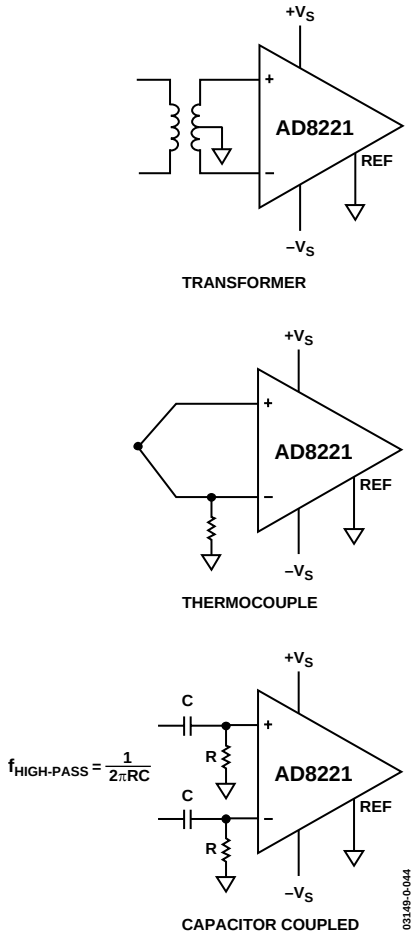


*Figure 48. Creating an $I_{BIAS}$ Path*

## INPUT PROTECTION

All terminals of the AD8221 are protected against ESD[1]. In addition, the input structure allows for dc overload conditions below the negative supply, –Vs. The internal 400 Ω resistors limit current in the event of a negative fault condition. However, in the case of a dc overload voltage above the positive supply, +Vs, a large current would flow directly through the ESD diode to the positive rail. Therefore, an external resistor should be used in series with the input to limit current for voltages above +Vs. In either scenario, the AD8221 can safely handle a continuous 6 mA current, $I = V_{IN}/R_{EXT}$ for positive overvoltage and $I = V_{IN}/(400\ \Omega + R_{EXT})$ for negative overvoltage.

For applications where the AD8221 encounters extreme overload voltages, as in cardiac defibrillators, external series resistors and low leakage diode clamps such as BAV199Ls, FJH1100s, or SP720s should be used.

[1] 1 kV—Human Body Model.

## RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance may appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass R-C network placed at the input of the instrumentation amplifier, as shown in Figure 49. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{Diff} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

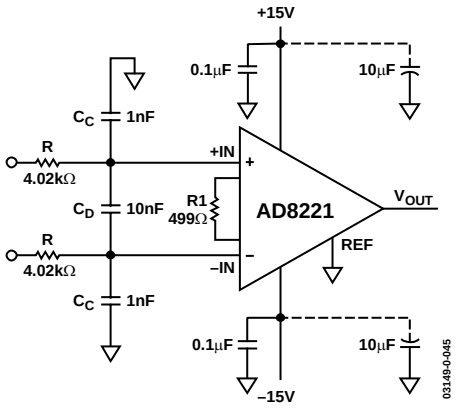


*Figure 49. RFI Suppression*

$C_D$ affects the difference signal and $C_C$ affects the common-mode signal. Values of R and $C_C$ should be chosen to minimize RFI. Mismatch between the R × $C_C$ at the positive input and the R × $C_C$ at negative input will degrade the AD8221's CMRR. By using a value of $C_D$ one magnitude larger than $C_C$, the effect of the mismatch is reduced, and hence, performance is improved.

## PRECISION STRAIN GAGE

The AD8221's low offset and high CMRR over frequency make it an excellent candidate for bridge measurements. As shown in Figure 50, the bridge can be directly connected to the inputs of the amplifier.

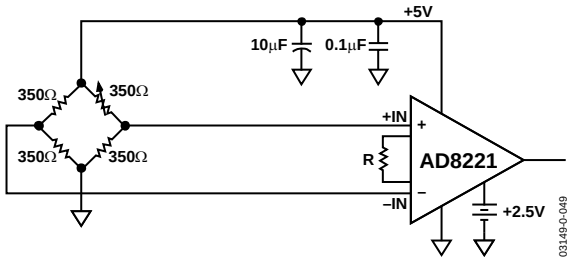


*Figure 50. Precision Strain Gage*

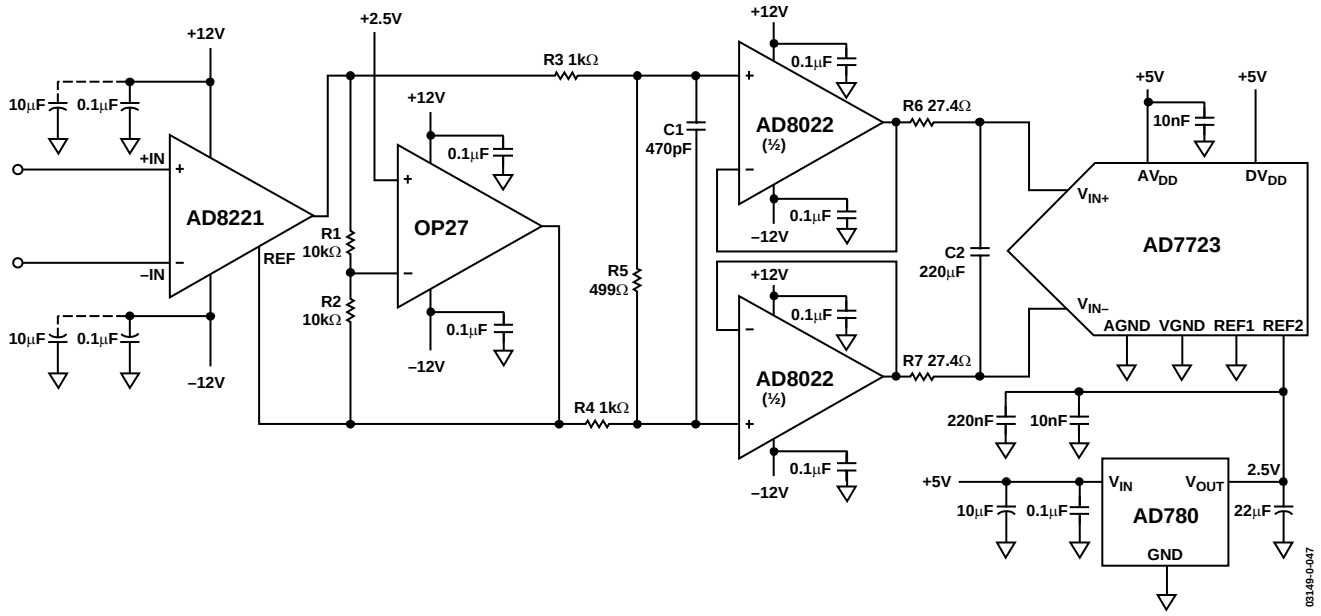


*Figure 51. Interfacing to a Differential Input ADC*

## CONDITIONING ±10 V SIGNALS FOR A +5 V DIFFERENTIAL INPUT ADC

There is a need in many applications to condition ±10 V signals. However, many of today's ADCs and digital ICs operate on much lower, single-supply voltages. Furthermore, new ADCs have differential inputs because they provide better common-mode rejection, noise immunity, and performance at low supply voltages. Interfacing a ±10 V, single-ended instrumentation amplifier to a +5 V, differential ADC may be a challenge. Interfacing the in-amp to the ADC requires attenuation and a level shift. A solution is shown in Figure 51.

In this topology, an OP27 sets the AD8221's reference voltage. The in-amp's output signal is taken across the OUT pin and the REF pin. Two 1 kΩ resistors and a 499 Ω resistor attenuate the ±10 V signal to +4 V. An optional capacitor, C1, may serve as an ant aliasing filter. An AD8022 is used to drive the ADC.

This topology has five benefits. In addition to level-shifting and attenuation, very little noise is contributed to the system. Noise from R1 and R2 is common to both of the ADC's inputs and is easily rejected. R5 adds a third of the dominant noise and therefore makes a negligible contribution to the noise of the system. The attenuator divides the noise from R3 and R4. Likewise, its noise contribution is negligible. The fourth benefit of this interface circuit is that the AD8221's acquisition time is reduced by a factor of 2. With the help of the OP27, the AD8221 only needs to deliver one-half of the full swing; therefore, signals can settle more quickly. Lastly, the AD8022 settles quickly, which is helpful because the shorter the settling time, the more bits that can be resolved when the ADC acquires data. This configuration provides attenuation, a level-shift, and a convenient interface with a differential input ADC while maintaining performance.

## AC-COUPLED INSTRUMENTATION AMPLIFIER

Measuring small signals that are in the amplifier's noise or offset can be a challenge. Figure 52 shows a circuit that can improve the resolution of small ac signals. The large gain reduces the referred input noise of the amplifier to 8 nV/√Hz. Thus, smaller signals can be measured since the noise floor is lower. DC offsets that would have been gained by 100 are eliminated from the AD8221's output by the integrator feedback network.

At low frequencies, the OP1177 forces the AD8221's output to 0 V. Once a signal exceeds $f_{HIGH\text{-}PASS}$, the AD8221 outputs the amplified input signal.

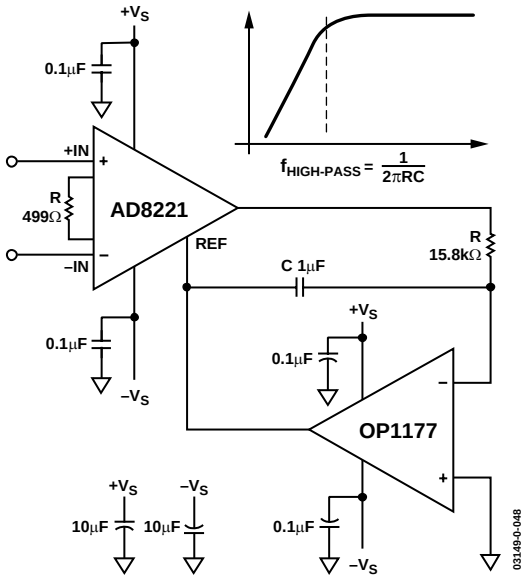


*Figure 52. AC-Coupled Circuit*

# OUTLINE DIMENSIONS

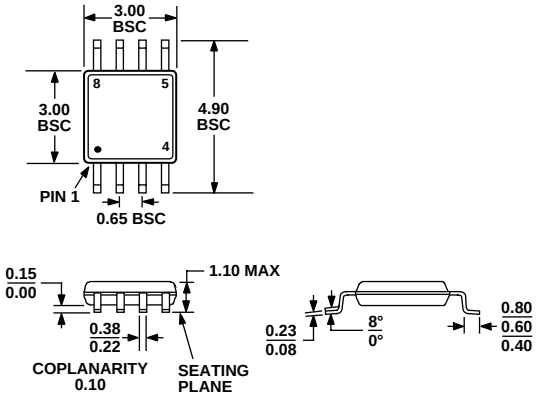


*Figure 53. 8-Lead Mini Small Outline Package [MSOP] (RM-8)*
*Dimensions shown in millimeters*

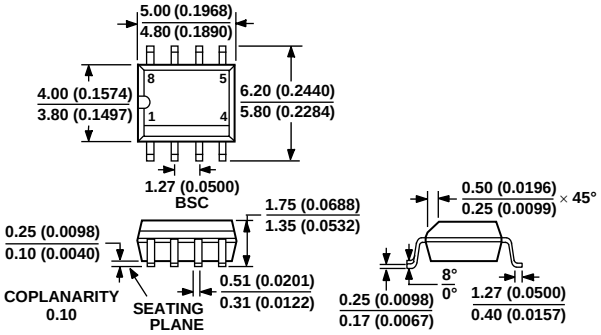


*Figure 54. 8-Lead Shrink Small Outline Package [SOIC] (R-8)*

## ORDERING GUIDE

| Model | Temperature Range for Specified Performance | Operational[1] Temperature Range | Package Description | Package Option | Branding |
|---|---|---|---|---|---|
| AD8221AR | –40°C to +85°C | –40°C to 125°C | 8-Lead SOIC | R-8 | |
| AD8221AR-REEL | –40°C to +85°C | –40°C to 125°C | 13" Tape and Reel | R-8 | |
| AD8221AR-REEL7 | –40°C to +85°C | –40°C to 125°C | 7" Tape and Reel | R-8 | |
| AD8221ARM | –40°C to +85°C | –40°C to 125°C | 8-Lead MSOP | RM-8 | JLA |
| AD8221ARM-REEL | –40°C to +85°C | –40°C to 125°C | 13" Tape and Reel | RM-8 | JLA |
| AD8221ARM-REEL7 | –40°C to +85°C | –40°C to 125°C | 7" Tape and Reel | RM-8 | JLA |
| AD8221BR | –40°C to +85°C | –40°C to 125°C | 8-Lead SOIC | R-8 | |
| AD8221BR-REEL | –40°C to +85°C | –40°C to 125°C | 13" Tape and Reel | R-8 | |
| AD8221BR-REEL7 | –40°C to +85°C | –40°C to 125°C | 7" Tape and Reel | R-8 | |
| AD8221-EVAL | | | Evaluation Board | | |

[1] See Typical Performance Curves for expected operation from 85°C to 125°C.

## NOTES

## NOTES


C03149–0–11/03(A)