Zero Drift, Digitally Programmable Instrumentation Amplifier

AD8231

FEATURES

- Digitally/pin programmable gain
  - G = 1, 2, 4, 8, 16, 32, 64, 128
- Specified from −40°C to +125°C
  - 50 nV/°C maximum input offset drift
  - 10 ppm/°C maximum gain drift
- Excellent dc performance
  - 80 dB minimum CMR, G = 1
  - 15 µV maximum input offset voltage
  - 500 pA maximum bias current
  - 0.7 µV p-p noise (0.1 Hz to 10 Hz)
- Good ac performance
  - 2.7 MHz bandwidth, G = 1
  - 1.1 V/µs slew rate
- Rail-to-rail input and output
- Shutdown/multiplex
- Extra op amp
- Single supply range: 3 V to 6 V
- Dual supply range: ±1.5 V to ±3 V

APPLICATIONS

- Pressure and strain transducers
- Thermocouples and RTDs
- Programmable instrumentation
- Industrial controls
- Weigh scales

GENERAL DESCRIPTION

The AD8231 is a low drift, rail-to-rail, instrumentation amplifier with software programmable gains of 1, 2, 4, 8, 16, 32, 64, or 128. The gains are programmed via digital logic or pin strapping.

The AD8231 is ideal for applications that require precision performance over a wide temperature range, such as industrial temperature sensing and data logging. Because the gain setting resistors are internal, maximum gain drift is only 10 ppm/°C. Because of the auto-zero input stage, maximum input offset is 15 µV and maximum input offset drift is just 50 nV/°C. CMRR is also guaranteed over temperature at 80 dB for G = 1, increasing to 110 dB at higher gains.

FUNCTIONAL BLOCK DIAGRAM

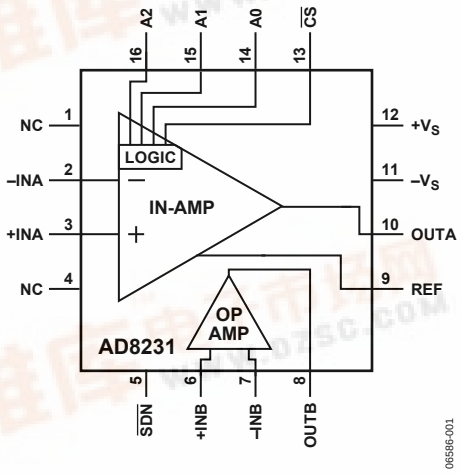

Figure 1.

Table 1. Instrumentation/Difference Amplifiers by Category

High Performance	Low Cost	High Voltage	Mil Grade	Low Power	Digital Gain
AD8221	AD623[1]	AD628	AD620	AD627[1]	AD8231[1]
AD8220[1]	AD8553[1]	AD629	AD621		AD8250
AD8222			AD524		AD8251
AD8224[1]			AD526		AD8555[1]
			AD624		AD8556[1]
					AD8557[1]

[1] Rail-to-rail output.

The AD8231 also includes an uncommitted op amp that can be used for additional gain, differential signal driving or filtering. Like the in-amp, the op amp has an auto-zero architecture, rail-to-rail input, and rail-to-rail output.

The AD8231 includes a shutdown feature that reduces current to a maximum of 1 µA. In shutdown, both amplifiers also have a high output impedance. This allows easy multiplexing of multiple amplifiers without additional switches.

The AD8231 is specified over the extended industrial temperature range of −40°C to +125°C. It is available in a 4 mm × 4 mm 16-lead LFCSP (chip scale).

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com

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REVISION HISTORY

5/07—Revision 0: Initial Version

SPECIFICATIONS

V_S = 5 V, V_{REF} = 2.5 V, G = 1, R_L = 10 kΩ, T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Conditions	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
OFFSET VOLTAGE	V_{OS} RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			4	15	µV
Average Temperature Drift	T_A = −40°C to +125°C		0.01	0.05	µV/°C
Output Offset, V_{OSO}			15	30	µV
Average Temperature Drift	T_A = −40°C to +125°C		0.05	0.5	µV/°C
INPUT CURRENTS					
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
GAINS	1, 2, 4, 8, 16, 32, 64, 128				
Gain Error					
G = 1				0.05	%
G = 2 to 128				0.8	%
Gain Drift					
G = 1			3	10	ppm/°C
G = 2 to 128			3	10	ppm/°C
CMRR					
G = 1		80			dB
G = 2		86			dB
G = 4		92			dB
G = 8		98			dB
G = 16		104			dB
G = 32		110			dB
G = 64		110			dB
G = 128		110			dB
NOISE	$e_n = \sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$, V_{IN+}, V_{IN-} = 2.5 V				
Input Voltage Noise, e_{ni}	f = 1 kHz		32		nV/√Hz
	f = 1 kHz, T_A = −40°C		27		nV/√Hz
	f = 1 kHz, T_A = 125°C		39		nV/√Hz
	f = 0.1 Hz to 10 Hz,		0.7		µV p-p
Output Voltage Noise, e_{no}	f = 1 kHz		58		nV/√Hz
	f = 1 kHz, T_A = −40°C		50		nV/√Hz
	f = 1 kHz, T_A = 125°C		70		nV/√Hz
	f = 0.1 Hz to 10 Hz		1.1		µV p-p
OTHER INPUT CHARACTERISTICS					
Common-Mode Input Impedance			10‖5		GΩ‖pF
Power Supply Rejection Ratio		100	110		dB
Input Operating Voltage Range		0.05		4.95	V
REFERENCE INPUT					
Input Impedance			28		kΩ
Voltage Range		−0.2		+5.2	V

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth					
G = 1			2.7		MHz
G = 2			2.5		MHz
Gain Bandwidth Product					
G = 4 to 128			7		MHz
Slew Rate			1.1		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100 kΩ to ground	4.9	4.94		V
	R_L = 10 kΩ to ground	4.8	4.88		V
Output Voltage Low	R_L = 100 kΩ to 5 V		60	100	mV
	R_L = 10 kΩ to 5 V		80	200	mV
Short-Circuit Current			70		mA
DIGITAL INTERFACE					
Input Voltage Low	T_A = −40°C to +125°C			1.0	V
Input Voltage High	T_A = −40°C to +125°C	4.0			V
Setup Time to $\overline{CS}$ high	T_A = −40°C to +125°C	50			ns
Hold Time after $\overline{CS}$ high	T_A = −40°C to +125°C	20			ns
OPERATIONAL AMPLIFIER					
INPUT CHARACTERISTICS					
Offset Voltage, V_{OS}			5	15	µV
Temperature Drift	T_A = −40°C to +125°C		0.01	0.06	uV/°C
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
Input Voltage Range		0.05		4.95	V
Open-Loop Gain		100	120		V/mV
Common-Mode Rejection Ratio		100	120		dB
Power Supply Rejection Ratio		100	115		dB
Voltage Noise Density			20		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.4		µV p-p
DYNAMIC PERFORMANCE					
Gain Bandwidth Product			1		MHz
Slew Rate			0.5		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100 kΩ to ground	4.9	4.96		V
	R_L = 10 kΩ to ground	4.8	4.92		V
Output Voltage Low	R_L = 100 kΩ to 5 V		60	100	mV
	R_L = 10 kΩ to 5 V		80	200	mV
Short-Circuit Current			70		mA
BOTH AMPLIFIERS					
POWER SUPPLY					
Quiescent Current			4	5	mA
Quiescent Current (Shutdown)			0.01	1	µA

V_S = 3.0 V, V_{REF} = 1.5 V, T_A = 25°C, G = 1, R_L = 10 kΩ, unless otherwise noted.

Table 3.

Parameter	Conditions	Min	Typ	Max	Unit
INSTRUMENTATION AMPLIFIER					
OFFSET VOLTAGE	V_{OS} RTI = V_{OSI} + V_{OSO}/G				
Input Offset, V_{OSI}			4	15	μV
Average Temperature Drift			0.01	0.05	μV/°C
Output Offset, V_{OSO}			15	30	μV
Average Temperature Drift			0.05	0.5	μV/°C
INPUT CURRENTS					
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
GAINS	1, 2, 4, 8, 16, 32, 64, 128				
Gain Error					
G = 1				0.05	%
G = 2 to 128				0.8	%
Gain Drift					
G = 1			3	10	ppm/°C
G = 2 to 128			3	10	ppm/°C
CMRR					
G = 1		80			dB
G = 2		86			dB
G = 4		92			dB
G = 8		98			dB
G = 16		104			dB
G = 32		110			dB
G = 64		110			dB
G = 128		110			dB
NOISE	$e_n = \sqrt{(e_{ni}^2 + (e_{no}/G)^2)}$				
	V_{IN+}, V_{IN-} = 2.5 V, T_A = 25°C				
Input Voltage Noise, e_{ni}	f = 1 kHz		40		nV/√Hz
	f = 1 kHz, T_A = −40°C		35		nV/√Hz
	f = 1 kHz, T_A = 125°C		48		nV/√Hz
	f = 0.1 Hz to 10 Hz		0.8		μV p-p
Output Voltage Noise, e_{no}	f = 1 kHz		72		nV/√Hz
	f = 1 kHz, T_A = −40°C		62		nV/√Hz
	f = 1 kHz, T_A = 125°C		83		nV/√Hz
	f = 0.1 Hz to 10 Hz		1.4		μV p-p
OTHER INPUT CHARACTERISTICS					
Common-Mode Input Impedance			10‖5		GΩ‖pF
Power Supply Rejection Ratio		100	110		dB
Input Operating Voltage Range		0.05		2.95	V
REFERENCE INPUT					
Input Impedance			28		kΩ‖pF
Voltage Range		−0.2		+3.2	V

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
Bandwidth					
G = 1			2.7		MHz
G = 2			2.5		MHz
Gain Bandwidth Product					
G = 4 to 128			7		MHz
Slew Rate			1.1		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100 kΩ to ground	2.9	2.94		V
	R_L = 10 kΩ to ground	2.8	2.88		V
Output Voltage Low	R_L = 100 kΩ to 3 V		60	100	mV
	R_L = 10 kΩ to 3 V		80	200	mV
Short-Circuit Current			70		mA
DIGITAL INTERFACE					
Input Voltage Low	T_A = −40°C to +125°C			0.7	V
Input Voltage High	T_A = −40°C to +125°C	2.3			V
Setup Time to $\overline{CS}$ high	T_A = −40°C to +125°C	60			ns
Hold Time after $\overline{CS}$ high	T_A = −40°C to +125°C	20			ns
OPERATIONAL AMPLIFIER					
INPUT CHARACTERISTICS					
Offset Voltage, V_{OS}			5	15	µV
Temperature Drift	T_A = −40°C to +125°C		0.01	0.06	µV/°C
Input Bias Current			250	500	pA
	T_A = −40°C to +125°C			5	nA
Input Offset Current			20	100	pA
	T_A = −40°C to +125°C			0.5	nA
Input Voltage Range		0.05		2.95	V
Open-Loop Gain		100	120		V/mV
Common-Mode Rejection Ratio		100	120		dB
Power Supply Rejection Ratio		100	115		dB
Voltage Noise Density			27		nV/√Hz
Voltage Noise	f = 0.1 Hz to 10 Hz		0.6		µV p-p
DYNAMIC PERFORMANCE					
Gain Bandwidth Product			1		MHz
Slew Rate			0.5		V/µs
OUTPUT CHARACTERISTICS					
Output Voltage High	R_L = 100 kΩ to ground	2.9	2.96		V
	R_L = 10 kΩ to ground	2.8	2.82		V
Output Voltage Low	R_L = 100 kΩ to 3 V		60	100	mV
	R_L = 10 kΩ to 3 V		80	200	mV
Short-Circuit Current			70		mA
BOTH AMPLIFIERS					
POWER SUPPLY					
Quiescent Current			3.5	4.5	mA
Quiescent Current (Shutdown)			0.01	1	µA

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Current	Indefinite[1]
Input Voltage (Common-Mode)	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Differential Input Voltage	$-V_S - 0.3$ V to $+V_S + 0.3$ V
Storage Temperature Range	–65°C to +150°C
Operational Temperature Range	–40°C to +125°C
Package Glass Transition Temperature	130°C
ESD (Human Body Model)	1.5 kV
ESD (Charged Device Model)	1.5 kV
ESD (Machine Model)	0.2 kV

[1] For junction temperatures between 105°C and 130°C, short-circuit operation beyond 1000 hours may impact part reliability.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

Table 5.

Thermal Pad	θ_{JA}	Unit
Soldered to Board	54	°C/W
Not Soldered to Board	96	°C/W

The θ_{JA} values in Table 5 assume a 4-layer JEDEC standard board. If the thermal pad is soldered to the board, then it is also assumed it is connected to a plane. θ_{JC} at the exposed pad is 6.3°C/W.

Maximum Power Dissipation

The maximum safe power dissipation for the AD8231 is limited by the associated rise in junction temperature (T_J) on the die. At approximately 130°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the amplifiers. Exceeding a temperature of 130°C for an extended period can result in a loss of functionality.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

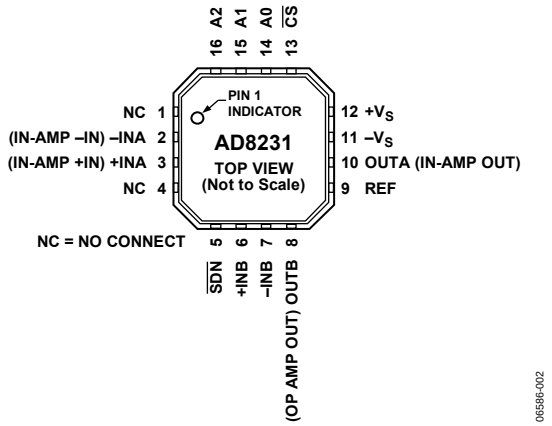

Figure 2. 16-Lead LFCSP (Chip Scale)

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	NC	No Connect.
2	−INA	In-Amp Negative Input.
3	+INA	In-Amp Positive Input.
4	NC	No Connect.
5	$\overline{SDN}$	Shutdown.
6	+INB	Op Amp Positive Input.
7	−INB	Op Amp Negative Input.
8	OUTB	Op Amp Output.
9	REF	In-Amp Reference Pin. It should be driven with a low impedance. Output is referred to this pin.
10	OUTA	In-Amp Output.
11	$-V_S$	Negative Power Supply. Connect to ground in single supply applications.
12	$+V_S$	Positive Power Supply.
13	$\overline{CS}$	Chip Select. Enables digital logic interface.
14	A0	Gain Setting Bit (LSB).
15	A1	Gain Setting Bit.
16	A2	Gain Setting Bit (MSB).

TYPICAL PERFORMANCE CHARACTERISTICS

INSTRUMENTATION AMPLIFIER PERFORMANCE CURVES

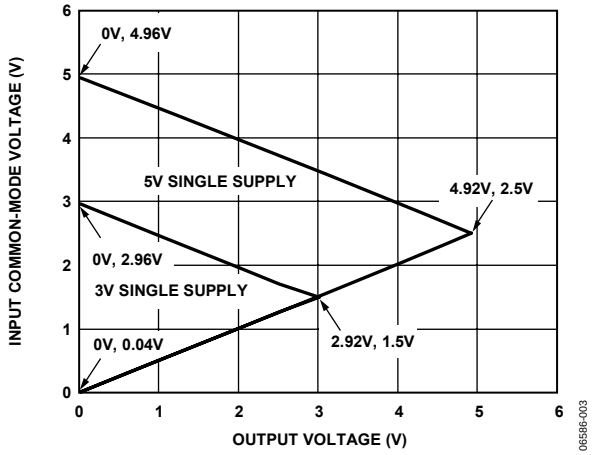

Figure 3. Input Common-Mode Range vs. Output Voltage, V_{REF} = 0 V

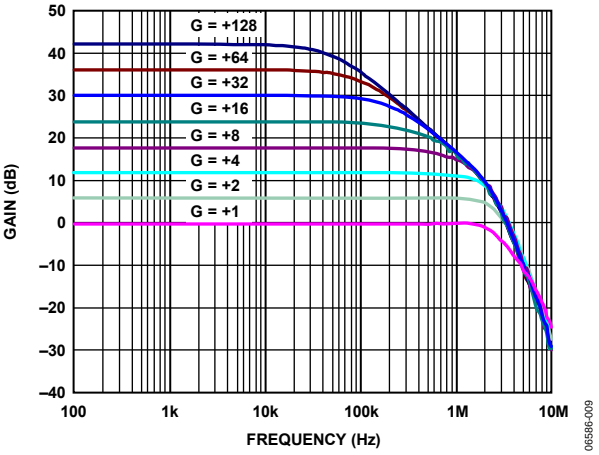

Figure 6. Gain vs. Frequency

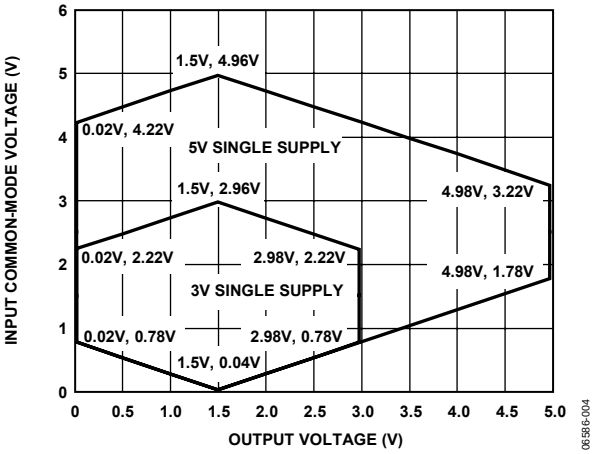

Figure 4. Input Common-Mode Range vs. Output Voltage, V_{REF} = 1.5 V

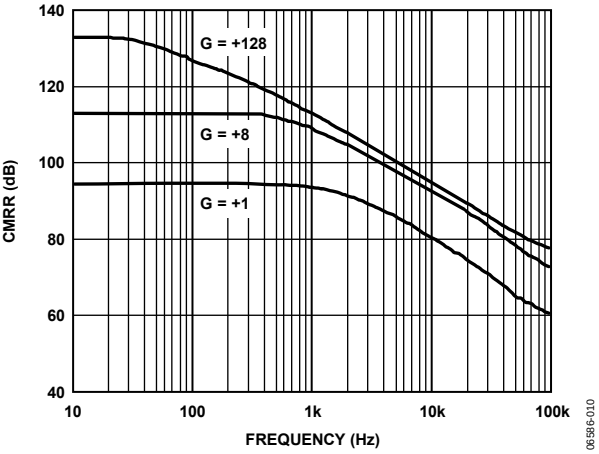

Figure 7. CMRR vs. Frequency

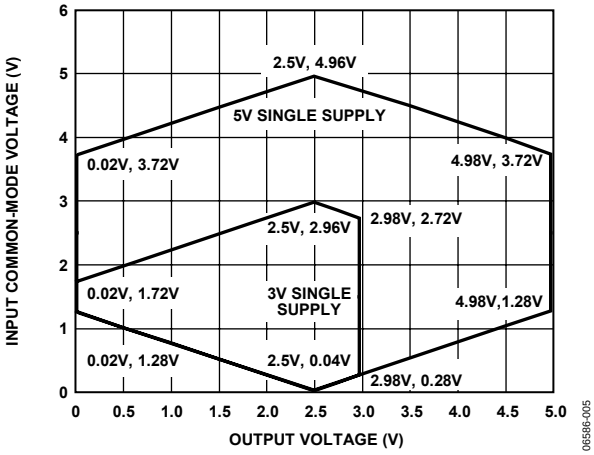

Figure 5. Input Common-Mode Range vs. Output Voltage, V_{REF} = 2.5 V

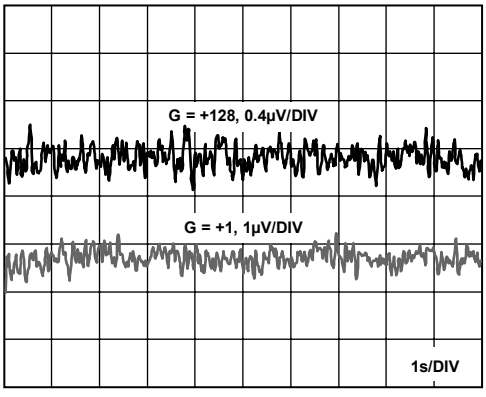

Figure 8. 0.1 Hz to 10 Hz Noise

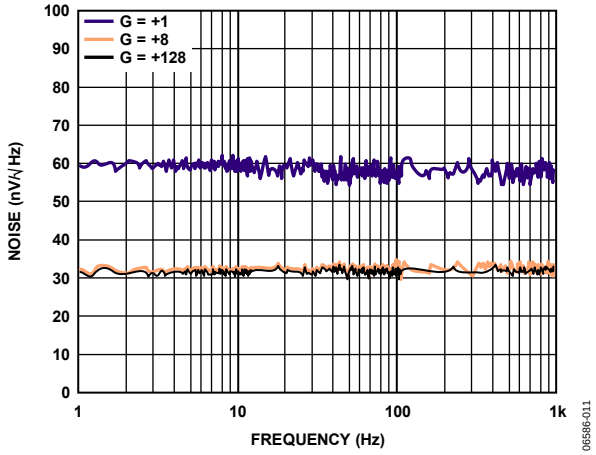

Figure 9. Voltage Noise Spectral Density vs. Frequency, 5 V, 1 Hz to 1000 Hz

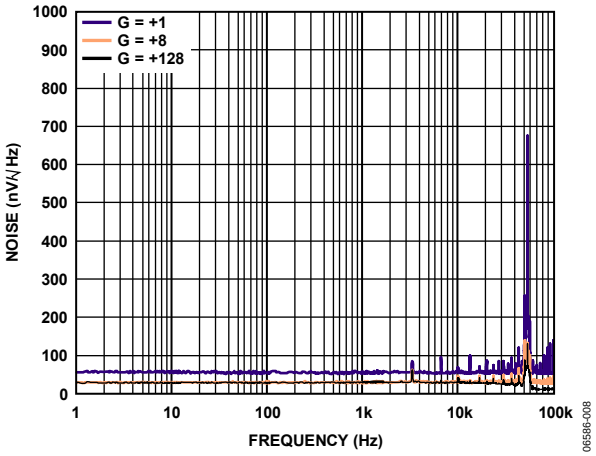

Figure 10. Voltage Noise Spectral Density vs. Frequency, 5V, 1 Hz to 1 MHz

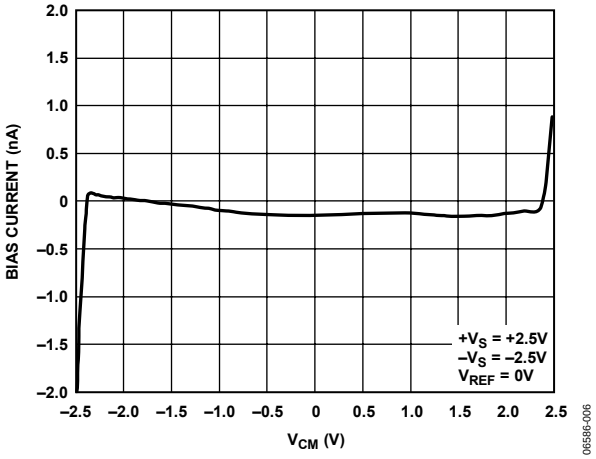

Figure 11. Bias Current vs. Common-Mode Voltage, 5 V

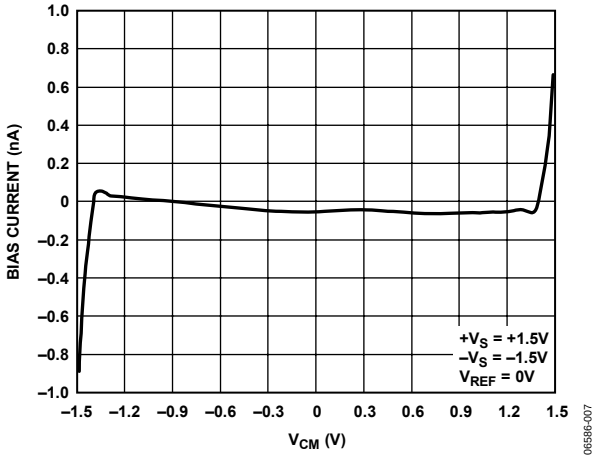

Figure 12. Bias Current vs. Common-Mode Voltage, 3 V

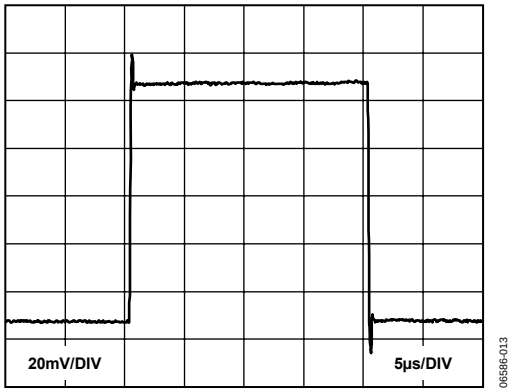

Figure 13. Small Signal Pulse Response, G = 1, R_L = 2 kΩ, C_L = 500 pF

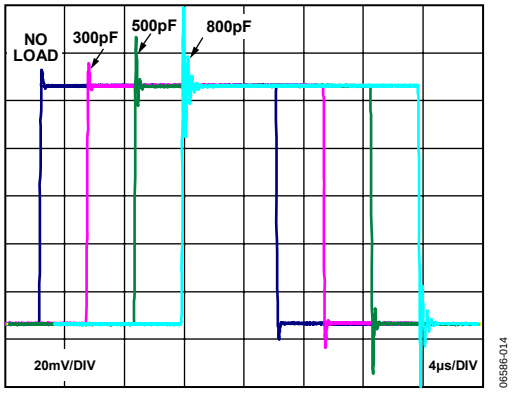

Figure 14. Small Signal Pulse Response for Various Capacitive Loads, G = 1

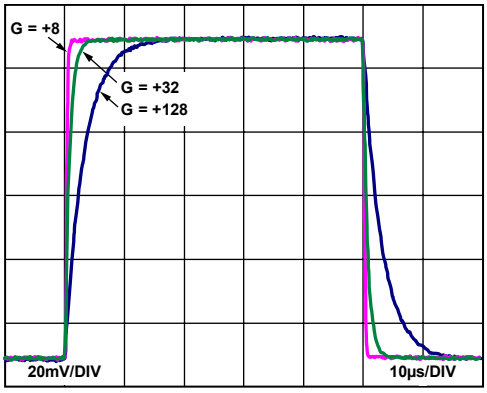

Figure 15. Small Signal Pulse Response, G = 8, 32, 128, R_L = 2 kΩ, C_L = 500 pF

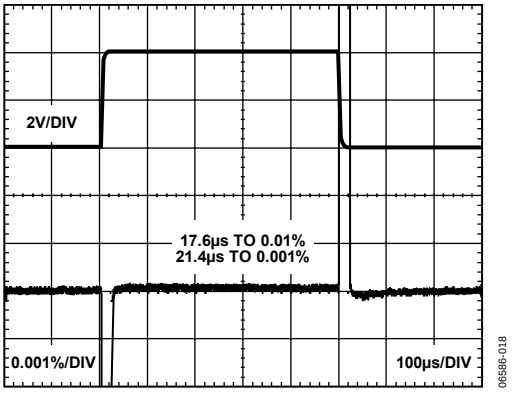

Figure 18. Large Signal Pulse Response, G = 128, V_S = 5 V

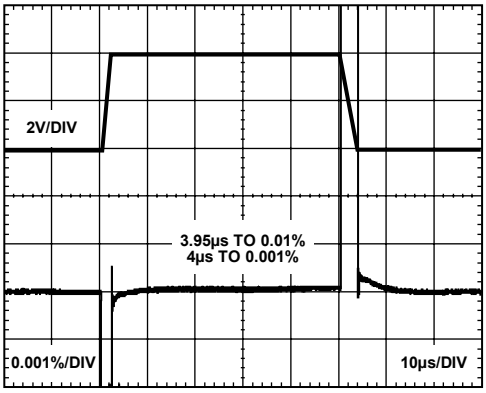

Figure 16. Large Signal Pulse Response, G = 1, V_S = 5 V

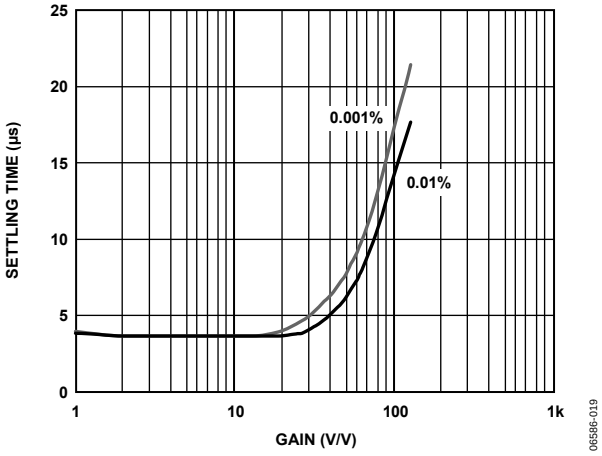

Figure 19. Settling Time vs. Gain for a 4 V p-p Step, V_S = 5 V

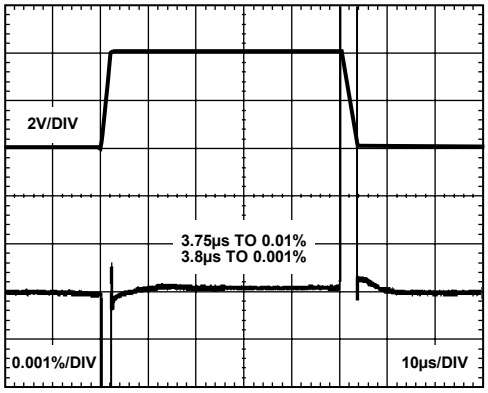

Figure 17. Large Signal Pulse Response, G = 8, V_S = 5 V

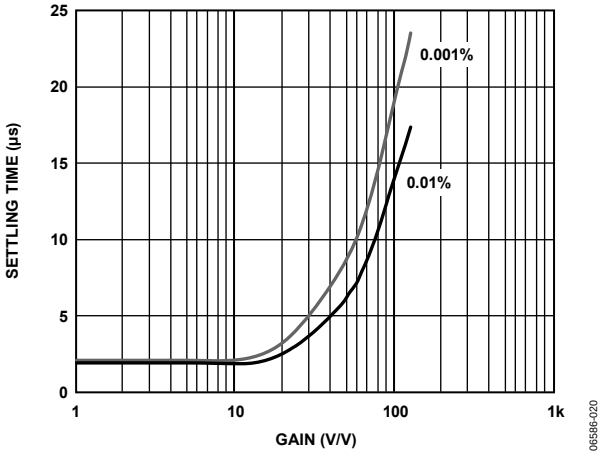

Figure 20. Settling Time vs. Gain for a 2 V p-p Step, V_S = 3 V

OPERATIONAL AMPLIFIER PERFORMANCE CURVES

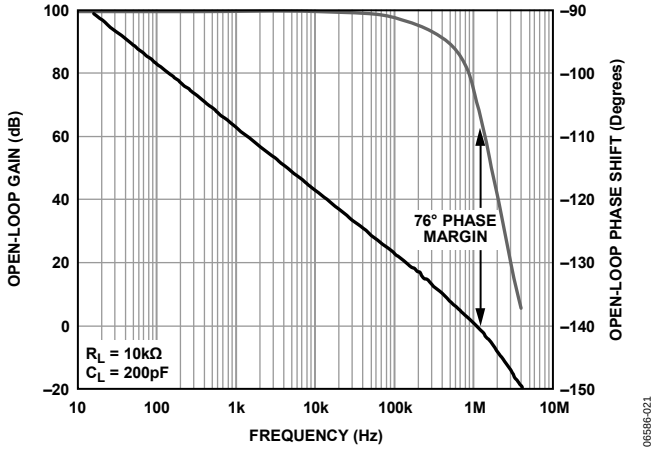

Figure 21. Open Loop Gain and Phase vs. Frequency, V_S = 5 V

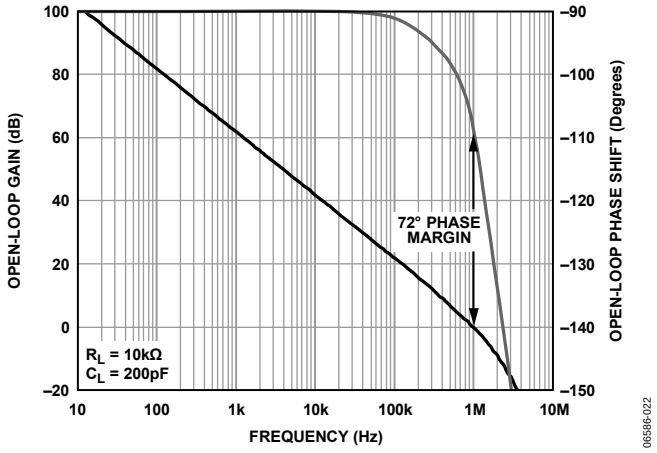

Figure 22. Open Loop Gain and Phase vs. Frequency, V_S = 3 V

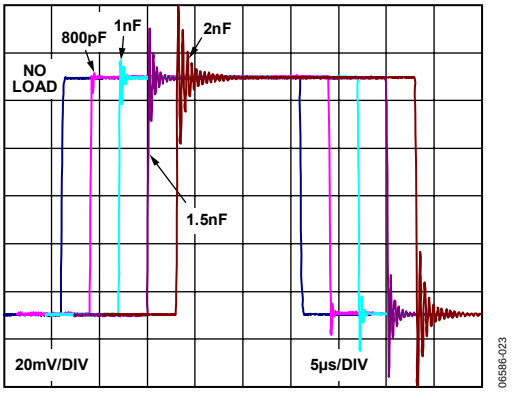

Figure 23. Small Signal Response for Various Capacitive Loads, V_S = 5 V

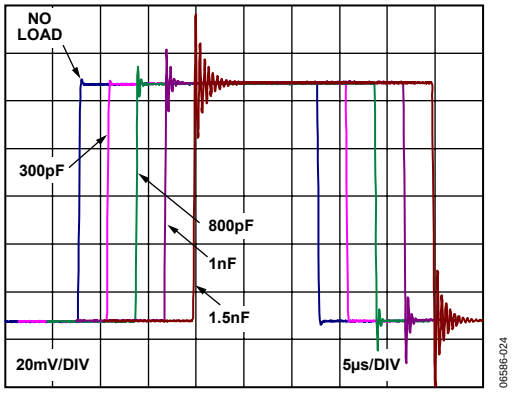

Figure 24. Small Signal Response for Various Capacitive Loads, V_S = 3 V

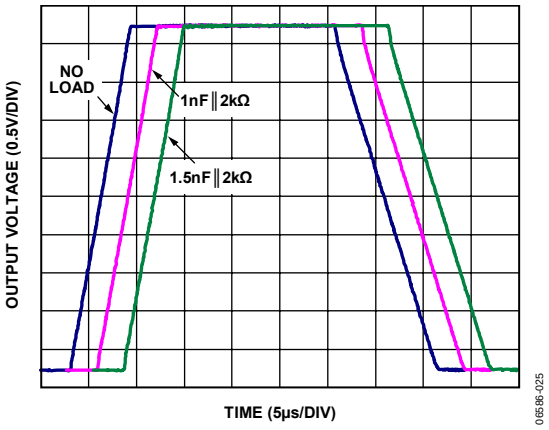

Figure 25. Large Signal Transient Response, V_S = 5 V

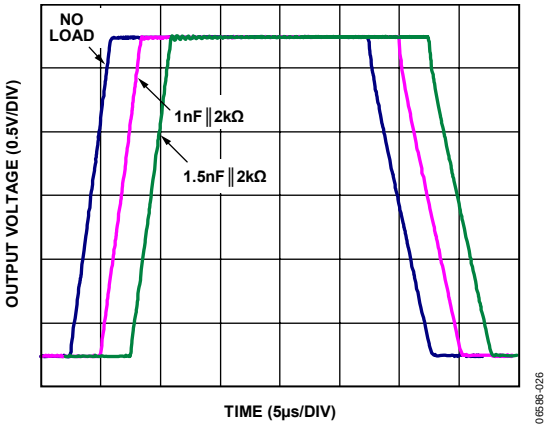

Figure 26. Large Signal Transient Response, V_S = 3 V

PERFORMANCE CURVES VALID FOR BOTH AMPLIFIERS

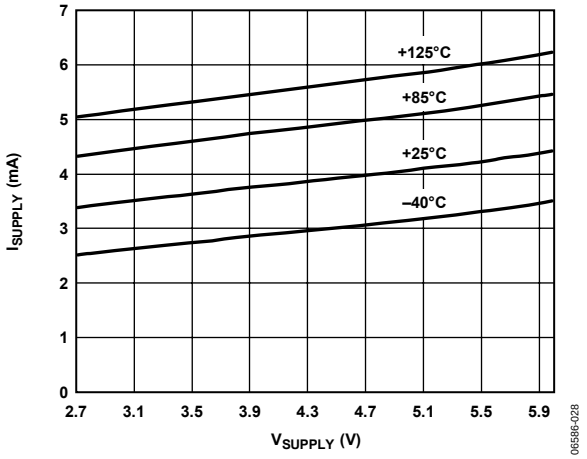

Figure 27. Supply Current vs. Supply Voltage

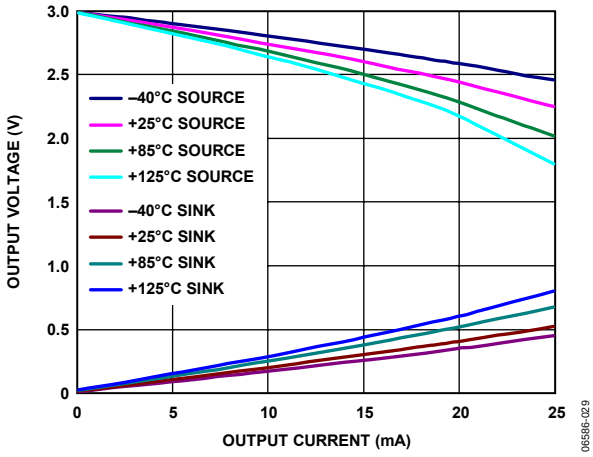

Figure 28. Output voltage Swing vs. Output Current, V_S = 3 V

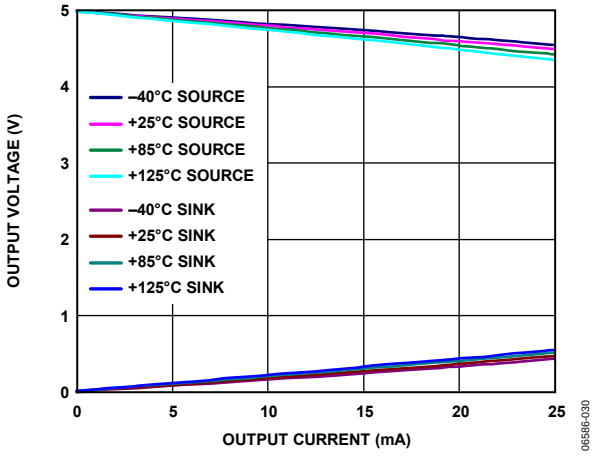

Figure 29. Output Voltage Swing vs. Output Current, V_S = 5 V

THEORY OF OPERATION

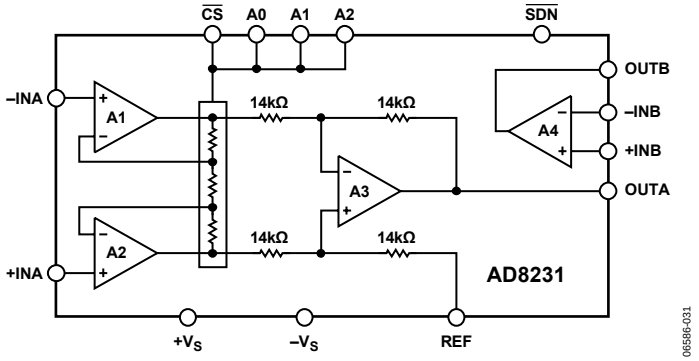

Figure 30. Simplified Schematic

AMPLIFIER ARCHITECTURE

The AD8231 is based on the classic 3-op amp topology. This topology has two stages: a preamplifier to provide amplification, followed by a difference amplifier to remove the common-mode voltage. Figure 30 shows a simplified schematic of the AD8231. The preamp stage is composed of Amplifier A1, Amplifier A2, and a digitally controlled resistor network. The second stage is a gain of 1 difference amplifier composed of A3 and four 14 kΩ resistors. Amplifier A1, Amplifier A2, and Amplifier A3 are all zero drift, rail-to-rail input, rail-to rail-output amplifiers.

The AD8231 design makes it extremely robust over temperature. The AD8231 uses an internal thin film resistor to set the gain. Since all of the resistors are on the same die, gain temperature drift performance and CMRR drift performance are better than can be achieved with topologies using external resistors. The AD8231 also uses an auto-zero topology to null the offsets of all its internal amplifiers. Since this topology continually corrects for any offset errors, offset temperature drift is nearly nonexistent.

The AD8231 also includes a free operational amplifier. Like the other amplifiers in the AD8231, it is a zero drift, rail-to-rail input, rail-to-rail output architecture.

GAIN SELECTION

The AD8231's gain is set by voltages applied to the A0, A1, and A2 pins. To change the gain, the $\overline{CS}$ pin must be driven low. When the $\overline{CS}$ pin is driven high, the gain is latched, and voltages at the A0 to A2 pins have no effect. Table 7 shows the different gain settings.

The time required for a gain change is dominated by the settling time of the amplifier. The AD8231 takes about 200 ns to switch gains, after which the amplifier begins to settle. Refer to Figure 16 through Figure 20 to determine the settling time for different gains.

Table 7. Truth Table for AD8231 Gain Settings

$\overline{CS}$	A2	A1	A0	Gain
Low	Low	Low	Low	1
Low	Low	Low	High	2
Low	Low	High	Low	4
Low	Low	High	High	8
Low	High	Low	Low	16
Low	High	Low	High	32
Low	High	High	Low	64
Low	High	High	High	128
High	X	X	X	No change

REFERENCE TERMINAL

The output voltage of the AD8231 is developed with respect to the potential on the reference terminal. This is useful when the output signal needs to be offset to a midsupply level. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8231 can drive a single-supply ADC. The REF pin is protected with ESD diodes and should not exceed either $+V_S$ or $-V_S$ by more than 0.3 V.

For best performance, source impedance to the REF terminal should be kept below 1 Ω. As shown in Figure 30, the reference terminal, REF, is at one end of a 14 kΩ resistor. Additional impedance at the REF terminal adds to this 14 kΩ resistor and results in amplification of the signal connected to the positive input, causing a CMRR error.

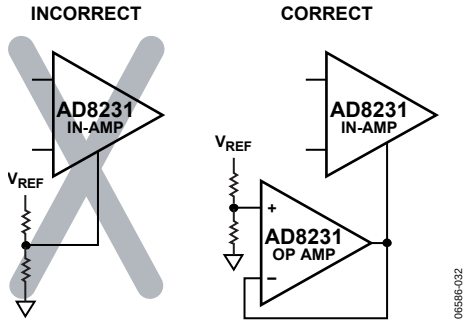

Figure 31. Driving the Reference Pin

LAYOUT

The AD8231 is a high precision device. To ensure optimum performance at the PC board level, care must be taken in the design of the board layout. The AD8231 pinout is arranged in a logical manner to aid in this task.

Power Supplies

The AD8231 should be decoupled with a 0.1 µF bypass capacitor between the two supplies. This capacitor should be placed as close as possible to Pin 11 and Pin 12, either directly next to the pins or beneath the pins on the backside of the board. The AD8231's auto-zero architecture requires a low ac impedance between the supplies. Long trace lengths to the bypass capacitor increase this impedance, which results in a larger input offset voltage.

A stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance.

Package Considerations

The AD8231 comes in a 4 mm × 4 mm LFCSP. Beware of blindly copying the footprint from another 4 mm × 4 mm LFCSP part; it may not have the same thermal pad size and leads. Refer to the Outline Dimensions section to verify that the PCB symbol has the correct dimensions. Space between the leads and thermal pad should be kept as wide as possible for the best bias current performance.

Thermal Pad

The AD8231 4 mm × 4 mm LFCSP comes with a thermal pad. This pad is connected internally to $-V_S$. The pad can either be left unconnected or connected to the negative supply rail. For high vibration applications, a landing is recommended.

Because the AD8231 dissipates little power, heat dissipation is rarely an issue. If improved heat dissipation is desired (for example, when ambient temperatures are near 125°C or when driving heavy loads), connect the thermal pad to the negative supply rail. For the best heat dissipation performance, the negative supply rail should be a plane in the board. See the Thermal Resistance section for thermal coefficients with and without the pad soldered.

INPUT BIAS CURRENT RETURN PATH

The input bias current of the AD8231 must have a return path to common. When the source, such as a thermocouple, cannot provide a return current path, one should be created, as shown in Figure 32.

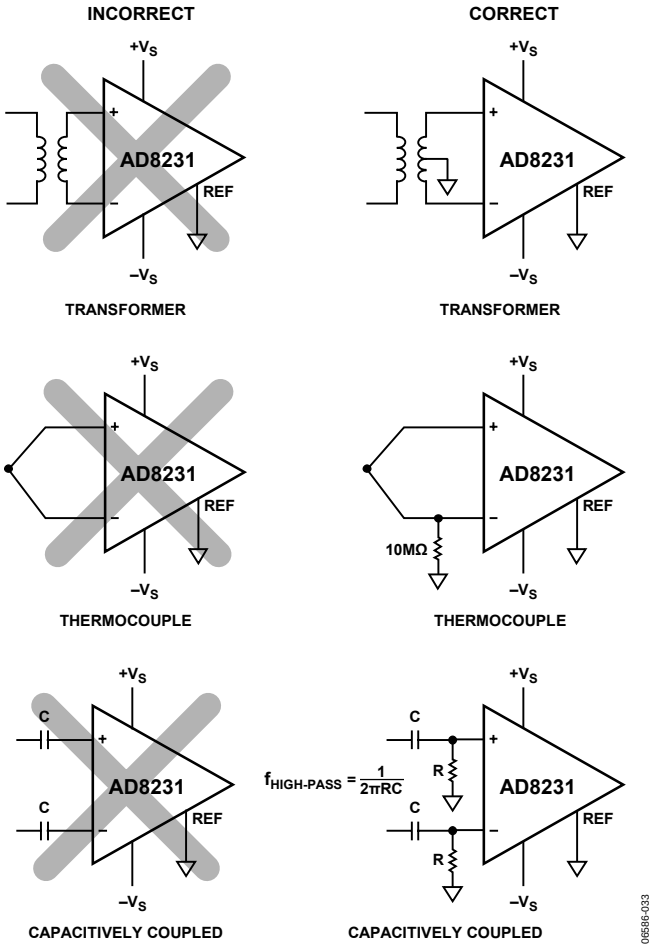

Figure 32. Creating an I_{BIAS} Path

RF INTERFERENCE

RF rectification is often a problem when amplifiers are used in applications where there are strong RF signals. The disturbance can appear as a small dc offset voltage. High frequency signals can be filtered with a low-pass, RC network placed at the input of the instrumentation amplifier, as shown in Figure 33. The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{Diff} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

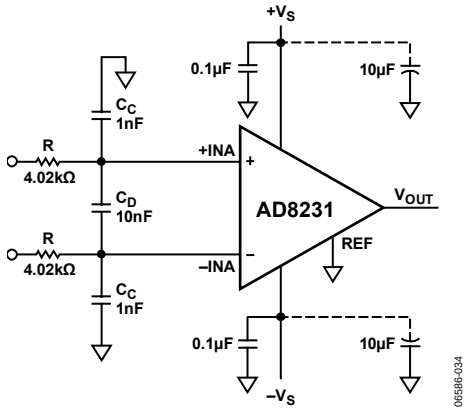

Figure 33. RFI Suppression

Figure 33 shows an example where the differential filter frequency is approximately 2 kHz, and the common-mode filter frequency is approximately 40 kHz.

Values of R and C_C should be chosen to minimize RFI. Mismatch between the R × C_C at the positive input and the R × C_C at negative input degrades the CMRR of the AD8231. By using a value of C_D ten times larger than the value of C_C, the effect of the mismatch is reduced and performance is improved.

COMMON-MODE INPUT VOLTAGE RANGE

The 3-op amp architecture of the AD8231 applies gain and then removes the common-mode voltage. Therefore, internal nodes in the AD8231 experience a combination of both the gained signal and the common-mode signal. This combined signal can be limited by the voltage supplies even when the individual input and output signals are not. To determine whether the signal could be limited, refer to Figure 3 through Figure 5 or use the following formula:

$$-V_S + 0.04\text{ V} < V_{CM} \pm \frac{|V_{DIFF}| \times Gain}{2} < +V_S - 0.04\text{ V}$$

If more common mode range is required, the simplest solution is to apply less gain in the instrumentation amplifier. The extra op amp can be used to provide another gain stage after the in-amp. Because the AD8231 has good offset and noise performance at low gains, applying less gain in the instrumentation amplifier generally has a limited impact on the overall system performance.

APPLICATIONS INFORMATION

DIFFERENTIAL OUTPUT

Figure 34 shows how to create a differential output in-amp using the AD8231 uncommitted op amp. Errors from the op amp are common to both outputs and are thus common-mode. Errors from mismatched resistors also create a common-mode dc offset. Because these errors are common-mode, they will likely be rejected by the next device in the signal chain.

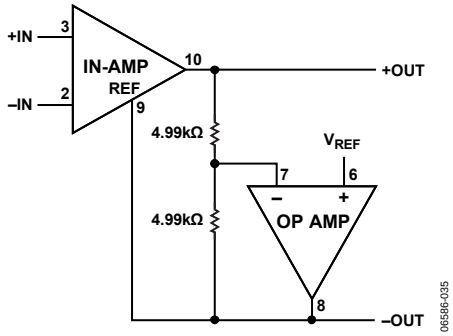

Figure 34. Differential Output Using Op Amp

MULTIPLEXING

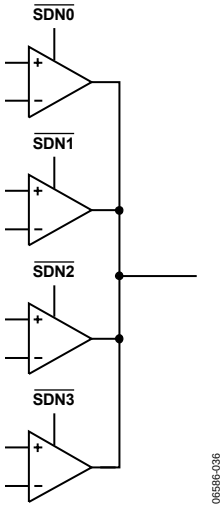

Figure 35.

The outputs of both the AD8231 in-amp and op amp are high impedance in the shutdown state. This feature allows several AD8231s to be multiplexed together without any external switches. Figure 35 shows an example of such a configuration. All the outputs are connected together and only one amplifier is turned on at a time. This feature is analogous to the high Z mode of digital tristate logic. Because the output impedance in shutdown is multiple megaohms, several thousand AD8231s can theoretically be multiplexed in such a way.

The AD8231 can enter and leave shutdown mode very quickly. However, when the amplifier wakes up and reconnects its input circuitry, the voltage at its internal input nodes changes dramatically. It will take time for the output of the amplifier to settle. Refer to Figure 16 through Figure 20 to determine the settling time for different gains. This settling time limits how quickly the user can multiplex the AD8231 with the $\overline{SDN}$ pin.

OUTLINE DIMENSIONS

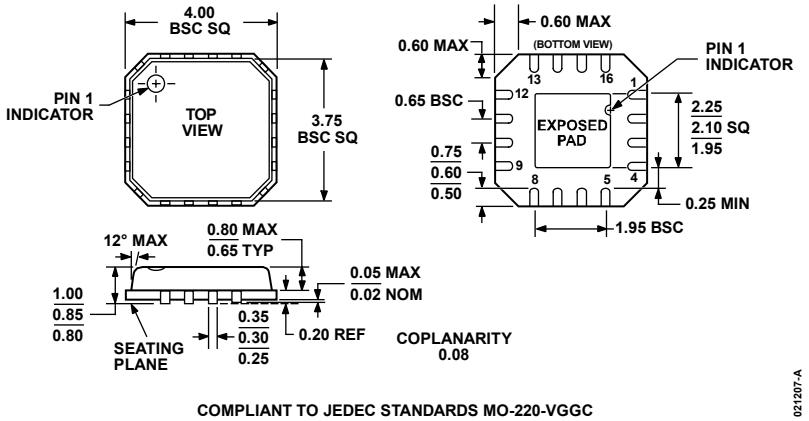

Figure 36. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-16-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8231ACPZ-R7[1]	−40°C to +125°C	16-Lead LFCSP_VQ, 7″ Tape and Reel	CP-16-4
AD8231ACPZ-RL[1]	−40°C to +125°C	16-Lead LFCSP_VQ, 13″ Tape and Reel	CP-16-4
AD8231ACPZ-WP[1]	−40°C to +125°C	16-Lead LFCSP_VQ, Waffle Pack	CP-16-4

[1] Z = RoHS Compliant Part.

NOTES

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