100 dB Range (10 nA to 1 mA) Logarithmic Converter

AD8305*

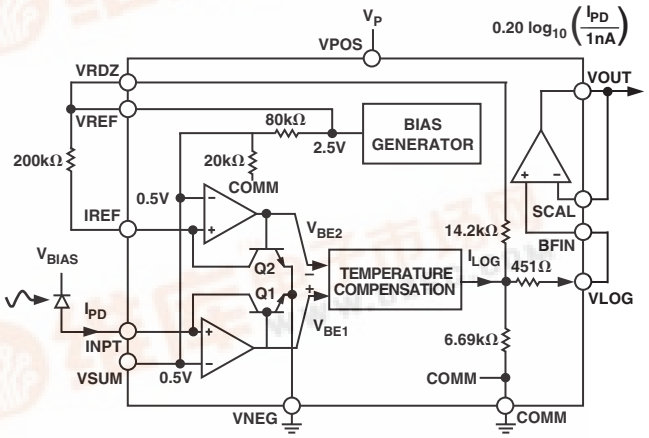
FEATURES

Optimized for Fiber Optic Photodiode Interfacing
Measures Current over 5 Decades
  Law Conformance 0.1 dB from 10 nA to 1 mA
Single- or Dual-Supply Operation (3 V to 12 V Total)
Full Log-Ratio Capabilities
Nominal Slope of 10 mV/dB (200 mV/Decade)
Nominal Intercept of 1 nA (Set by External Resistor)
  Optional Adjustment of Slope and Intercept
Complete and Temperature Stable
Rapid Response Time for a Given Current Level
Miniature 16-Lead Chip Scale Package
  (LFCSP 3 mm × 3 mm)
Low Power: ~5 mA Quiescent Current

APPLICATIONS

Optical Power Measurement
Wide Range Baseband Logarithmic Compression
Measurement of Current and Voltage Ratios
Optical Absorbance Measurement

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8305 is an inexpensive microminiature logarithmic converter optimized for determining optical power in fiber optic systems. It uses an advanced implementation of a classic translinear (junction based) technique to provide a large dynamic range in a versatile and easily used form. A single-supply voltage of between 3 V and 12 V is adequate; dual supplies may optionally be used. The low quiescent current (typically 5 mA) permits use in battery-operated applications.

The input current, I_{PD}, of 10 nA to 1 mA applied to the INPT pin is the collector current of an optimally scaled NPN transistor, which converts this current to a voltage (V_{BE}) with a precise logarithmic relationship. A second such converter is used to handle the reference current (I_{REF}) applied to pin IREF. These input nodes are biased slightly above ground (0.5 V). This is generally acceptable for photodiode applications where the anode does not need to be grounded. Similarly, this bias voltage is easily accounted for in generating I_{REF}. The output of the logarithmic front end is available at Pin VLOG.

The basic logarithmic slope at this output is nominally 200 mV/decade (10 mV/dB). Thus, a 100 dB range corresponds to an output change of 1 V. When this voltage (or the buffer output) is applied to an ADC that permits an external reference voltage to be employed, the AD8305's voltage reference output of 2.5 V at Pin VREF can be used to improve the scaling accuracy. Suitable ADCs include the AD7810 (serial 10-bit), AD7823 (serial 8-bit), and AD7813 (parallel, 8-bit or 10-bit). Other values of the logarithmic slope can be provided using a simple external resistor network.

The logarithmic intercept (also known as the reference current) is nominally positioned at 1 nA by the use of the externally generated current, I_{REF}, of 10 μA, provided by a 200 kΩ resistor connected between VREF, at 2.5 V, and the reference input IREF, at 0.5 V. The intercept can be adjusted over a wide range by varying this resistor. The AD8305 can also operate in a log-ratio mode, with the numerator current applied to INPT and the denominator current applied to IREF.

A buffer amplifier is provided for driving a substantial load, for use in raising the basic slope of 10 mV/dB to higher values, as a precision comparator (threshold detector), or in implementing low-pass filters. Its rail-to-rail output stage can swing to within 100 mV of the positive and negative supply rails, and its peak current sourcing capacity is 25 mA.

It is a fundamental aspect of translinear logarithmic converters that the small signal bandwidth falls as the current level diminishes, and the low frequency noise-spectral density increases. At the 10 nA level, the bandwidth of the AD8305 is about 50 kHz, and increases in proportion to I_{PD} up to a maximum value of about 15 MHz. Using the buffer amplifier, the increase in noise level at low currents can be addressed by using it to realize low-pass filters of up to three poles.

The AD8305 is available in a 16-lead LFCSP package and is specified for operation from –40°C to +85°C.

*Protected by U.S. Patent No. 4,604,532 and 5,519,308; other patents pending.

REV. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

AD8305–SPECIFICATIONS (V_P = 5 V, V_N = 0 V, T_A = 25°C, R_{REF} = 200 kΩ, and VRDZ connected to VREF, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
INPUT INTERFACE	Pin 4, INPT, Pin 3, IREF				
Specified Current Range, I_{PD}	Flows toward INPT Pin	10 n		1 m	A
Input Current Min/Max Limits	Flows toward INPT Pin			10 m	A
Reference Current, I_{REF}, Range	Flows toward IREF Pin	10 n		1 m	A
Summing Node Voltage	Internally Preset; May be Altered by User	0.46	0.5	0.54	V
Temperature Drift	–40°C < T_A < +85°C		0.015		mV/°C
Input Offset Voltage	$V_{INPT} - V_{SUM}$, $V_{IREF} - V_{SUM}$	–20		+20	mV
LOGARITHMIC OUTPUT	Pin 9, VLOG				
Logarithmic Slope		190	200	210	mV/dec
	–40°C < T_A < +85°C	185		215	mV/dec
Logarithmic Intercept[1]		0.3	1	1.7	nA
	–40°C < T_A < +85°C	0.1		2.5	nA
Law Conformance Error	10 nA < I_{PD} < 1 mA		0.1	0.4	dB
Wideband Noise[2]	I_{PD} > 1 μA		0.7		$\mu V\sqrt{Hz}$
Small Signal Bandwidth[2]	I_{PD} > 1 μA		0.7		MHz
Maximum Output Voltage			1.7		V
Minimum Output Voltage	Limited by V_N = 0 V		0.01		V
Output Resistance		4.375	5	5.625	kΩ
REFERENCE OUTPUT	Pin 2, VREF				
Voltage wrt Ground		2.435	2.5	2.565	V
	–40°C < T_A < +85°C	2.4		2.6	V
Maximum Output Current	Sourcing (Grounded Load)		20		mA
Incremental Output Resistance	Load Current < 10 mA		2		Ω
OUTPUT BUFFER	Pin 10, BFIN; Pin 11, SCAL; Pin 12, VOUT				
Input Offset Voltage		–20		+20	mV
Input Bias Current	Flowing out of Pin 10 or 11		0.4		mA
Incremental Input Resistance			35		MΩ
Output Range	R_L = 1 kΩ to ground		V_P – 0.1		V
Incremental Output Resistance	Load Current < 10 mA		0.5		Ω
Peak Source/Sink Current			25		mA
Small Signal Bandwidth	GAIN = 1		15		MHz
Slew Rate	0.2 V to 4.8 V Output Swing		15		V/μs
POWER SUPPLY	Pin 8, VPOS; Pin 6 and Pin 7, VNEG				
Positive Supply Voltage	($V_P - V_N$) ≤ 12 V	3	5	12	V
Quiescent Current			5.4	6.5	mA
Negative Supply Voltage (Optional)	($V_P - V_N$) ≤ 12 V	–5.5	0		V

NOTES
[1]Other values of logarithmic intercept can be achieved by adjusting R_{REF}.
[2]Output noise and incremental bandwidth are functions of input current, measured using output buffer connected for GAIN = 1.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage $V_P - V_N$ . . . . . 12 V
Input Current . . . . . 20 mA
Internal Power Dissipation . . . . . 500 mW
θ_{JA}[2] . . . . . 30°C/W
Maximum Junction Temperature . . . . . 125°C
Operating Temperature Range . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 sec) . . . . . 300°C

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2] With package die paddle soldered to thermal pad containing nine vias connected to inner and bottom layers.

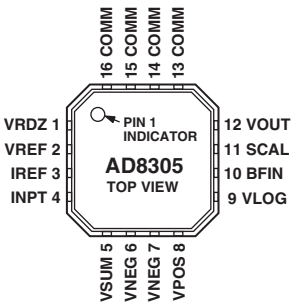
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8305ACP	–40°C to +85°C	16-Lead LFCSP	CP-16
AD8305ACP-REEL7	7" Tape and Reel		
AD8305-EVAL	Evaluation Board		

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8305 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

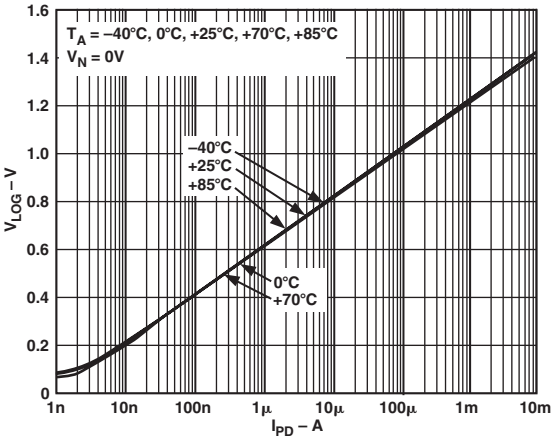


PIN FUNCTION DESCRIPTIONS

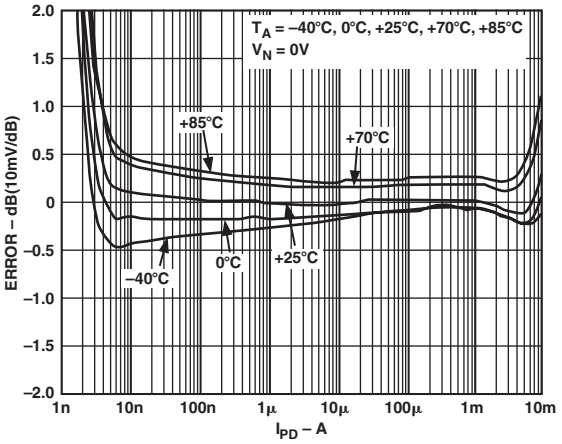
Pin No.	Mnemonic	Function
1	VRDZ	Top of a Resistive Divider Network that Offsets V_{LOG} to Position the Intercept. Normally connected to VREF; may also be connected to ground when bipolar outputs are to be provided.
2	VREF	Reference Output Voltage of 2.5 V.
3	IREF	Accepts (Sinks) Reference Current, $I_{REF.}$
4	INPT	Accepts (Sinks) Photodiode Current, I_{PD}. Usually connected to photodiode anode such that photo current flows into INPT.
5	VSUM	Guard Pin. Used to shield the INPT current line and for optional adjustment of the INPT and I_{REF} node potential.
6, 7	VNEG	Optional Negative Supply, V_N. (This pin is usually grounded; for details of usage, see the Applications section).
8	VPOS	Positive Supply, $(V_P - V_N) \leq 12$ V.
9	VLOG	Output of the Logarithmic Front End.
10	BFIN	Buffer Amplifier Noninverting Input.
11	SCAL	Buffer Amplifier Inverting Input.
12	VOUT	Buffer Output.
13–16	COMM	Analog Ground.

AD8305–Typical Performance Characteristics

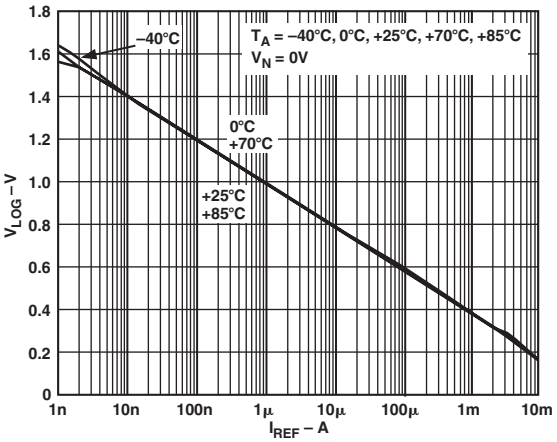
(V_P = 5 V, V_N = 0 V, R_{REF} = 200 kΩ, T_A = 25°C, unless otherwise noted.)



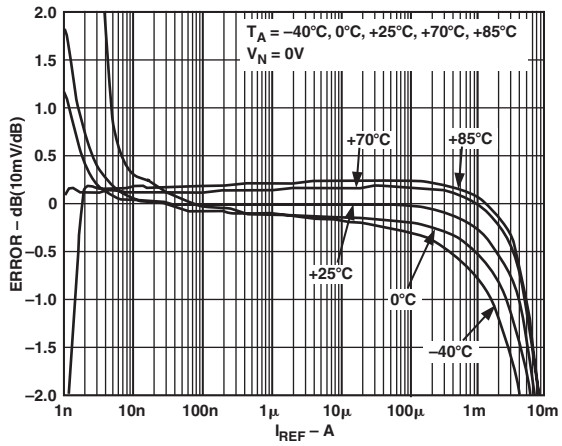
TPC 1. V_{LOG} vs. I_{PD} for Multiple Temperatures



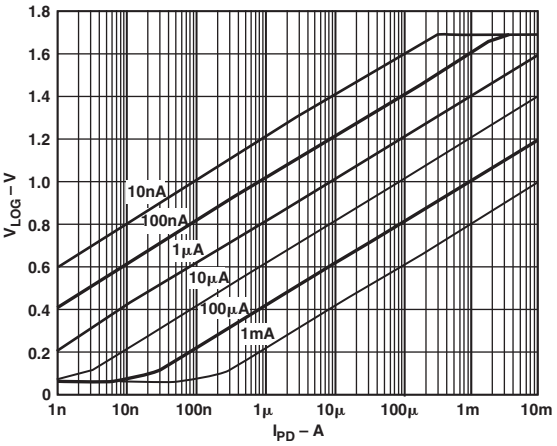
TPC 4. Law Conformance Error vs. I_{PD} (at I_{REF} = 10 μA) for Multiple Temperatures, Normalized to 25°C



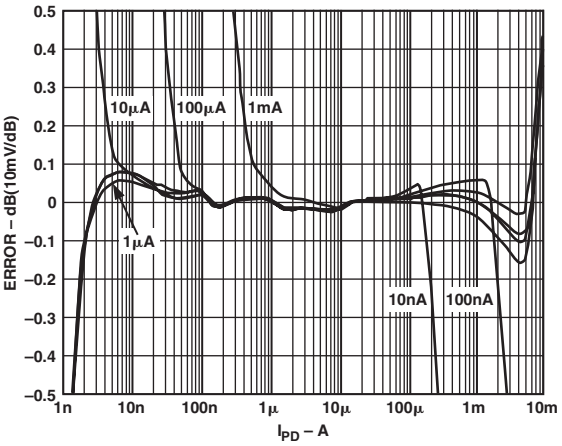
TPC 2. V_{LOG} vs. I_{REF} for Multiple Temperatures



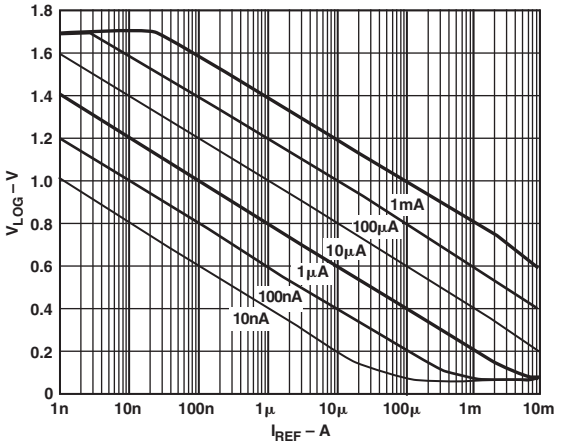
TPC 5. Law Conformance Error vs. I_{REF} (at I_{PD} = 10 μA) for Multiple Temperatures, Normalized to 25°C



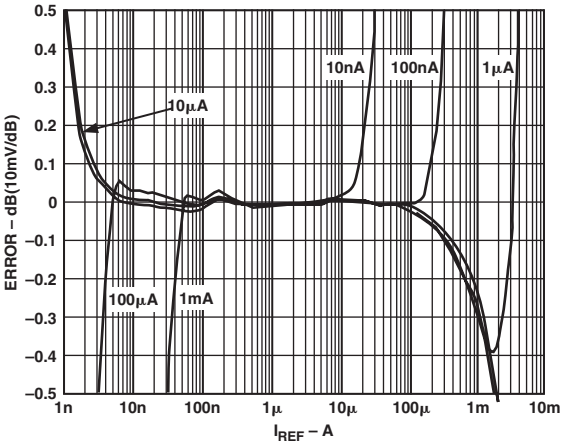
TPC 3. V_{LOG} vs. I_{PD} for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)



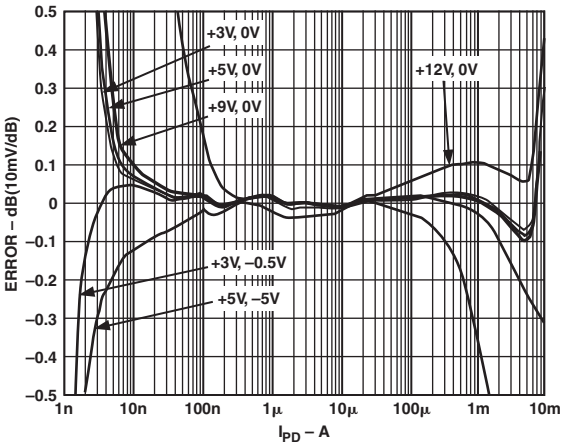
TPC 6. Law Conformance Error vs. I_{PD} for Multiple Values of I_{REF} (Decade Steps from 10 nA to 1 mA)



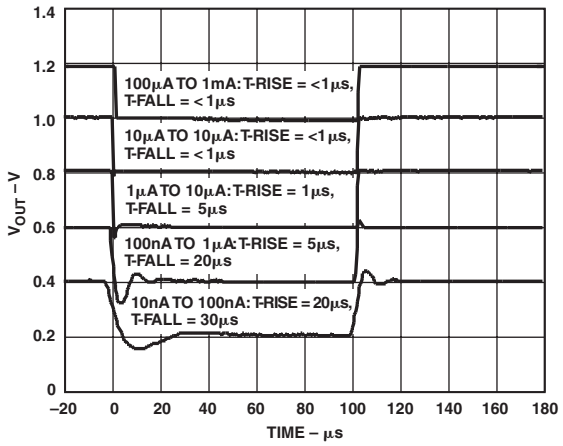
TPC 7. V_{LOG} vs. I_{REF} for Multiple Values of I_{PD} (Decade Steps from 10 nA to 1 mA)



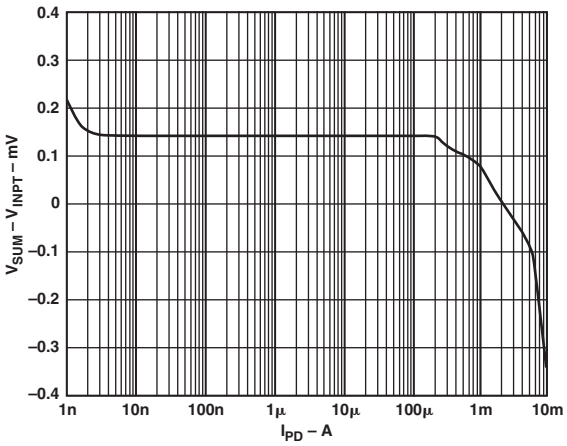
TPC 10. Law Conformance Error vs. I_{REF} for Multiple Values of I_{PD} (Decade Steps from 10 nA to 1 mA)



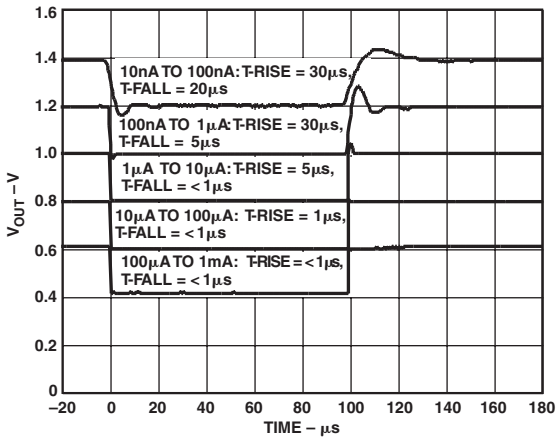
TPC 8. Law Conformance Error vs. I_{PD} for Various Supply Conditions (see Annotations)



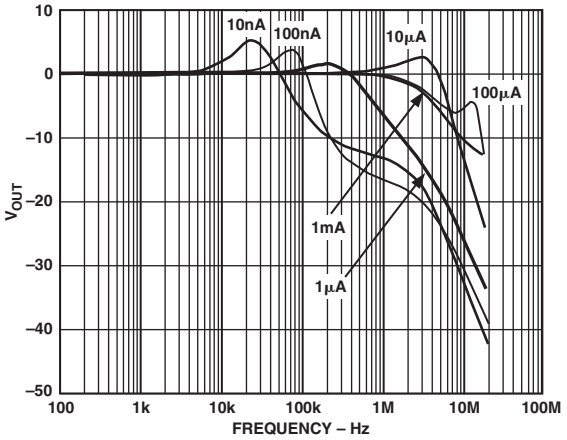
TPC 11. Pulse Response – I_{PD} to V_{OUT} (G = 1)



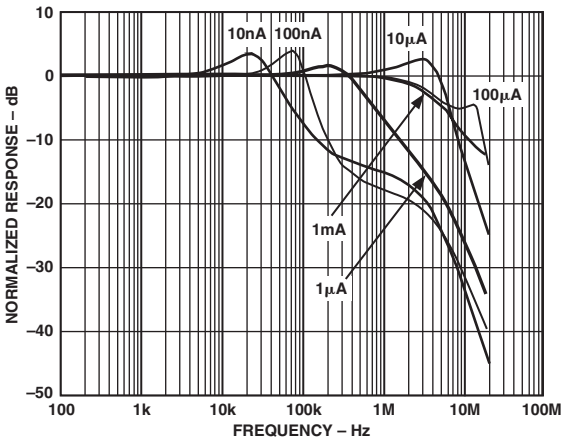
TPC 9. V_{INPT} – V_{SUM} vs. I_{PD}



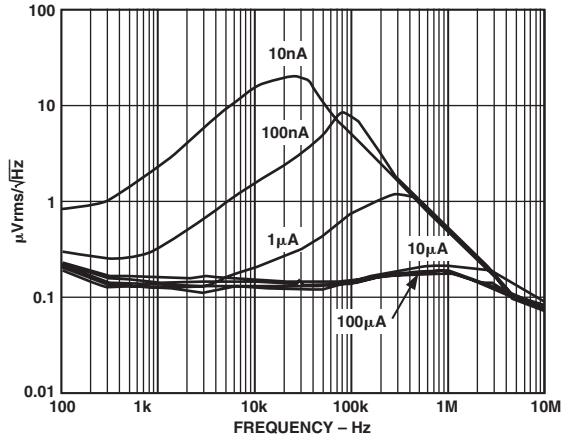
TPC 12. Pulse Response – I_{REF} to V_{OUT} (G = 1)



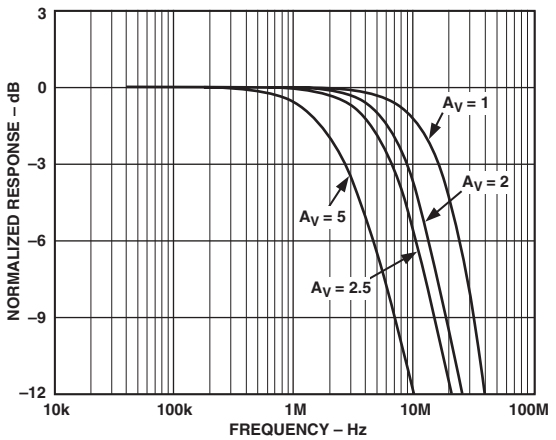
TPC 13. Small Signal AC Response (5% Sine Modulation), from I_{PD} to V_{OUT} (G = 1) for I_{PD} in Decade Steps from 10 nA to 1 mA, I_{REF} = 10 μA



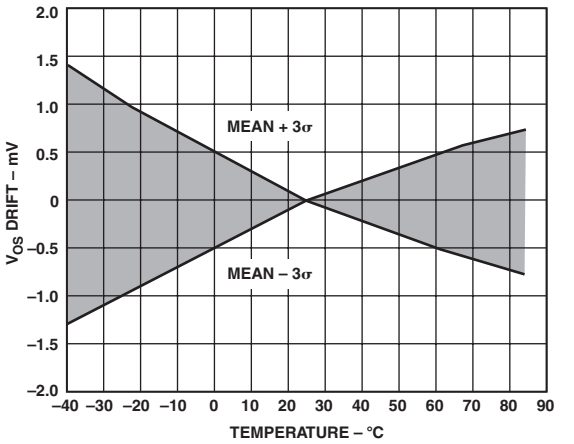
TPC 14. Small Signal AC Response (5% Sine Modulation), from I_{REF} to V_{OUT} (G = 1) for I_{REF} in Decade Steps from 10 nA to 1 mA, I_{PD} = 10 μA



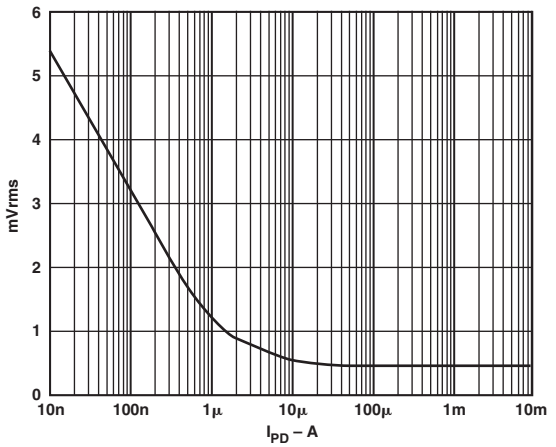
TPC 15. Spot Noise Spectral Density at V_{OUT} (G = 1) vs. Frequency for I_{PD} in Decade Steps from 10 nA to 1 mA



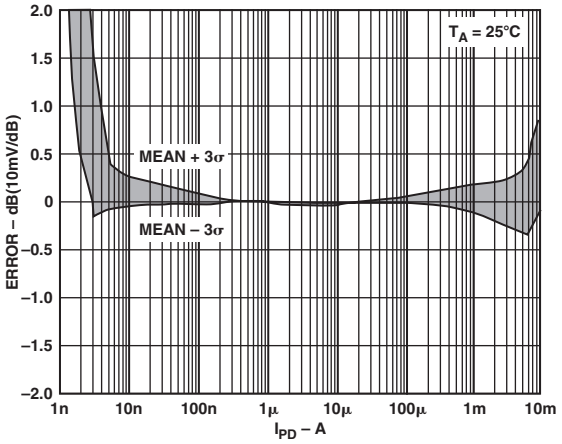
TPC 16. Small Signal AC Response of the Buffer for Various Closed-Loop Gains (R_L = 1 kΩ C_L < 2 pF)



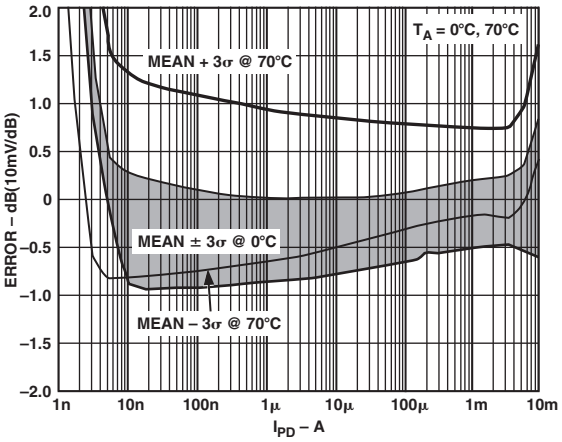
TPC 17. Buffer Input Offset Drift vs. Temperature (3σ to Either Side of Mean)



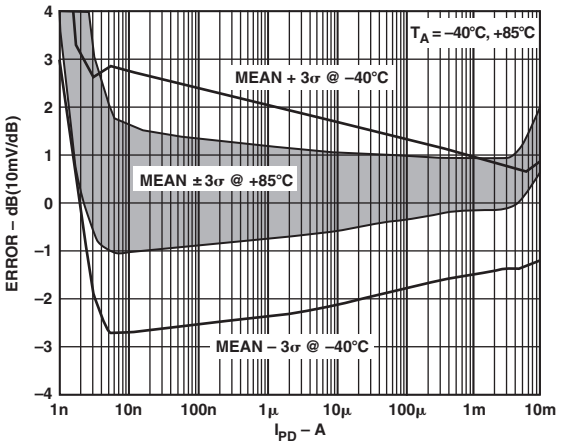
TPC 18. Total Wideband Noise Voltage at V_{OUT} vs. I_{PD} (G = 1)



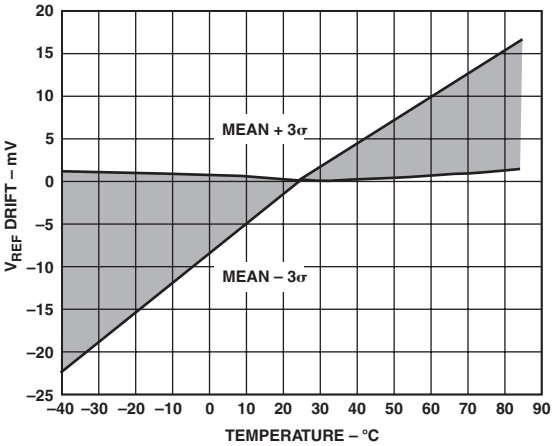
TPC 19. Law Conformance Error Distribution (3σ to Either Side of Mean)



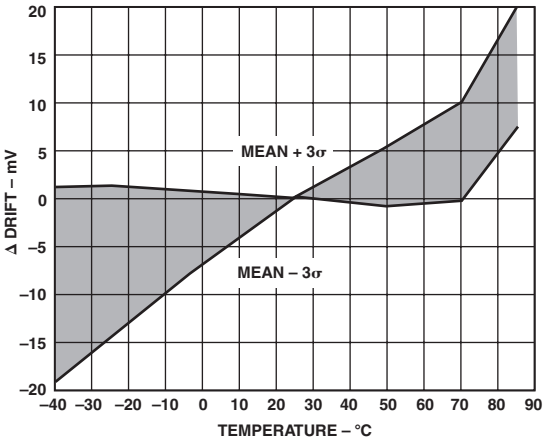
TPC 20. Law Conformance Error Distribution (3σ to Either Side of Mean)



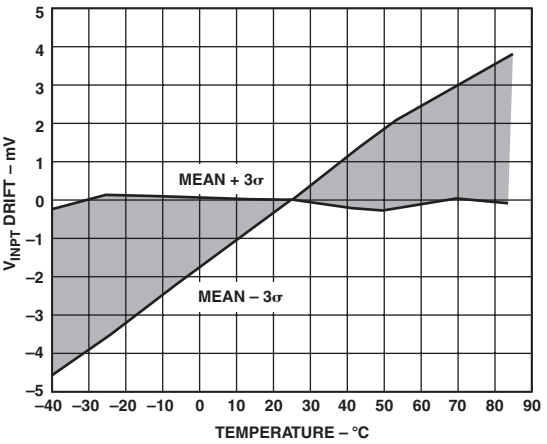
TPC 21. Law Conformance Error Distribution (3σ to Either Side of Mean)



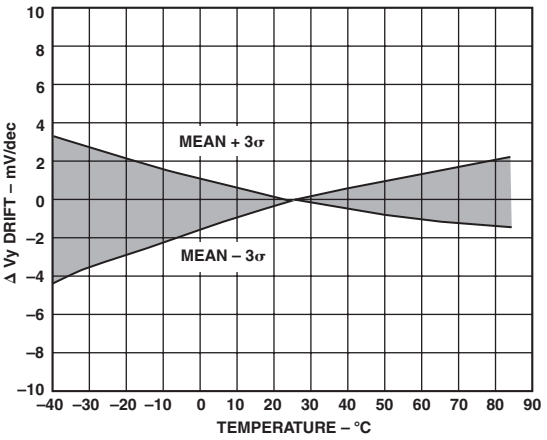
TPC 22. V_{REF} Drift vs. Temperature (3σ to Either Side of Mean)



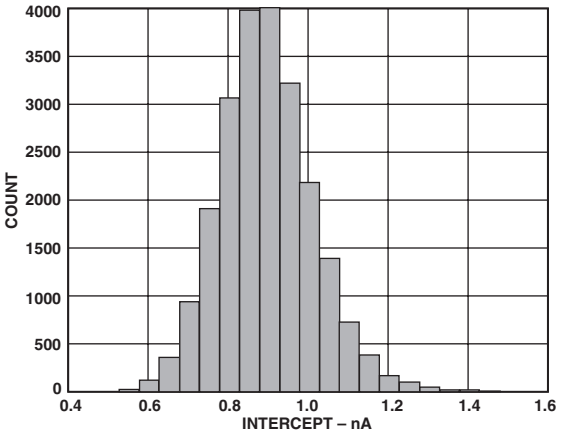
TPC 23. V_{REF} – V_{IREF} Drift vs. Temperature (3σ to Either Side of Mean)



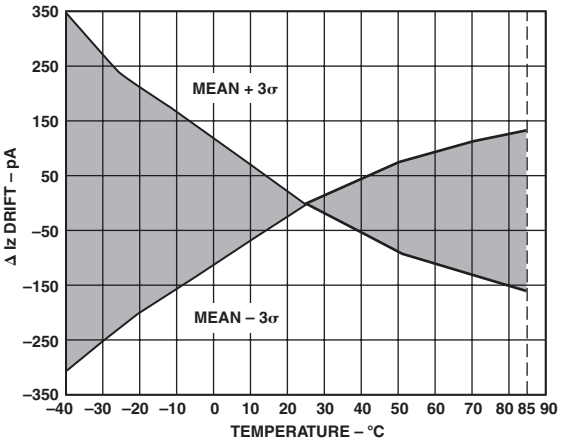
TPC 24. V_{INPT} Drift vs. Temperature (3σ to Either Side of Mean)



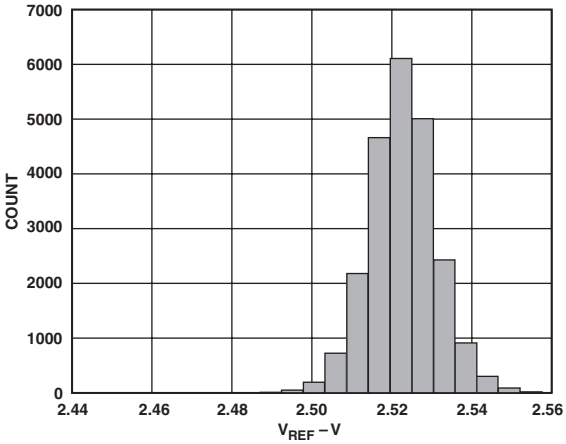
TPC 25. Slope Drift vs. Temperature (3σ to Either Side of Mean of 200 mV/decade)



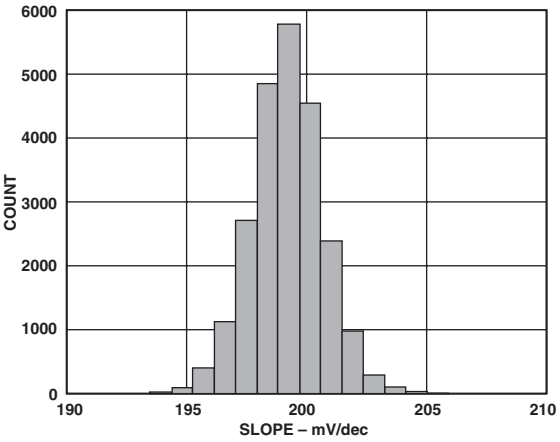
TPC 28. Distribution of Logarithmic Intercept (Nominally 1 nA when R_{REF} = 200 kΩ ± 0.1%) Sample >22,000



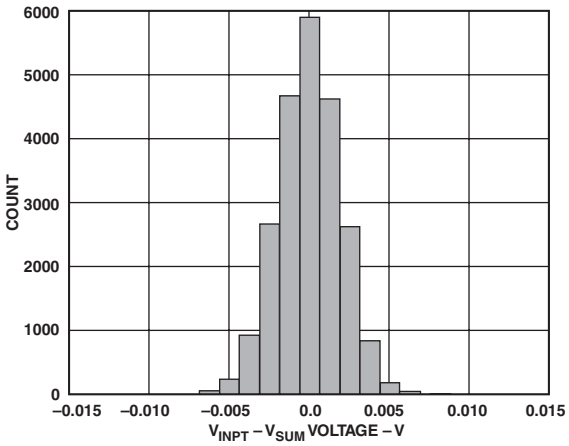
TPC 26. Intercept Drift vs. Temperature (3σ to Either Side of Mean of 1 nA)



TPC 29. Distribution of V_{REF} (R_L = 100 kΩ) Sample >22,000



TPC 27. Distribution of Logarithmic Slope (Nominally 200 mV/decade) Sample >22,000



TPC 30. Distribution of Offset Voltage (V_{INPT} – V_{SUM}) Sample >22,000

GENERAL STRUCTURE

The AD8305 addresses a wide variety of interfacing conditions to meet the needs of fiber optic supervisory systems, and will also be useful in many nonoptical applications. These notes explain the structure of this unique style of translinear log amp. Figure 1 is a simplified schematic showing the key elements.

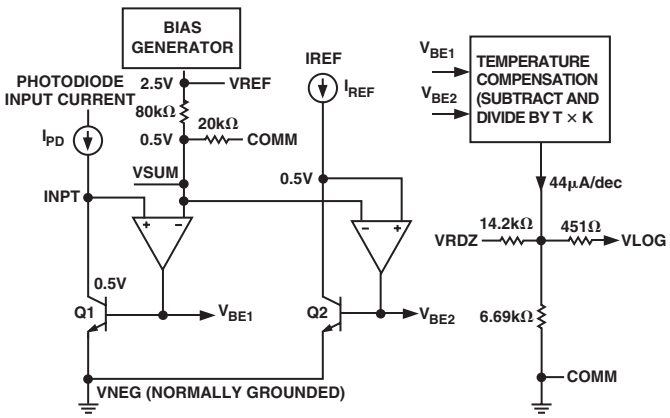


Figure 1. Simplified Schematic

The photodiode current I_{PD} is received at Pin INPT. The voltage at this node is essentially equal to those on the two adjacent guard pins, VSUM and IREF, due to the low offset voltage of the JFET op amp. Transistor Q1 converts the input current I_{PD} to a corresponding logarithmic voltage, as shown in Equation 1. A finite positive value of V_{SUM} is needed to bias the collector of Q1 for the usual case of a single-supply voltage. This is internally set to 0.5 V, that is, one fifth of the reference voltage of 2.5 V appearing on Pin VREF. The resistance at the VSUM pin is nominally 16 kΩ; this voltage is not intended as a general bias source.

The AD8305 also supports the use of an optional negative supply voltage, V_N, at Pin VNEG. When V_N is –0.5 V or more negative, VSUM may be connected to ground; thus INPT and IREF assume this potential. This allows operation as a voltage-input logarithmic converter by the inclusion of a series resistor at either or both inputs. Note that the resistor setting I_{REF} will need to be adjusted to maintain the intercept value. It should also be noted that the collector-emitter voltages of Q1 and Q2 are now the full V_N, and effects due to self-heating will cause errors at large input currents.

The input dependent V_{BE1} of Q1 is compared with the reference V_{BE2} of a second transistor, Q2, operating at I_{REF}. This is generated externally, to a recommended value of 10 μA. However, other values over a several-decade range can be used with a slight degradation in law conformance (TPC 1).

Theory

The base-emitter voltage of a BJT (bipolar junction transistor) can be expressed by Equation 1, which immediately shows its basic logarithmic nature:

$$V_{BE} = kT/q\,In\left(I_C/I_S\right) \tag{1}$$

where I_C is its collector current, I_S is a scaling current, typically only 10^{-17} A, and kT/q is the thermal voltage, proportional to absolute temperature (PTAT) and is 25.85 mV at 300 K. The current, I_S, is never precisely defined and exhibits an even stronger temperature dependence, varying by a factor of roughly a billion between –35°C and +85°C. Thus, to make use of the BJT as an accurate logarithmic element, both of these temperature dependencies must be eliminated.

The difference between the base-emitter voltages of a matched pair of BJTs, one operating at the photodiode current I_{PD} and the second operating at a reference current I_{REF}, can be written as:

$$\begin{aligned} V_{BE1} - V_{BE2} &= kT/q\ In\left(I_C/I_S\right) - kT/q\ In\left(I_{REF}/I_S\right) \\ &= In\left(10\right)kT/q\log_{10}\left(I_{PD}/I_{REF}\right) \\ &= 59.5\,mV\log_{10}\left(I_{PD}/I_{REF}\right)\left(T = 300\ K\right) \end{aligned} \tag{2}$$

The uncertain and temperature dependent saturation current I_S, which appears in Equation 1, has thus been eliminated. To eliminate the temperature variation of kT/q, this difference voltage is processed by what is essentially an analog divider. Effectively, it puts a variable under Equation 2. The output of this process, which also involves a conversion from voltage-mode to current-mode, is an intermediate, temperature-corrected current:

$$I_{LOG} = I_Y \log_{10}\left(I_{PD}/I_{REF}\right) \tag{3}$$

where I_Y is an accurate, temperature-stable scaling current that determines the slope of the function (the change in current per decade). For the AD8305, I_Y is 44 μA, resulting in a temperature-independent slope of 44 μA/decade, for all values of I_{PD} and I_{REF}. This current is subsequently converted back to a voltage-mode output, V_{LOG}, scaled 200 mV/decade.

It is apparent that this output should be zero for $I_{PD} = I_{REF}$, and would need to swing negative for smaller values of input current. To avoid this, I_{REF} would need to be as small as the smallest value of I_{PD}. However, it is impractical to use such a small reference current as 1 nA. Accordingly, an offset voltage is added to V_{LOG} to shift it upward by 0.8 V when Pin VRDZ is directly connected to VREF. This has the effect of moving the intercept to the left by four decades, from 10 μA to 1 nA:

$$I_{LOG} = I_Y \log_{10}\left(I_{PD}/I_{INTC}\right) \tag{4}$$

where I_{INTC} is the operational value of the intercept current. To disable this offset, Pin VRDZ should be grounded, then the intercept I_{INTC} is simply I_{REF}. Since values of $I_{PD} < I_{INTC}$ result in a negative V_{LOG}, a negative supply of sufficient value is required to accommodate this situation (discussed later).

The voltage V_{LOG} is generated by applying I_{LOG} to an internal resistance of 4.55 kΩ, formed by the parallel combination of a 6.69 kΩ resistor to ground and the 14.2 kΩ resistor to the VRDZ pin. When the VLOG pin is unloaded and the intercept repositioning is disabled by grounding VRDZ, the output current I_{LOG} generates a voltage at the VLOG pin of:

$$\begin{aligned} V_{LOG} &= I_{LOG} \times 4.55\ \mathrm{k}\Omega \\ &= 44\ \mu A \times 4.55\ \mathrm{k}\Omega \times \log_{10}\left(I_{PD}/I_{REF}\right) \\ &= V_Y \log_{10}\left(I_{PD}/I_{REF}\right) \end{aligned} \tag{5}$$

where V_Y = 200 mV/decade, or 10 mV/dB. Note that any resistive loading on VLOG will lower this slope and also result in an overall scaling uncertainty due to the variability of the on-chip resistors. Consequently, this practice is not recommended.

V_{LOG} may also swing below ground when dual supplies (V_P and V_N) are used. When V_N = –0.5 V or larger, the input pins INPT and IREF may now be positioned at ground level by simply grounding VSUM.

Managing Intercept and Slope

When using a single supply, VRDZ should be directly connected to VREF to allow operation over the entire five-decade input current range. As noted previously, this introduces an accurate offset voltage of 0.8 V at the VLOG pin, equivalent to four decades, resulting in a logarithmic transfer function that can be written as:

$$\begin{aligned} V_{LOG} &= V_Y \log_{10}\left(10^4 \times I_{PD}/I_{REF}\right) \\ &= V_Y \log_{10}\left(I_{PD}/I_{INTC}\right) \end{aligned} \quad (6)$$

where $I_{INTC} = I_{REF}/10^4$

Thus, the effective intercept current I_{INTC} is only one ten-thousandth of I_{REF}, corresponding to 1 nA when using the recommended value of I_{REF} = 10 μA.

The slope can be reduced by attaching a resistor to the VLOG pin. This is strongly discouraged, in view of the fact that the on-chip resistors will not ratio correctly to the added resistance. Also, it is rare that one would want to lower the basic slope of 10 mV/dB; if this is needed, it should be effected at the low impedance output of the buffer, which is provided to avoid such miscalibration and also allow higher slopes to be used.

The AD8305 buffer is essentially an uncommitted op amp with rail-to-rail output swing, good load-driving capabilities and a unity-gain bandwidth of >12 MHz. In addition to allowing the introduction of gain, using standard feedback networks and thereby increasing the slope voltage V_Y, the buffer can be used to implement multipole low-pass filters, threshold detectors, and a variety of other functions. Further details of these can be found in the AD8304 data sheet.

Response Time and Noise Considerations

The response time and output noise of the AD8305 are fundamentally a function of the signal current I_{PD}. For small currents, the bandwidth is proportional to I_{PD}, as shown in TPC 13. The output low frequency voltage-noise spectral-density is a function of I_{PD} (TPC 15) and also increases for small values of I_{REF}. Details of the noise and bandwidth performance of translinear log amps can be found in the AD8304 Data Sheet.

APPLICATIONS

The AD8305 is easy to use in optical supervisory systems and in similar situations where a wide ranging current is to be converted to its logarithmic equivalent, which is represented in decibel terms. Basic connections for measuring a single-current input are shown in Figure 2, which also includes various nonessential components, as will be explained.

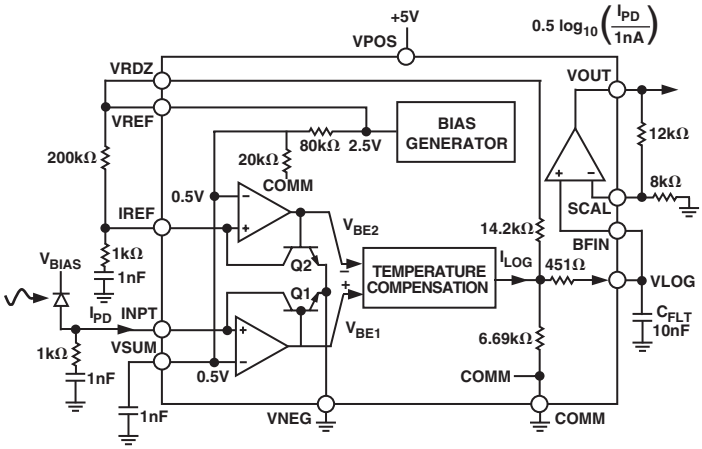


Figure 2. Basic Connections for Fixed Intercept Use

The 2 V difference in voltage between the VREF and INPT pins in conjunction with the external 200 kΩ resistor R_{REF} provide a reference current I_{REF} of 10 μA into Pin IREF. Connecting pin VRDZ to VREF raises the voltage at VLOG by 0.8 V, effectively lowering the intercept current I_{INTC} by a factor of 104 to position it at 1 nA. A wide range of other values for I_{REF}, from under 100 nA to over 1 mA, may be used. The effect of such changes is shown in TPC 3.

Any temperature variation in R_{REF} must be taken into account when estimating the stability of the intercept. Also, the overall noise will increase when using very low values of I_{REF}. In fixed-intercept applications, there is little benefit in using a large reference current, since this only compresses the low current end of the dynamic range when operated from a single supply, here shown as 5 V. The capacitor between VSUM and ground is recommended to minimize the noise on this node and to help provide a clean reference current.

Since the basic scaling at VLOG is 0.2 V/decade, and thus a swing of 4 V at the buffer output would correspond to 20 decades, it will often be useful to raise the slope to make better use of the rail-to-rail voltage range. For illustrative purposes, the circuit in Figure 2 provides an overall slope of 0.5 V/decade (25 mV/dB). Thus, using I_{REF} = 10 μA, V_{LOG} runs from 0.2 V at I_{PD} = 10 nA to 1.4 V at I_{PD} = 1 mA while the buffer output runs from 0.5 V to 3.5 V, corresponding to a dynamic range of 120 dB (electrical, that is, 60 dB optical power).

The optional capacitor from VLOG to ground forms a single-pole low-pass filter in combination with the 4.55 kΩ resistance at this pin. For example, using a C_{FLT} of 10 nF, the –3 dB corner frequency is 3.5 kHz. Such filtering is useful in minimizing the output noise, particularly when I_{PD} is small. Multipole filters are more effective in reducing the total noise; examples are provided in the AD8304 data sheet.

The dynamic response of this overall input system is influenced by the external RC networks connected from the two inputs (INPT, IREF) to ground. These are required to stabilize the input systems over the full current range. The bandwidth changes with the input current due to the widely varying pole frequency. The RC network adds a zero to the input system to ensure stability over the full range of input current levels. The network values shown in Figure 2 will usually suffice, but some experimentation may be necessary when the photodiode capacitance is high.

Although the two current inputs are similar, some care is needed to operate the reference input at extremes of current (<100 nA) and temperature (<0°C). Modifying the RC network to 4.7 nF and 2 kΩ will allow operation to –40°C at 10 nA. By inspecting the transient response to perturbations in I_{REF} at representative current levels, the capacitor value can be adjusted to provide fast rise and fall times with acceptable settling. To fine tune the network zero, the resistor value should be adjusted.

CALIBRATION

The AD8305 has a nominal slope and intercept of 200 mV/decade and 1 nA, respectively. These values are untrimmed and the slope alone may vary as much as 7.5% over temperature. For this reason, it is recommended that a simple calibration be done to achieve increased accuracy.

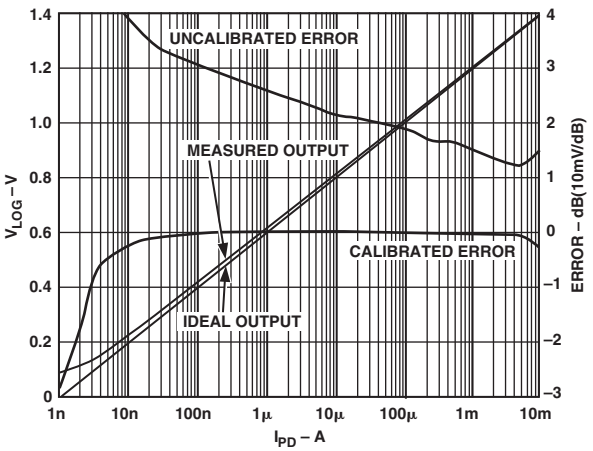


Figure 3. Using Two-Point Calibration to Increase Measurement Accuracy

Figure 3 shows the improvement in accuracy when using a two-point calibration method. To perform this calibration, apply two known currents, I_1 and I_2, in the linear operating range between 10 nA and 1 mA. Measure the resulting output, V_1 and V_2, respectively, and calculate the slope m and intercept b.

$$m = (V_1 - V_2) / [\log_{10}(I_1) - \log_{10}(I_2)] \quad (7)$$

$$b = V_1 - m \times \log_{10}(I_1) \quad (8)$$

The same calibration could be performed with two known optical powers, P_1 and P_2. This allows for calibration of the entire measurement system while providing a simplified relationship between the incident optical power and V_{LOG} voltage.

$$m = (V_1 - V_2) / (P_1 - P_2) \quad (9)$$

$$b = V_1 - m \times P_1 \quad (10)$$

The Uncalibrated Error line in Figure 3 was generated assuming that the slope of the measured output was 200 mV/decade when in fact it was actually 194 mV/decade. Correcting for this discrepancy decreased measurement error up to 3 dB.

USING A NEGATIVE SUPPLY

Most applications of the AD8305 require only a single supply of 3.0 V to 5.5 V. However, to provide further versatility, dual supplies may be employed, as illustrated in Figure 4.

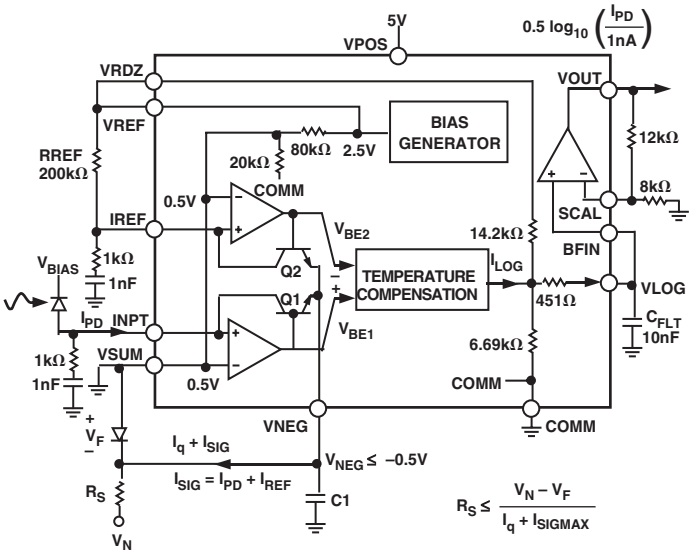


Figure 4. Negative Supply Application

The use of a negative supply, V_N, allows the summing node to be placed at ground level whenever the input transistor (Q1 in Figure 1) has a sufficiently negative bias on its emitter. When V_{NEG} = –0.5 V, the V_{CE} of Q1 and Q2 will be the same as for the default case when VSUM is grounded. This bias need not be accurate, and a poorly defined source can be used. The source does however need to be able to support the quiescent current as well as the INPT and IREF signal current. For example, it may be convenient to utilize a forward-biased junction voltage of about 0.7 V or a Schottky barrier voltage of a little over 0.5 V. The effect of supply on the dynamic range and accuracy can be seen in TPC 8.

With the summing node at ground, the AD8305 may now be used as a voltage-input log amp at either the numerator input, INPT, or the denominator input, IREF, by inserting a suitably scaled resistor from the voltage source to the relevant pin. The overall accuracy for small input voltages is limited by the voltage offset at the inputs of the JFET op amps.

The use of a negative supply also allows the output to swing below ground, thereby allowing the intercept to correspond to a midrange value of I_{PD}. However, the voltage V_{LOG} remains referenced to the ACOM pin, and while it does not swing negative for default operating conditions, it is free to do so. Thus, adding a resistor from VLOG to the negative supply lowers all values of VLOG, which raises the intercept. The disadvantage of this method is that the slope is reduced by the shunting of the external resistor, and the poorly defined ratio of on-chip and off-chip resistances causes errors in both the slope and the intercept.

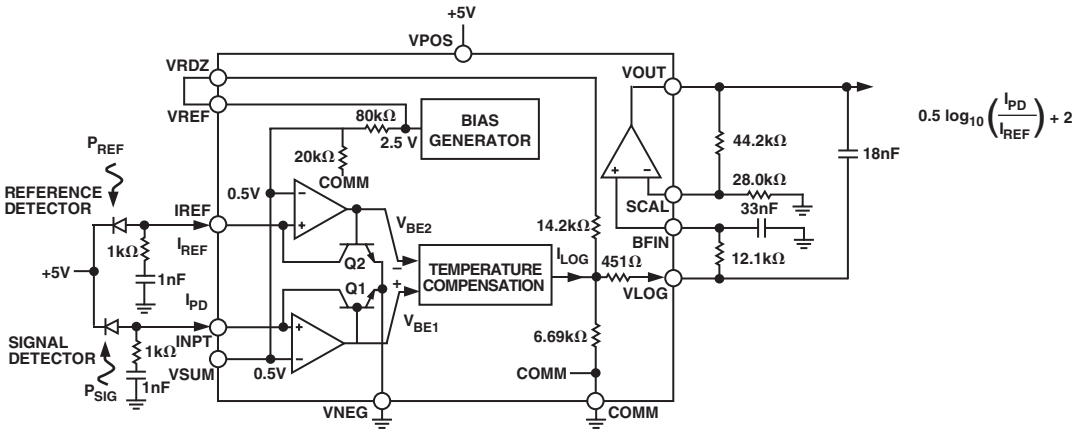


Figure 5. Optical Absorbance Measurement

LOG-RATIO APPLICATIONS

It is often desirable to determine the ratio of two currents, for example, in absorbance measurements. These are commonly used to assess the attenuation of a passive optical component, such as an optical filter or variable optical attenuator. In these situations, a reference detector is used to measure the incident power entering the component. The exiting power is then measured using a second detector and the ratio is calculated to determine the attenuation factor. Since the AD8305 is fundamentally a ratiometric device, having nearly identical logging systems for both numerator and denominator (I_{PD} and I_{REF}, respectively), it can greatly simplify such measurements.

Figure 5 illustrates the AD8305's log-ratio capabilities in optical absorbance measurements. Here a reference detector diode is used to provide the reference current, I_{REF}, proportional to the optical reference power level. A second detector measures the transmitted signal power, proportional to I_{PD}. The AD8305 calculates the logarithm of the ratio of these two currents, as shown in Equation 11, and which is reformulated in power terms in Equation 12. Both of these equations include the internal factor of 10,000 introduced by the output offset applied to V_{LOG} via pin VRDZ. If the true (nonoffset) log ratio shown in Equation 4 is preferred, VRDZ should be grounded to remove the offset. As already noted, the use of a negative supply at Pin VNEG will allow both V_{LOG} and the buffer output to swing below ground, and also allow the input pins INPT and IREF to be set to ground potential. Thus, the AD8305 may also be used to determine the log ratio of two voltages.

Figure 5 also illustrates how a second order Sallen-Key low-pass filter can be realized using two external capacitors and one resistor. Here, the corner frequency is set to 1 kHz and the filter Q is chosen to provide an optimally flat (overshoot-free) pulse response. To scale this frequency either up or down, simply scale the capacitors by the appropriate factor. Note that one of the resistors needed to realize this filter is the output resistance of 4.55 kΩ present at Pin VLOG. While this will not ratio exactly to the external resistor, which may slightly alter the Q of the filter, the effect on pulse response will be negligible for most purposes. Note that the gain of the buffer (×2.5) is an integral part of this illustrative filter design; in general, the filter may be redesigned for other closed-loop gains.

The transfer characteristics can be expressed in terms of optical power. If we assume that the two detectors have equal responsivities, the relationship is

$$V_{OUT} = 0.5\,V \log_{10}\left(10^4 \times P_{SIG}/P_{REF}\right) \tag{11}$$

Using the identity $\log_{10}(AB) = \log_{10}A + \log_{10}B$ and defining the attenuation as $-10 \times \log_{10}(P_{SIG}/P_{REF})$, the overall transfer characteristic can be written as

$$V_{OUT} = 2 - 50\,mV/dB \times \alpha \tag{12}$$

where $\alpha = -10 \times \log_{10}(P_{SIG}/P_{REF})$

Figure 6 illustrates the linear-in-dB relationship between the absorbance and the output of the circuit in Figure 5.

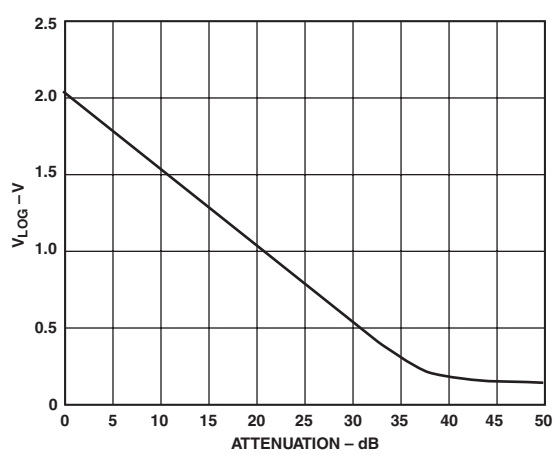


Figure 6. Example of an Absorbance Transfer Function

REVERSING THE INPUT POLARITY

Some applications may require interfacing to a circuit that sources current rather than sinks current, such as connecting to the cathode side of a photodiode. Figure 7 shows the use of a current mirror circuit. This allows for simultaneous monitoring of the optical power at the cathode, and a data recovery path using a transimpedance amplifier at the anode. The modified Wilson mirror provides a current gain very close to unity and a high output resistance. Figure 8 shows measured transfer function and law conformance performance of the AD8305 in conjunction with this current mirror interface.

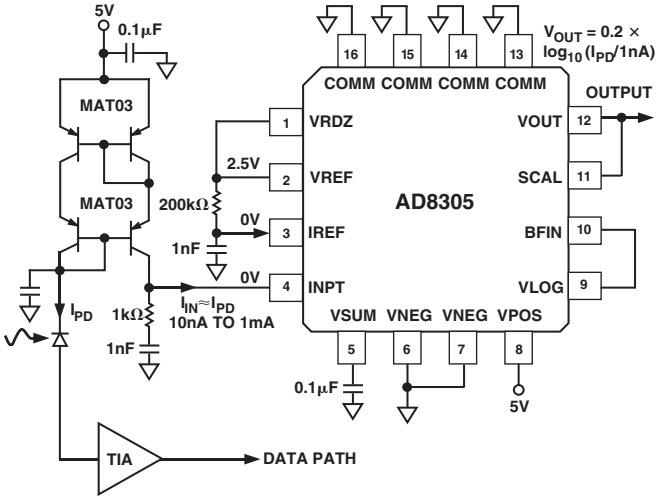


Figure 7. Wilson Current Mirror for Cathode Interfacing

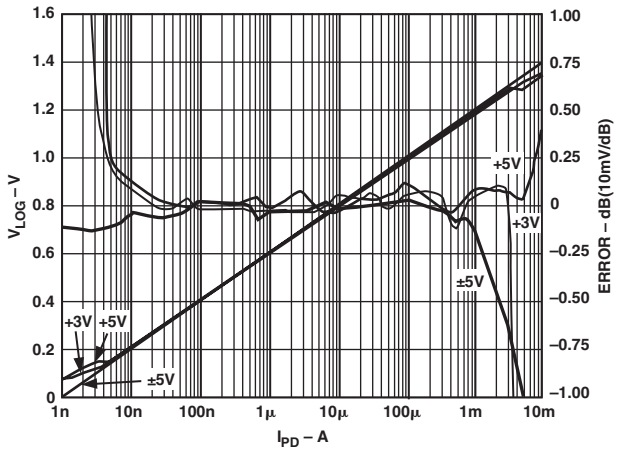


Figure 8. Log Output and Error Using Current Mirror with Various Supplies

CHARACTERIZATION METHODS

During the characterization of the AD8305, the device was treated as a precision current-input logarithmic converter, since it is not practical for several reasons to generate accurate photocurrents by illuminating a photodiode. The test currents were generated either by using well calibrated current sources, such as the Keithley 236, or by using a high value resistor from a voltage source to the input pin. Great care is needed when using very small input currents. For example, the triax output connection from the current generator was used with the guard tied to VSUM. The input trace on the PC board was guarded by connecting adjacent traces to VSUM.

These measures are needed to minimize the risk of leakage current paths. With 0.5 V as the nominal bias on the INPT pin, a leakage-path resistance of 1 GΩ to ground would subtract 0.5 nA from the input, which amounts to an error of –0.44 dB for a source current of 10 nA. Additionally, the very high output resistance at the input pins and the long cables commonly needed during characterization allow 60 Hz and RF emissions to introduce substantial measurement errors. Careful guarding techniques are essential to reduce the pickup of these spurious signals.

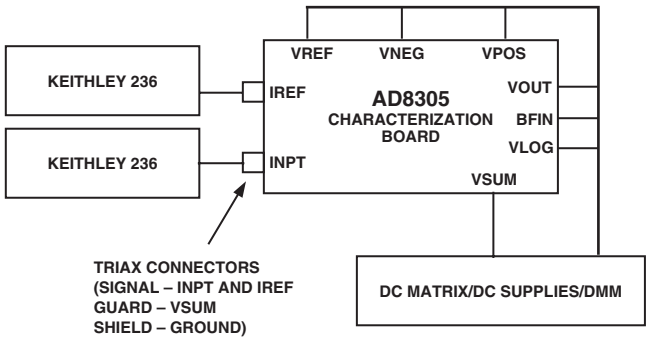


Figure 9. Primary Characterization Setup

The primary characterization setup shown in Figure 9 is used to measure V_{REF}, the static (dc) performance, logarithmic conformance, slope and intercept, the voltages appearing at pins VSUM, INPT and IREF, and the buffer offset and V_{REF} drift with temperature. To ensure stable operation over the full current range of I_{REF} and temperature extremes, filter components of C1 = 4.7 nF and R13 = 2 kΩ are used at pin to IREF ground. In some cases, a fixed resistor between pins VREF and IREF was used in place of a precision current source. For the dynamic tests, including noise and bandwidth measurements, more specialized setups are required.

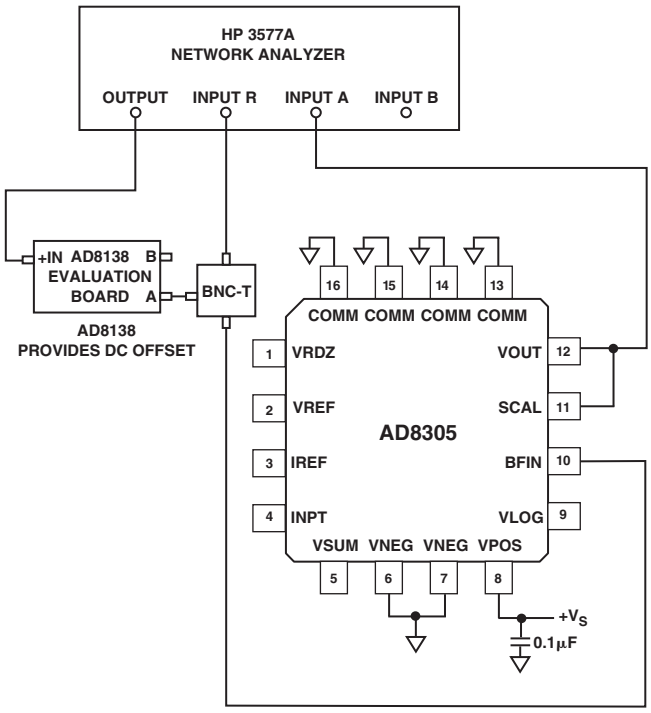


Figure 10. Configuration for Buffer Amplifier Bandwidth Measurement

Figure 10 shows the configuration used to measure the buffer amplifier bandwidth. The AD8138 evaluation board includes

provisions to offset V_{LOG} at the buffer input, allowing measurements over the full range of I_{PD} using a single supply. The network analyzer input impedances were set to 1 MΩ.

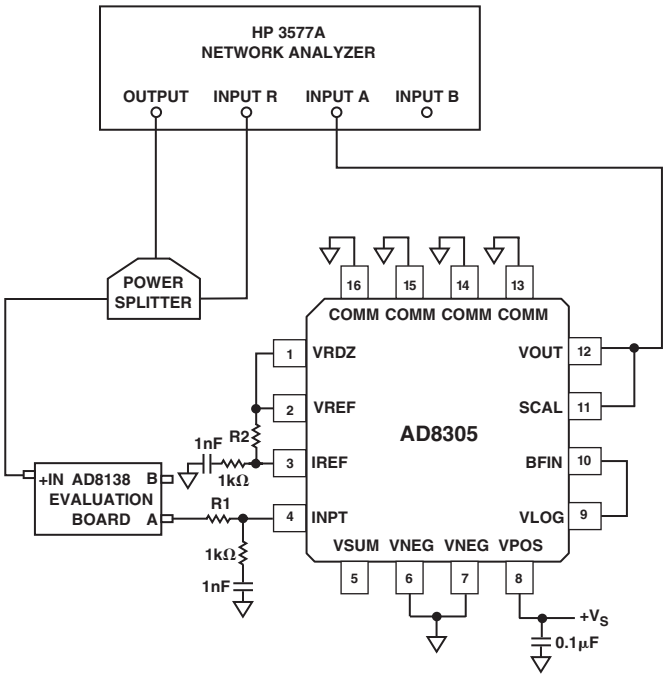


Figure 11. Configuration for Logarithmic Amplifier Bandwidth Measurement

The setup shown in Figure 11 was used for frequency response measurements of the logarithmic amplifier section. The AD8138 output is offset to 1.5 V dc and modulated to a depth of 5% at frequency. R1 is chosen (over a wide range of values up to 1.0 GΩ) to provide I_{PD}. The buffer was used to deload VLOG from the measurement system.

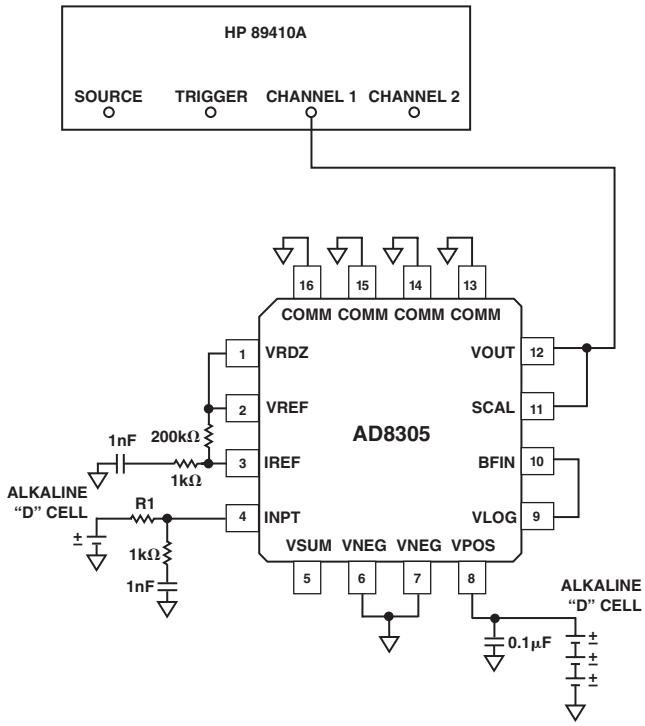


Figure 12. Configuration for Noise Spectral

The configuration in Figure 12 is used to measure the noise performance. Batteries provide both the supply voltage and the input current in order to minimize the introduction of spurious noise and ground loop effects. The entire evaluation system, including the current setting resistors, is mounted in a closed aluminum enclosure to provide additional shielding to external noise sources.

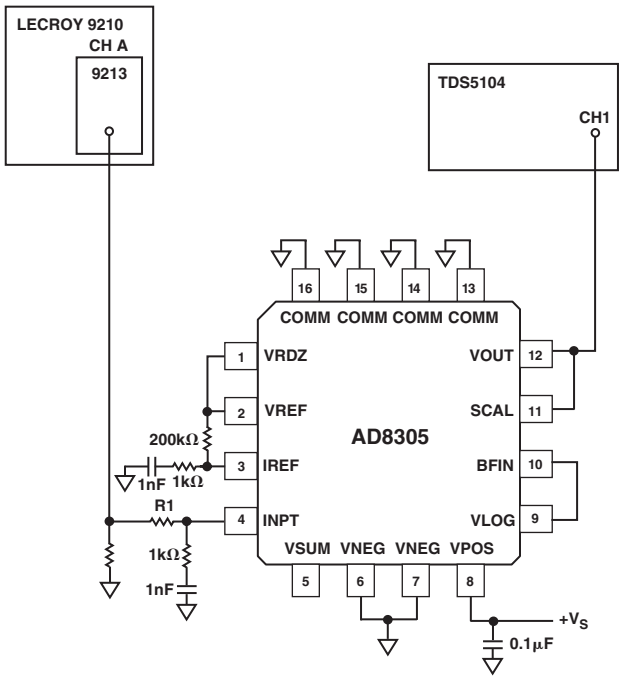


Figure 13. Configuration for Logarithmic Amplifier Pulse Response Measurement

Figure 13 shows the setup used to make the pulse response measurements. As with the bandwidth measurement, the VLOG is connected directly to BFIN and the buffer amplifier is configured for unity gain. The buffer's output is connected through a short cable to the TDS5104 scope with input impedance set to 1 MΩ. The LeCroy's output is offset to create the initial pedestal current for a given value of R1, the pulse then creates one-decade current step.

EVALUATION BOARD

An evaluation board is available for the AD8305, the schematic for which is shown in Figure 16. It can be configured for a wide variety of experiments. The buffer gain is factory-set to unity, providing a slope of 200 mV/decade, and the intercept is set to 1 nA. Table I describes the various configuration options.

Table I. Evaluation Board Configuration Options

Component	Function	Default Condition
P1	Supply Interface. Provides access to supply pins, VNEG, COMM, and VPOS.	P1 = Installed
P2, R8, R9, R10, R11, R17, R18	Monitor Interface. By adding 0 Ω resistors to R8, R9, R10, R11, R17, and R18, the VRDZ, VREF, VSUM, VOUT, and VLOG pin voltages can be monitored using a high impedance probe.	P2 = Not Installed R8 = R9 = R10 = Open (Size 0603) R17 = R18 = Open (Size 0603)
R2, R3, R4, R6, R14, C2, C7, C9, C10	Buffer Amplifier/Output Interface. The logarithmic slope of the AD8305 can be altered using the buffer's gain-setting resistors, R2 and R3. R4, R14, and C2 allow variation in the buffer loading. R6, C7, C9, and C10 are provided for a variety of filtering applications.	R2 = R6 = 0 Ω (Size 0603) R3 = R4 = Open (Size 0603) R11 = R14 = 0 Ω (Size 0603) C2 = C7 = Open (Size 0603) C9 = C10 = Open (Size 0603) VLOG = VOUT = Installed
R1, R7, R19, R20	Intercept Adjustment. The voltage dropped across resistor R1 determines the intercept reference current, nominally set to 10 μA using a 200 kΩ 1% resistor. R7 and R19 can be used to adjust the output-offset voltage at the VLOG output.	R1 = 200 kΩ (Size 0603) R7 = R19 = 0 Ω (Size 0603) R20 = Open (Size 0603)
R12, R15, C3, C4, C5, C6	Supply Decoupling.	C3 = C4 = 0.01 μF (Size 0603) C5 = C6 = 0.1 μF (Size 0603) R12 = R15 = 0 Ω (Size 0603)
C11	VSUM Decoupling Capacitor.	C11 = 1 nF (Size 0603)
R13, R16, C1, C8	Input Compensation. Provides essential HF compensation at the input pins, INPT and IREF.	R13 = R16 = 1 kΩ (Size 0603) C1 = C8 = 1 nF (Size 0603)
IREF, INPT, PD, LK1, R5	Input Interface. The test board is configured to accept a current through the SMA connector labeled INPT. An SC-style packaged photodiode can be used in place of the INPT SMA for optical interfacing. By removing R1 and adding a 0 Ω short for R5, a second current can be applied to the IREF input (also SMA) for evaluating the AD8305 in log-ratio applications.	IREF = INPT = Installed PD = Not Installed LK1 = Installed R5 = Open (Size 0603)
J1	SC-Style Photodiode. Allows for direct mounting of SC style photodiodes.	J1 = Not Installed

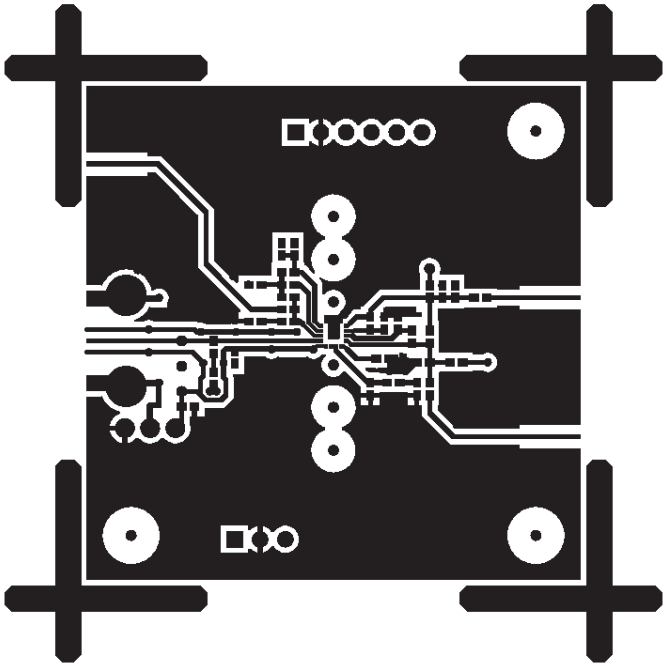


Figure 14. Component Side Layout

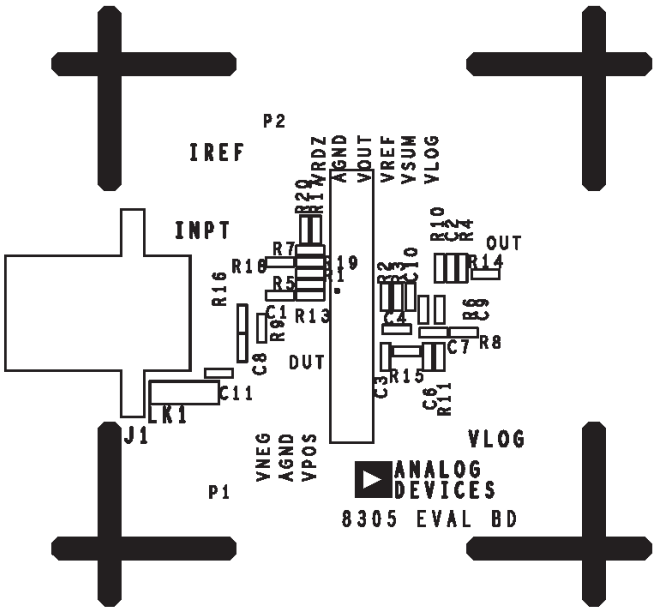


Figure 15. Component Side Silkscreen

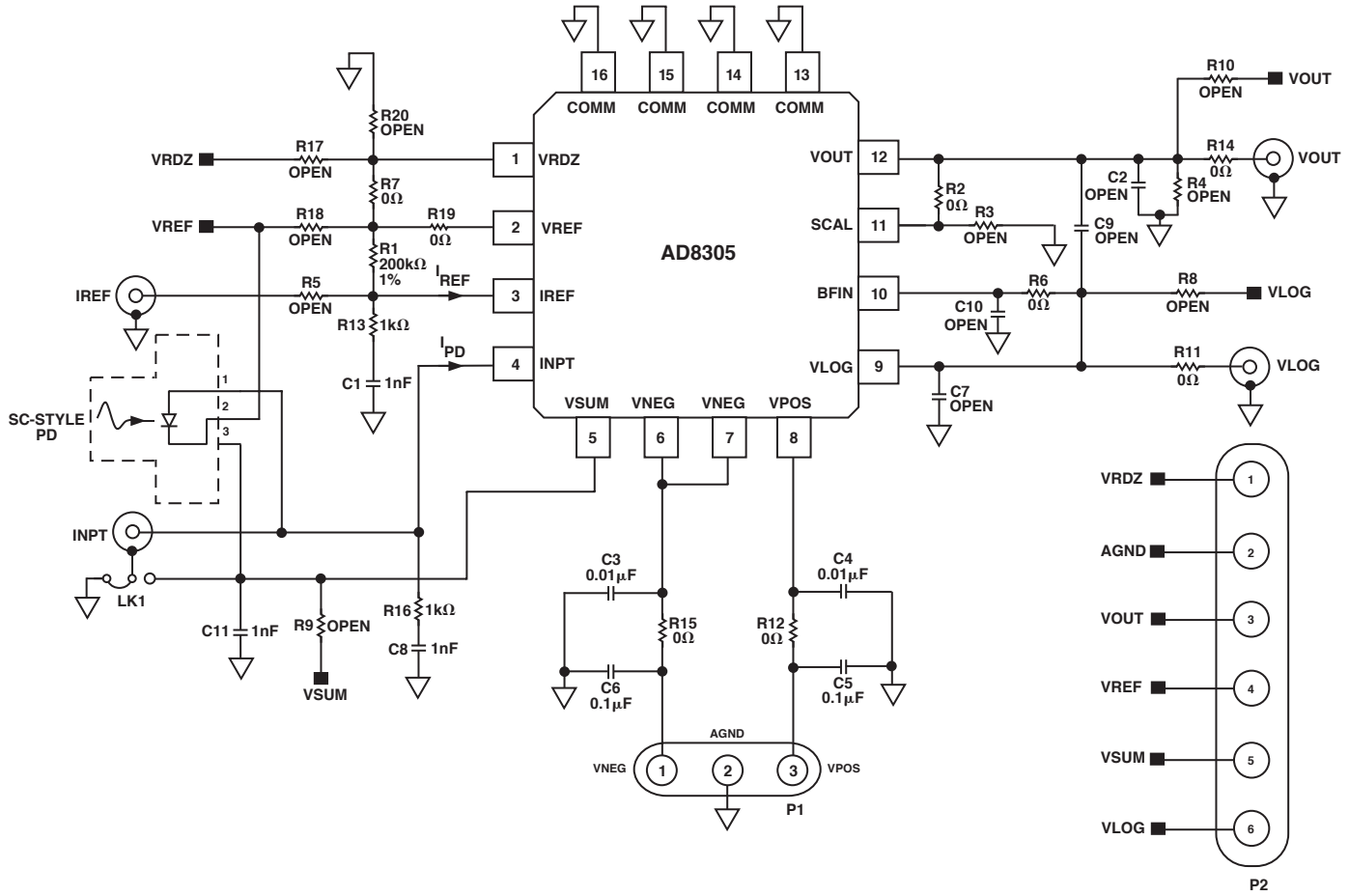
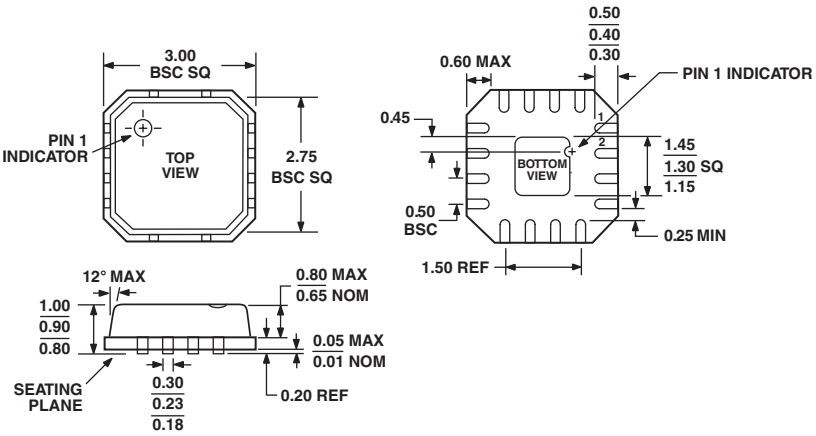


Figure 16. Evaluation Board Schematic

OUTLINE DIMENSIONS

16-Lead Leadframe Chip-Scale Package [LFCSP]
3 mm × 3 mm Body
(CP-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VEED-2

Revision History

Location	Page
3/03—Data Sheet changed from REV. 0 to REV. A.	
Changes to TPC 3	4
Changes to TPC 18	6
Changes to Figure 3	11
Changes to Figure 8	13
Updated OUTLINE DIMENSIONS	18

PRINTED IN U.S.A.

C03053–0–3/03(A)