TEXAS INSTRUMENTS
www.ti.com

SBOS421A–MARCH 2008–REVISED MARCH 2008

8-CHANNEL ANALOG FRONT-END FOR ULTRASOUND

FEATURES

- 8-Channel Complete Analog Front-End:
  - LNA, VCA, PGA, LPF, and ADC
- Ultra-Low Noise:
  - 0.85nV/√Hz (TGC)
  - 1.1nV/√Hz (CW)
- Low Power:
  - 122mW/Channel (40MSPS)
- Low-Noise Pre-Amp (LNA):
  - 20dB Fixed Gain
  - 250mV$_{PP}$ Linear Input Range
- Variable-Gain Amplifier:
  - Gain Control Range: 46dB
- PGA Gain Settings: 20dB, 25dB, 27dB, 30dB
- Low-Pass Filter:
  - Selectable BW: 10MHz, 15MHz
  - 2nd-Order
- Gain Error: ±0.5dB
- Channel Matching: ±0.8dB
- Distortion, HD2: –45dBc at 0.2V$_{PP}$ Input
- Clamping Control
- Fast Overload Recovery
- 12-Bit Analog-to-Digital Converter:
  - 10MSPS to 50MSPS
  - 69.5dB SNR at 10MHz
  - 6dB Overload Recovery Within One Clock Cycle
  - Serial LVDS Interface
  - Internal and External Reference
  - Single-Ended or Differential Clock Input
- Integrated CW Switch Matrix
- 15mm × 9mm, 135-BGA Package:
  - Pb-Free (RoHS-Compliant) and Green

APPLICATIONS

- Medical Imaging, Ultrasound
  - Portable Systems

DESCRIPTION

The AFE5805 is a complete analog front-end device specifically designed for ultrasound systems that require low power and small size.

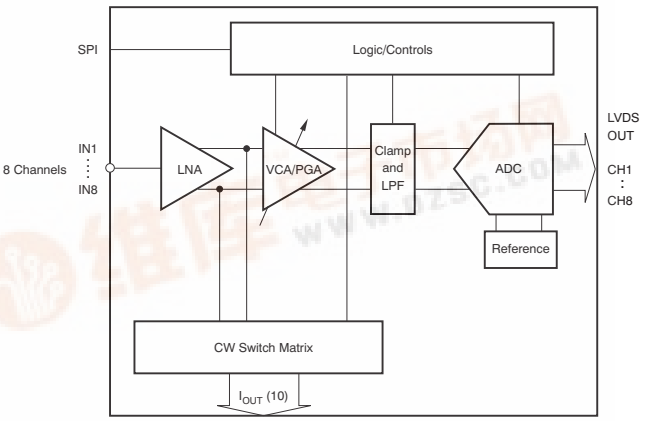
The AFE5805 consists of eight channels, including a low-noise amplifier (LNA), voltage-controlled attenuator (VCA), programmable gain amplifier (PGA), low-pass filter (LPF), and a 12-bit analog-to-digital converter (ADC) with low voltage differential signaling (LVDS) data outputs.

The LNA gain is set for 20dB gain, and has excellent noise and signal handling capabilities, including fast overload recovery. VCA gain can vary over a 46dB range with a 0V to 1.2V control voltage common to all channels of the AFE5805.

The PGA can be programmed for gains of 20dB, 25dB, 27dB, and 30dB. The internal low-pass filter can also be programmed to 10MHz or 15MHz.

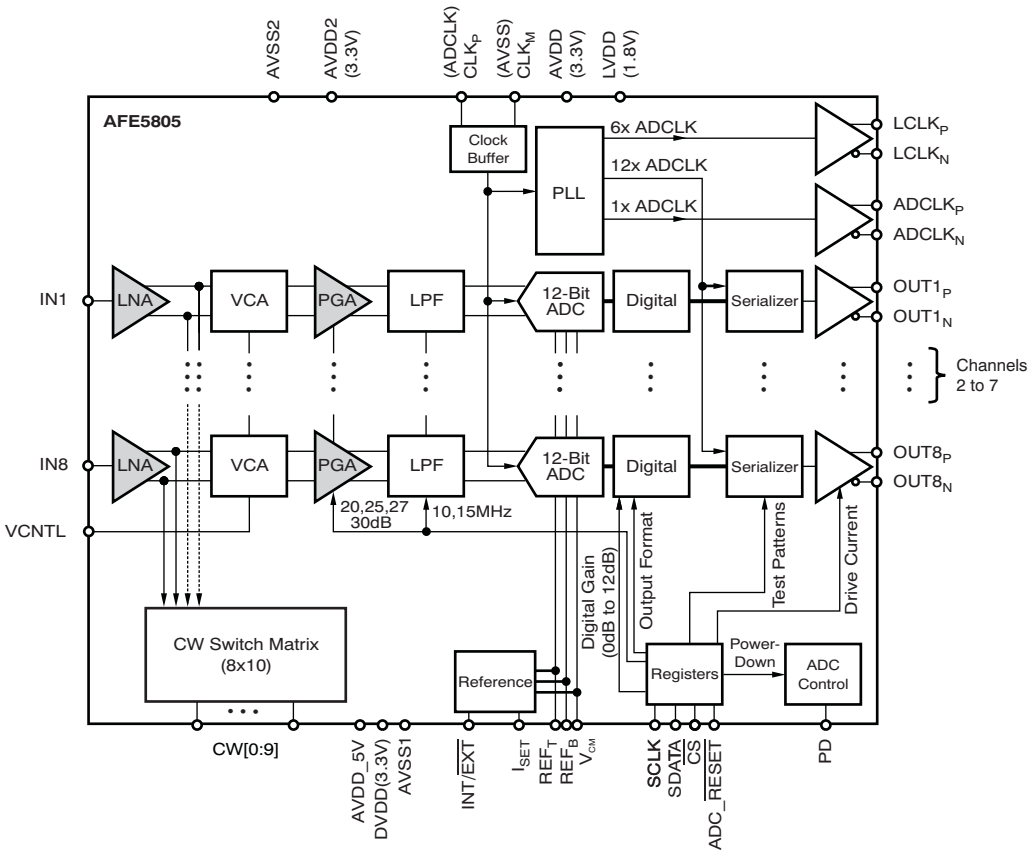
The LVDS outputs of the ADC reduce the number of interface lines to an ASIC or FPGA, thereby enabling the high system integration densities desired for portable systems. The ADC can either be operated with internal or external references. The ADC also features a signal-to-noise ratio (SNR) enhancement mode that can be useful at high gains.

The AFE5805 is available in a 15mm × 9mm, 135-ball BGA package that is Pb-free (RoHS-compliant) and green. It is specified for operation from 0°C to +70°C.



PRODUCT PREVIEW

Block Diagram



PRODUCT PREVIEW

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGING/ORDERING INFORMATION(1)(2)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	OPERATING TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY	ECO STATUS
AFE5805	µFBGA-135	ZCF	0°C to +70°C	AFE5805ZCF-R	Tape and Reel, 1000	Pb-Free, Green

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) These packages conform to Lead (Pb)-free and green manufacturing specifications. Additional details including specific material content can be accessed at www.ti.com/leadfree.
GREEN: Ti defines Green to mean Lead (Pb)-Free and in addition, uses less package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1%of total product weight. N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree. Pb-FREE: Ti defines Lead (Pb)-Free to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		AFE5805	UNIT
Supply voltage range, AVDD1		–0.3 to +3.9	V
Supply voltage range, AVDD2		–0.3 to +3.9	V
Supply voltage range, AVDD_5V		–0.3 to +6	V
Supply voltage range, DVDD		–0.3 to +3.9	V
Supply voltage range, LVDD		–0.3 to +2.2	V
Voltage between AVSS1 and LVSS		–0.3 to +0.3	V
Voltage at analog inputs		–0.3 to AVDD2 +0.3	V
External voltage applied to REFT-pin		–0.3 to +3	V
External voltage applied to REFB-pin		–0.3 to +2	V
Voltage at digital inputs		TBD	V
Peak solder temperature		TBD	°C
Maximum junction temperature, T_J any condition(2)		+150	°C
Maximum junction temperature, T_J continuous operation, long term reliability(3)		+125	°C
Storage temperature range		–40 to +125	°C
Operating temperature range		–40 to +85	°C
ESD ratings	HBM	2000	V
	CDM	500	V
	MM	TBD	V

(1) Stresses above these ratings may cause permanent damage. Exposure to *absolute maximum conditions* for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.
(2) The absolute maximum junction temperature under any condition is limited by the constraints of the silicon process.
(3) The absolute maximum junction temperature for continuous operation is limited by the package constraints. Operation above this temperature may result in reduced reliability and/or lifetime of the device.

PRODUCT PREVIEW

RECOMMENDED OPERATING CONDITIONS

PARAMETER		AFE5805 MIN	AFE5805 TYP	AFE5805 MAX	UNIT
SUPPLIES, ANALOG INPUTS, AND REFERENCE VOLTAGES					
AVDD1	Analog supply voltage	3.0	3.3	3.6	V
	AVDD2, DVDD	3.0		3.6	V
	AVDD_5V	4.75		5.25	V
LVDD	Digital supply voltage	1.7	1.8	1.9	V
	Differential input voltage range		2		V_{PP}
	Input common-mode voltage		V_{CM} ± 0.05		V
REF_T	External reference mode		2.5		V
REF_B	External reference mode		0.5		V
CLOCK INPUTS					
	CLK_M, CLK_P	10	40	50	MHz
	Input clock amplitude differential (V_{CLKP} – V_{CLKM}), peak-to-peak				
	Sine wave, ac-coupled		3.0		V_{PP}
	LVPECL, ac-coupled		1.6		V_{PP}
	LVDS, ac-coupled		0.7		V_{PP}
	Input clock CMOS, single-ended (V_{CLKP})				
	V_{IL}			0.6	V
	V_{IH}	2.2			V
	Input clock duty cycle		50		%
DIGITAL OUTPUTS					
	$ADCLK_P$ and $ADCLK_N$ outputs (LVDS)	10	1x (sample rate)	50, 65	MHz
	$LCLK_P$ and $LCLK_N$ outputs (LVDS)	60	6x (sample rate)	300, 390	MHz
C_{LOAD}	Maximum external capacitance from each pin to LVSS		5		pF
R_{LOAD}	Differential load resistance between the LVDS output pairs		100		Ω
T_A	Ambient temperature	0		+70	°C

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, –1dBFS input magnitude, internal reference mode, I_{SET} = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE5805			UNIT
			MIN	TYP	MAX	
PREAMPLIFIER (LNA)						
Gain	A	SE-input to differential output		20		dB
Input voltage	V_{IN}	Linear operation (HD2 ≤ 40dB)		250		mV_{PP}
Maximum input voltage		Limited by internal diodes		600		mV_{PP}
Input voltage noise (TGC)	e_n (RTI)	R_S = 0Ω, f = 1MHz		0.75		nV/√Hz
Input current noise	i_n (RTI)			3		pA/√Hz
Common-mode voltage, input	V_{CMI}	Internally generated		2.4		V
Bandwidth	BW	Small-signal, –3dB		70		MHz
Input resistance	R_{IN}			8		kΩ
Input capacitance	C_{IN}	Includes internal diodes		30		pF
FULL-SIGNAL CHANNEL (LNA+VCA+LPF+ADC)						
Input voltage noise (TGC)	e_n	R_S = 0Ω, f = 1MHz, PGA = 30dB		0.85		nV/√Hz
		R_S = 0Ω, f = 1MHz, PGA = 20dB		0.95		nV/√Hz
Noise figure	NF	R_S = x		TBD		dB
Low-pass flter bandwidth	LPF	at –3dB, selectable through SPI		10, 15		MHz
Bandwidth tolerance				±15		%
High-pass filter	HPF	(First-order, due to internal ac-coupling)		200		kHz
Group delay variation				TBD		ns
Overload recovery				TBD		Clock Cycle
DC-ACCURACY						
Gain (PGA)		Selectable through SPI		20, 25, 27, 30		dB
Total gain, max[1]		LNA + PGA gain		50		dB
Gain range		V_{CNTL} = 0V to 1.2V	TBD	46	TBD	dB
Gain error[2]		0V < V_{CNTL} < 0.1V		TBD		dB
		0.1V < V_{CNTL} < 1.1V (= linear range)		±0.5	±1.0	dB
		1.1V < V_{CNTL} < 1.2V		TBD		dB
Gain matching, channel-to-channel		0.1V < V_{CNTL} < 1.1V		±0.5	±1.0	dB
Gain drift (tempco)				TBD		ppm/°C
Offset error		V_{CNTL} = TBD, gain = TBD		TBD		mV (LSB)
Offset drift (tempco)				TBD		ppm/°C
GAIN CONTROL (VCA)						
Input voltage range	V_{CNTL}			0 to 1.2		V
Gain slope		V_{CNTL} = 0.1V to 1.1V		40		dB/V
Input resistance				25		kΩ
Response time		V_{CNTL} = 0V to 1.2V step; to 90% signal		TBD		µs
DYNAMIC PERFORMANCE						
Signal-to-noise ratio	SNR	F_{IN} = 2MHz; –1dBFS (V_{CNTL} = TBD, PGA = TBD)		TBD		dBFS
		F_{IN} = 5MHz; –1dBFS		TBD		dBFS
		F_{IN} = 10MHz; –1dBFS		TBD		dBFS
Second-harmonic distortion	HD2	F_{IN} = 2MHz; –1dBFS (V_{CNTL} = TBD, PGA = TBD)		TBD		dBc
		F_{IN} = 5MHz; –1dBFS (V_{CNTL} = TBD, PGA = TBD)	TBD	TBD	TBD	dBc
		F_{IN} = 5MHz; –6dBFS (V_{CNTL} = TBD, PGA = TBD)	TBD	TBD	TBD	dBc

(1) Excludes digital gain within ADC.
(2) Excludes error of internal reference.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, –1dBFS input magnitude, internal reference mode, I_{SET} = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	AFE5805			UNIT
			MIN	TYP	MAX	
Third-harmonic distortion	HD3	F_{IN} = 2MHz; –1dBFS (V_{CNTL} = TBD, PGA = TBD)		TBD		dBc
		F_{IN} = 5MHz; –1dBFS (VV_{CNTL} = TBD, PGA = TBD)	TBD	TBD	TBD	dBc
		F_{IN} = 5MHz; –6dBFS (V_{CNTL} = TBD, PGA = TBD)	TBD	TBD	TBD	dBc
Total harmonic distortion	THD	F_{IN} = 2MHz; –1dBFS (VV_{CNTL} = TBD, PGA = TBD)		TBD		dBc
		F_{IN} = 5MHz; –1dBFS (VV_{CNTL} = TBD, PGA = TBD)		TBD		dBc
		F_{IN} = 10MHz; –1dBFS (V_{CNTL} = TBD, PGA = TBD)		TBD		dBc
Overload distortion		up to × dB overload		TBD		dBc
SNR + THD	SINAD	F_{IN} = 2.5MHz; –1dBFS (V_{CNTL} = TBD, PGA = TBD)		TBD		dBFS
		F_{IN} = 5MHz; –1dBFS		TBD		dBFS
		Fin = 10MHz; –1dBFS		TBD		dBFS
Intermodulation distortion	IMD	f_1 = 5Mhz at –1dBFS, f_2 = 5.01MHz at –27dBFS		TBD		dB
Crosstalk		F_{IN} = TBD, V_{IN} = TBD		TBD		dB
		(with overload input)		TBD		dB
CW - SIGNAL CHANNELS						
Input voltage noise (CW)	e_n	R_S = 0Ω, f = 1MHz		1.1		nV/√Hz
Output noise correlation factor		Summing of eight channels		TBD		%
Output transconductance (V/I)				12		mA/V
Dynamic CW output current	I_{OUTAC}			2.4 (±1.2)		mA_{PP}
Static CW output current	I_{OUTDC}			0.9		mA
Output common-mode voltage(3)	V_{CM}			2.5		V
Output impedance				50		kΩ
Output capacitance				<10		pF
INTERNAL REFERENCE VOLTAGES (ADC)						
Reference Top	$VREF_T$		TBD	0.5	TBD	
Reference Bottom	$VREF_B$		TBD	2.5	TBD	
$VREF_T$ – $VREF_B$			TBD	2	TBD	
Common-mode voltage (internal)	V_{CM}		TBD	1.5	TBD	
V_{CM} output current				±2		mA
EXTERNAL REFERENCE VOLTAGES (ADC)						
Reference top	$VREF_T$		2.4		2.6	V
Reference bottom	$VREF_B$		0.4		0.6	V
$VREF_T$ – $VREF_B$			1.9		2.1	
Switching current(4)				TBD		mA
POWER SUPPLY						
SUPPLY VOLTAGES						
AVDD1, AVDD2, DVDD		Specification	3.14	3.3	3.47	V
AVDD_5V		Specification	4.75	5	5.25	V
LVDD			1.7	1.8	1.9	V

(3) CW outputs require an externally applied bias voltage of +2.5V.
(4) Current drawn by the eight ADC channels from the external reference voltages; sourcing for $VREF_T$, sinking for $VREF_B$.

PRODUCT PREVIEW

ELECTRICAL CHARACTERISTICS (continued)

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, –1dBFS input magnitude, internal reference mode, I_{SET} = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS	AFE5805			UNIT
		MIN	TYP	MAX	
SUPPLY CURRENTS					
IAVDD1 (ADC)	at 40MSPS	TBD	TBD	TBD	mA
IAVDD2 (VCA)	TGC mode	TBD	TBD	TBD	mA
	CW mode		TBD		mA
IAVDD_5V (VCA)	TGC mode	TBD	8	TBD	mA
	CW mode		TBD		mA
IDVDD (VCA)		TBD		TBD	mA
ILVDD (ADC)	At 40MSPS	TBD	TBD	TBD	mA
Power dissipation, total	All channels, TGC mode , no signal		980	TBD	mW
	All channels, CW mode , no signal		TBD	TBD	mW
Power-supply rejection	DC power-supply rejection ratio		TBD		%FSR/V
	AC power supply rejection ratio		TBD		dBc
POWER-DOWN MODES					
Power-down dissipation, total	ADC_PD = H	TBD	TBD	TBD	mW
Power-down response time			10		µs
Power-up response time			50		µs
Power-down dissipation(5)	Standby (fast recovery mode)		TBD		mW
Power-down dissipation	No clock applied		TBD		mW
THERMAL CHARACTERISTICS					
Temperature range		0		70	°C
Thermal resistance, T_{JA}			TBD		C/W

(5) At VCA_PD pin pulled high; see also Power-Down Timing diagram.

DIGITAL CHARACTERISTICS

DC specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level '0' or '1'. At C_{LOAD} = 5pF(1), I_{OUT} = 3.5mA(2), R_{LOAD} = 100Ω(2), and no internal termination, unless otherwise noted.

PARAMETER	TEST CONDITIONS	AFE5805			UNIT
		MIN	TYP	MAX	
DIGITAL INPUTS					
High-level input voltage		1.4			V
Low-level input voltage				0.3	V
High-level input current			33		µA
Low-level input current			–33		µA
Input capacitance			3		pF
LVDS OUTPUTS					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
Output differential voltage, $\|V_{OD}\|$			350		mV
V_{OS} output offset voltage(2)	Common-mode voltage of OUT_P and OUT_N		1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

(1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(2) I_{OUT} refers to the LVDS buffer current setting; R_{LOAD} is the differential load resistance between the LVDS output pair.

PRODUCT PREVIEW

PIN CONFIGURATION

ZCF PACKAGE
135-BGA
BOTTOM VIEW

Rows	1	2	3	4	5	6	7	8	9
R	OUT4M	OUT3M	OUT2M	OUT1M	LVSS	OUT5M	OUT6M	OUT7M	OUT8M
P	OUT4P	OUT3P	OUT2P	OUT1P	LVDD	OUT5P	OUT6P	OUT7P	OUT8P
N	LCLKP	LCLKM	LVSS	LVSS	LVSS	LVDD	LVDD	FCLKM	FCLKP
M	DNC	DNC	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	DNC	DNC
L	CLKP	AVDD1	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	AVDD1	EN_SM
K	CLKM	DNC	AVDD1	DNC	AVDD1	AVDD1	AVDD1	CM	ISET
J	AVSS1	AVDD1	INT/$\overline{\text{EXT}}$	AVSS2	AVSS2	AVSS2	AVDD1	REFT	REFB
H	ADS_PD	DNC	DNC	VCA_CS	RST	SCLK	$\overline{\text{CS}}$	SDATA	ADS_$\overline{\text{RESET}}$
G	CW5	AVDD2	VCM	AVSS2	AVSS2	AVSS2	VREFL	AVDD2	CW4
F	CW6	VB1	VB5	AVSS2	AVSS2	AVSS2	VREFH	VB6	CW3
E	CW7	AVDD_5V	VB3	AVSS2	AVSS2	AVSS2	VB4	AVDD_5V	CW2
D	CW8	VCNTL	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	VB2	CW1
C	CW9	AVDD2	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	AVDD2	CW0
B	VBL1	VBL2	VBL3	VBL4	DNC	VBL8	VBL7	VBL6	VBL5
A	IN1	IN2	IN3	IN4	VCA_PD	IN8	IN7	IN6	IN5

Columns

PRODUCT PREVIEW

ZCF PACKAGE
135-BGA
CONFIGURATION MAP (TOP VIEW)

	9	8	7	6	5	4	3	2	1
R	OUT8M	OUT7M	OUT6M	OUT5M	LVSS	OUT1M	OUT2M	OUT3M	OUT4M
P	OUT8P	OUT7P	OUT6P	OUT5P	LVDD	OUT1P	OUT2P	OUT3P	OUT4P
N	FCLKP	FCLKM	LVDD	LVDD	LVSS	LVSS	LVSS	LCLKM	LCLKP
M	DNC	DNC	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	DNC	DNC
L	EN_SM	AVDD1	AVSS1	AVSS1	AVSS1	AVSS1	AVSS1	AVDD1	CLKP
K	ISET	CM	AVDD1	AVDD1	AVDD1	DNC	AVDD1	DNC	CLKM
J	REFB	REFT	AVDD1	AVSS2	AVSS2	AVSS2	INT/$\overline{EXT}$	AVDD1	AVSS1
H	ADS_$\overline{RESET}$	SDATA	$\overline{CS}$	SCLK	RST	VCA_$\overline{CS}$	DNC	DNC	ADS_PD
G	CW4	AVDD2	VREFL	AVSS2	AVSS2	AVSS2	VCM	AVDD2	CW5
F	CW3	VB6	VREFH	AVSS2	AVSS2	AVSS2	VB5	VB1	CW6
E	CW2	AVDD_5V	VB4	AVSS2	AVSS2	AVSS2	VB3	AVDD_5V	CW7
D	CW1	VB2	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	VCNTL	CW8
C	CW0	AVDD2	AVSS2	AVSS2	DVDD	AVSS2	AVSS2	AVDD2	CW9
B	VBL5	VBL6	VBL7	VBL8	DNC	VBL4	VBL3	VBL2	VBL1
A	IN5	IN6	IN7	IN8	VCA_PD	IN4	IN3	IN2	IN1

Legend:

AVDD1	+3.3V; Analog
AVDD2	+3.3V; Analog
DVDD	+3.3V; Analog
LVDD	+1.8V; Digital
AVDD_5V	+5V; Analog
AVSS1	Analog Ground
AVSS2	Analog Ground
LVSS	Digital Ground

PRODUCT PREVIEW

Table 1. TERMINAL FUNCTIONS

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
H7	$\overline{CS}$	Input	Chip select for serial interface; active low
H1	ADS_PD	Input	Power-down pin for ADS; active high
H9	ADS_$\overline{RESET}$	Input	RESET input for ADS; active low
H6	SCLK	Input	Serial clock input for serial interface
H8	SDATA	Input	Serial data input for serial interface
J2, L2, K7, J7, K3, L8, K5, K6	AVDD1	POWER	3.3V analog supply for ADS
L3, M3, L4, M4, L5, M5, L6, M6, L7, M7, J1	AVSS1	GND	Analog ground for ADS
P5, N6, N7	LVDD	POWER	1.8V digital supply for ADS
N3, N4, N5, R5	LVSS	GND	Digital ground for ADS
C5, D5	DVDD	POWER	3.3V digital supply for the VCA; connect to the 3.3V analog supply (AVDD2).
C2, C8, G2, G8	AVDD2	POWER	3.3V analog supply for VCA
E2, E8	AVDD_5V	POWER	5V supply for VCA
C3, D3, C4, D4, E4, F4, G4, E5, F5, G5, C6, D6, E6, F6, G6, C7, D7, J4, J5,J6	AVSS2	GND	Analog ground for VCA
K1	CLKM	Input	Negative clock input for ADS (connect to *Ground* in single-ended clock mode)
L1	CLKP	Input	Positive clock input for ADS
K8	CM	Input/Output	1.5V common-mode I/O for ADS. Becomes input pin in one of the external reference modes.
C9	CW0	Output	CW output 0
D9	CW1	Output	CW output 1
E9	CW2	Output	CW output 2
F9	CW3	Output	CW output 3
G9	CW4	Output	CW output 4
G1	CW5	Output	CW output 5
F1	CW6	Output	CW output 6
E1	CW7	Output	CW output 7
D1	CW8	Output	CW output 8
C1	CW9	Output	CW output 9
L9	EN_SM	Input	Enables access to the VCA register. Active high. Connect permanently to 3.3V (AVDD2).
N8	FCLKM	Output	LVDS frame clock (negative output)
N9	FCLKP	Output	LVDS frame clock (positive output)
A1	IN1	Input	LNA input Channel 1
A2	IN2	Input	LNA input Channel 2
A3	IN3	Input	LNA input Channel 3
A4	IN4	Input	LNA input Channel 4
A9	IN5	Input	LNA input Channel 5
A8	IN6	Input	LNA input Channel 6
A7	IN7	Input	LNA input Channel 7
A6	IN8	Input	LNA input Channel 8
J3	INT/$\overline{EXT}$	Input	Internal/ external reference mode select for ADS; internal = high
K9	ISET	Input	Current bias pin for ADS. Requires 56kΩ to ground.
N2	LCLKM	Output	LVDS bit clock (6x); negative output
N1	LCLKP	Output	LVDS bit clock (6x); positive output
R4	OUT1M	Output	LVDS data output (negative), Channel 1
P4	OUT1P	Output	LVDS data output (positive), Channel 1
R3	OUT2M	Output	LVDS data output (negative), Channel 2
P3	OUT2P	Output	LVDS data output (positive), Channel 2
R2	OUT3M	Output	LVDS data output (negative), Channel 3

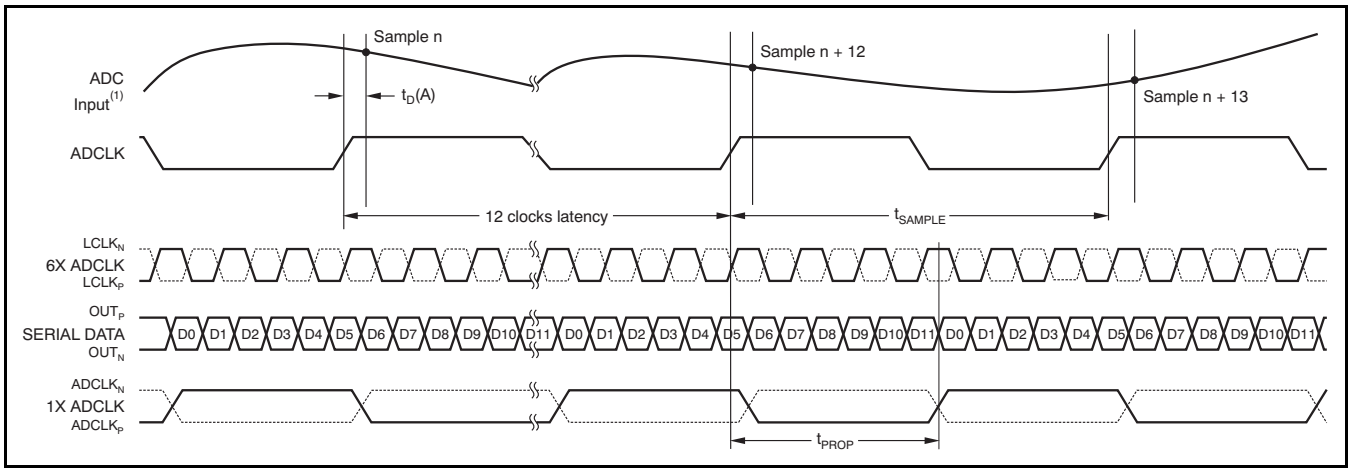
PRODUCT PREVIEW

Table 1. TERMINAL FUNCTIONS (continued)

PIN NO.	PIN NAME	FUNCTION	DESCRIPTION
P2	OUT3P	Output	LVDS data output (positive), Channel 3
R1	OUT4M	Output	LVDS data output (negative), Channel 4
P1	OUT4P	Output	LVDS data output (positive), Channel 4
R6	OUT5M	Output	LVDS data output (negative), Channel 5
P6	OUT5P	Output	LVDS data output (positive), Channel 5
R7	OUT6M	Output	LVDS data output (negative), Channel 6
P7	OUT6P	Output	LVDS data output (positive), Channel 6
R8	OUT7M	Output	LVDS data output (negative), Channel 7
P8	OUT7P	Output	LVDS data output (positive), Channel 7
R9	OUT8M	Output	LVDS data output (negative), Channel 8
P9	OUT8P	Output	LVDS data output (positive), Channel 8
J9	REFB	Input/Output	0.5V Negative reference of ADS. Decoupling to ground. Becomes input in external ref mode.
J8	REFT	Input/Output	2.5V Positive reference of ADS. Decoupling to ground. Becomes input in external ref mode.
H5	RST	Input	RESET input for VCA. Connect to the VCA_$\overline{CS}$ pin (H4).
H4	VCA_$\overline{CS}$	Output	Connect to RST–pin (H5)
F2	VB1	Output	Internal bias voltage. Bypass to ground with 2.2µF.
D8	VB2	Output	Internal bias voltage. Bypass to ground with 0.1µF.
E3	VB3	Output	Internal bias voltage. Bypass to ground with 0.1µF.
E7	VB4	Output	Internal bias voltage. Bypass to ground with 0.1µF
F3	VB5	Output	Internal bias voltage. Bypass to ground with 0.1µF.
F8	VB6	Output	Internal bias voltage. Bypass to ground with 0.1µF.
B1	VBL1	Input	Complementary LNA input Channel 1; bypass to ground with 0.1µF.
B2	VBL2	Input	Complementary LNA input Channel 2; bypass to ground with 0.1µF.
B3	VBL3	Input	Complementary LNA input Channel 3; bypass to ground with 0.1µF.
B4	VBL4	Input	Complementary LNA input Channel 4; bypass to ground with 0.1µF.
B9	VBL5	Input	Complementary LNA input Channel 5; bypass to ground with 0.1µF.
B8	VBL6	Input	Complementary LNA input Channel 6; bypass to ground with 0.1µF.
B7	VBL7	Input	Complementary LNA input Channel 7; bypass to ground with 0.1µF.
B6	VBL8	Input	Complementary LNA input Channel 8; bypass to ground with 0.1µF.
A5	VCA_PD	Input	Power-down pin for VCA; low = normal mode, high = power-down mode.
G3	VCM	Output	VCA reference voltage. Bypass to ground with 0.1µF.
D2	VCNTL	Input	VCA control voltage input
F7	VREFH	Output	Clamp reference voltage (2.0V). Bypass to ground with 0.1µF.
G7	VREFL	Output	Clamp reference voltage (2.7V). Bypass to ground with 0.1µF.
B5, H2, H3, K2, K4, M1, M2, M8, M9	DNC		Do not connect

PRODUCT PREVIEW

LVDS TIMING DIAGRAM



(1) Referenced to ADC Input (internal mode) for illustration purposes only.

DEFINITION OF SETUP AND HOLD TIMES

TIMING CHARACTERISTICS(1)

PARAMETER		TEST CONDITIONS	AFE5805			UNIT
			MIN	TYP	MAX	
$t_{D(A)}$	ADC aperture delay		1.5		4.5	ns
	Aperture delay variation	Channel-to-channel within the same device (3σ)		±20		ps
t_J	Aperture jitter			400		f_S, rms
t_{WAKE}	Wake-up time	Time to valid data after coming out of COMPLETE POWER-DOWN mode		50		µs
		Time to valid data after coming out of PARTIAL POWER-DOWN mode (with clock continuing to run during power-down)		2		µs
		Time to valid data after stopping and restarting the input clock		40		µs
	Data latency			12		Clock cycles

(1) Timing parameters are ensured by design and characterization; not production tested.

PRODUCT PREVIEW

SERIAL INTERFACE

The AFE5805 has a set of internal registers that can be accessed through the serial interface formed by pins $\overline{CS}$ (chip select, active low), SCLK (serial interface clock), and SDATA (serial interface data). When $\overline{CS}$ is low, the following actions occur:

- Serial shift of bits into the device is enabled
- SDATA (serial data) is latched at every rising edge of SCLK
- SDATA is loaded into the register at every 24th SCLK rising edge

If the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active $\overline{CS}$ pulse. The first eight bits form the register address and the remaining 16 bits form the register data. The interface can work with SCLK frequencies from 20MHz down to very low speeds (a few hertz) and also with a non-50% SCLK duty cycle.

Register Initialization

After power-up, the internal registers ***must*** be initialized to the respective default values. Initialization can be done in one of two ways:

1. Through a hardware reset, by applying a low-going pulse on the ADS_$\overline{RESET}$ pin; or
2. Through a software reset; using the serial interface, set the S_RST bit high. Setting this bit initializes the internal registers to the respective default values and then self-resets the bit low. In this case, the ADS_$\overline{RESET}$ pin stays high (inactive).

Serial Port Interface (SPI) Information

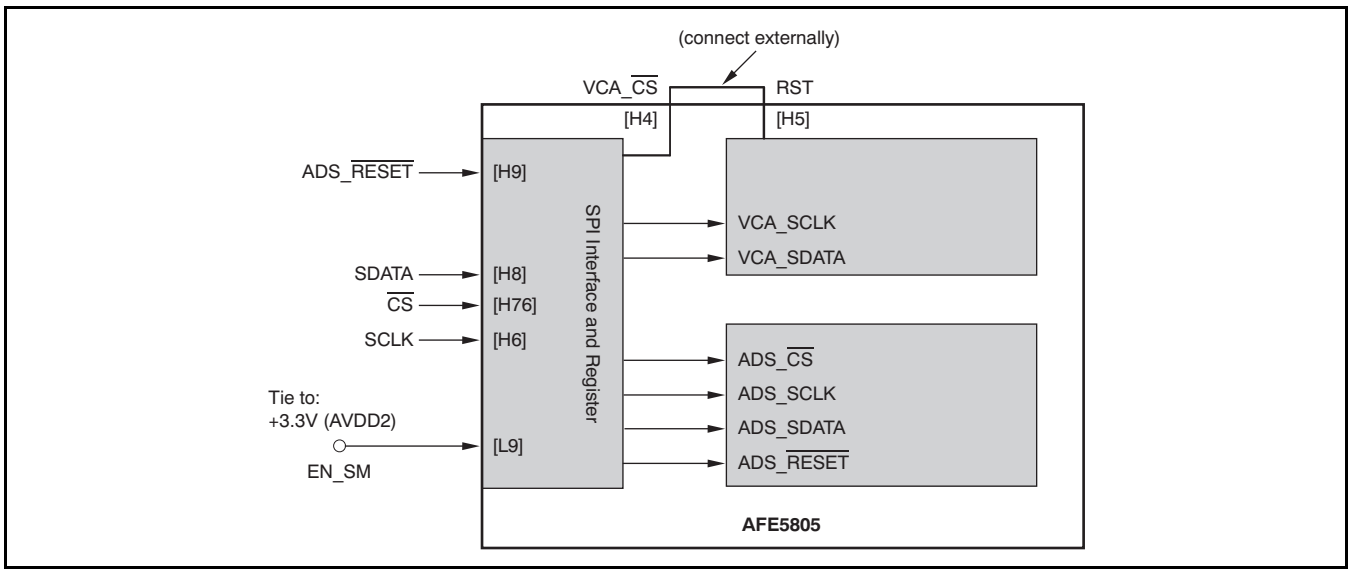
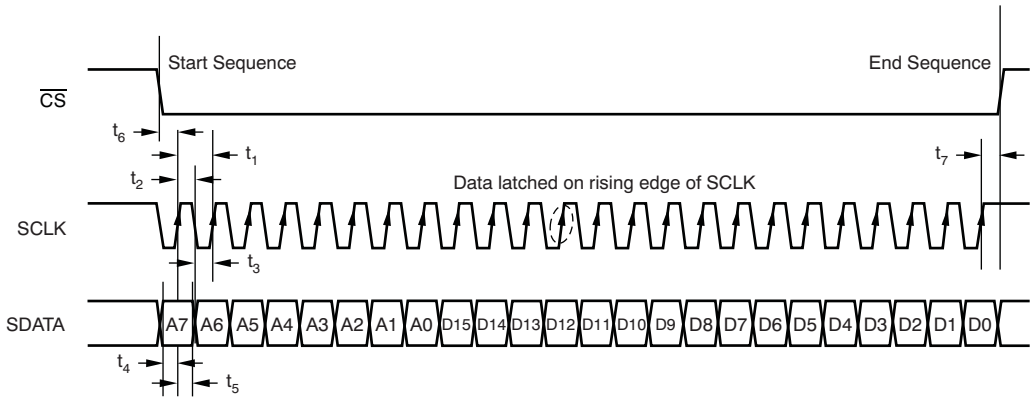


Figure 1. Typical Connection Diagram for the SPI Control Lines

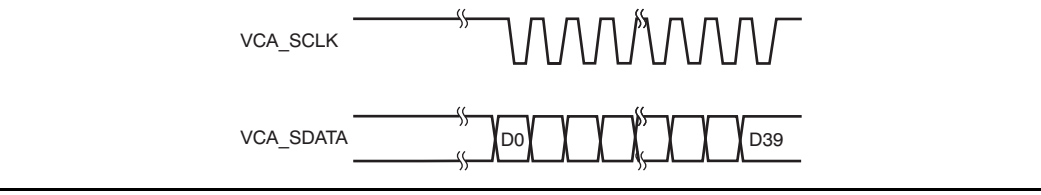
PRODUCT PREVIEW

SERIAL INTERFACE TIMING



PARAMETER	DESCRIPTION	AFE5805			UNIT
		MIN	TYP	MAX	
t_1	SCLK period	50			ns
t_2	SCLK high time	20			ns
t_3	SCLK low time	20			ns
t_4	Data setup time	5			ns
t_5	Data hold time	5			ns
t_6	$\overline{CS}$ fall to SCLK rise	8			ns
t_7	Time between last SCLK rising edge to $\overline{CS}$ rising edge	8			ns

Internally-Generated VCA Control Signals



VCA_SCLK and VCA_SDATA signals are generated if:

- Registers with address 16, 17, or 18 (Hex) are written to
- EN_SM is HIGH

PRODUCT PREVIEW

SERIAL REGISTER MAP

Table 2. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE(1)(2)(3)(4)

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
00																X	S_RST	Self-clearing software RESET.	Inactive
03	0	0	0	0	0	0	0	0	0	0	RES_VCA	0	0	0	0	0			
16	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	VCA_DATA<0:15>		
17	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	VCA_DATA<16:317		
18									X	X	X	X	X	X	X	X	VCA_DATA<32:39>		
0F													X	X	X	X	PDN_CH<1:4>	Channel-specific ADC power-down mode.	Inactive
									X	X	X	X					PDN_CH<1:5>	Channel-specific ADC power-down mode.	Inactive
								X									PDN_PARTIAL	Partial power-down mode (fast recovery from power-down).	Inactive
						0	X										PDN_COMPLETE	Register mode for complete power-down (slower recovery).	Inactive
						X	0										PDN_PIN_CFG	Configures the PD pin for partial power-down mode.	Complete power-down
11														X	X	X	ILVDS_LCLK<2:0>	LVDS current drive programmability for $LCLK_N$ and $LCLK_P$ pins.	3.5mA drive
										X	X	X					ILVDS_FRAME <2:0>	LVDS current drive programmability for $ADCLK_N$ and $ADCLK_P$ pins.	3.5mA drive
						X	X	X									ILVDS_DAT<2:0>	LVDS current drive programmability for OUT_N and OUT_P pins.	3.5mA drive
12		X															EN_LVDS_TERM	Enables internal termination for LVDS buffers.	Termination disabled
		1												X	X	X	TERM_LCLK<2:0>	Programmable termination for $LCLK_N$ and $LCLK_P$ buffers.	Termination disabled
		1								X	X	X					TERM_FRAME <2:0>	Programmable termination for $ADCLK_N$ and $ADCLK_P$ buffers.	Termination disabled
		1				X	X	X									TERM_DAT<2:0>	Programmable termination for OUT_N and OUT_P buffers.	Termination disabled
14													X	X	X	X	LFNS_CH<8:1>	Channel-specific, low-frequency noise suppression mode enable.	Inactive
									X	X	X	X					LFNS_CH<8:5>	Channel-specific, low-frequency noise suppression mode enable.	Inactive
24									X	X	X	X	X	X	X	X	INVERT_CH<1:4>	Swaps the polarity of the analog input pins electrically.	IN_P is positive input
																	INVERT_CH<8:5>	Swaps the polarity of the analog input pins electrically.	IN_P is positive input
25										X	0	0					EN_RAMP	Enables a repeating full-scale ramp pattern on the outputs.	Inactive
										0	X	0					DUALCUSTOM_ PAT	Enables the mode wherein the output toggles between two defined codes.	Inactive
										0	0	X					SINGLE_CUSTOM _PAT	Enables the mode wherein the output is a constant specified code.	Inactive
															X	X	BITS_CUSTOM1 <11:10>	2MSBs for a single custom pattern (and for the first code of the dual custom pattern). <11> is the MSB.	Inactive
													X	X			BITS_CUSTOM2 <11:10>	2MSBs for the second code of the dual custom pattern.	Inactive
26	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM1 <9:0>	10 lower bits for the single custom pattern (and for the first code of the dual custom pattern). <0> is the LSB.	Inactive

(1) The unused bits in each register (identified as blank table cells) must be programmed as '0'.
(2) X = Register bit referenced by the corresponding name and description (default is 0).
(3) Bits marked as '0' should be forced to 0, and bits marked as '1' should be forced to 1 when the particular register is programmed.
(4) Multiple functions in a register should be programmed in a single write operation.

PRODUCT PREVIEW

Table 2. SUMMARY OF FUNCTIONS SUPPORTED BY SERIAL INTERFACE (continued)

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME	DESCRIPTION	DEFAULT
27	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM2 <9:0>	10 lower bits for the second code of the dual custom pattern.	Inactive
2A													X	X	X	X	GAIN_CH1<3:0>	Programmable gain channel 4.	0dB gain
									X	X	X	X					GAIN_CH2<3:0>	Programmable gain channel 3.	0dB gain
					X	X	X	X									GAIN_CH3<3:0>	Programmable gain channel 2.	0dB gain
	X	X	X	X													GAIN_CH4<3:0>	Programmable gain channel 1.	0dB gain
2B	X	X	X	X													GAIN_CH5<3:0>	Programmable gain channel 5.	0dB gain
					X	X	X	X									GAIN_CH6<3:0>	Programmable gain channel 6.	0dB gain
									X	X	X	X					GAIN_CH7<3:0>	Programmable gain channel 7.	0dB gain
													X	X	X	X	GAIN_CH8<3:0>	Programmable gain channel 8.	0dB gain
42	1															X	DIFF_CLK	Differential clock mode.	Single-ended clock
	1													X			EN_DCC	Enables the duty-cycle correction circuit.	Disabled
	1												X				EXT_REF_VCM	Drives the external reference mode through the V_{CM} pin.	External reference drives REF_T and REF_B
	1									X	X						PHASE_DDR<1:0>	Controls the phase of LCLK output relative to data.	90 degrees
45															0	X	PAT_DESKEW	Enables deskew pattern mode.	Inactive
															X	0	PAT_SYNC	Enables sync pattern mode.	Inactive
46	1						1							X			BTC_MODE	Binary two's complement format for ADC output.	Straight offset binary
	1						1						X				MSB_FIRST	Serialized ADC output comes out MSB-first.	LSB-first output
	1						1					X					EN_SDR	Enables SDR output mode (LCLK becomes a 12x input clock).	DDR output mode
	1		1				1					1					FALL_SDR	Controls whether the LCLK rising or falling edge comes in the middle of the data window when operating in SDR output mode.	Rising edge of LCLK in middle of data window

PRODUCT PREVIEW

SUMMARY OF FEATURES

FEATURES	DEFAULT	SELECTION	POWER IMPACT (Relative to Default) AT f_S = 50MSPS
ANALOG FEATURES			
Internal or external reference (driven on the REF_T and REF_B pins)	N/A	Pin	Internal reference mode takes approximately 20mW more power on AVDD
Exernal reference driven on the V_{CM} pin	Off	Register 42	Approximately 8mW less power on AVDD
Duty cycle correction circuit	Off	Register 42	Approximately 7mW more power on AVDD
Low-frequency noise suppression	Off	Register 14	With zero input to the ADC, low-frequency noise suppression causes digital switching at $f_S/2$, thereby increasing LVDD power by approximately 5.5mW/channel
Single-ended or differential clock	Single-ended	Register 42	Differential clock mode mode takes approximately 7mW more power on AVDD
Power-down mode	Off	Pin and register 0F	Refer to the *Power-Down Modes* section in the Electrical Characteristics table
DIGITAL FEATURES			
Programmable digital gain (0dB to 12dB)	0dB	Registers 2A and 2B	No difference
Straight offset or BTC output	Straight offset	Register 46	No difference
Swap polarity of analog input pins	Off	Register 24	No difference
LVDS OUTPUT PHYSICAL LAYER			
LVDS internal termination	Off	Register 12	Approximately 7mW more power on AVDD
LVDS current programmability	3.5mA	Register 11	As per LVDS clock and data buffer current setting
LVDS OUTPUT TIMING			
LSB- or MSB-first output	LSB-first	Register 46	No difference
DDR or SDR output	DDR	Register 46	SDR mode takes approximately 2mW more power on LVDD (at f_S = 30MSPS)
LCLK phase relative to data output	Refer to Figure 2	Register 42	No difference

DESCRIPTION OF SERIAL REGISTERS

SOFTWARE RESET

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
00																X	S_RST

Software reset is applied when the RST bit is set to '1'; setting this bit resets all internal registers and self-clears to '0'.

VCA Register Information

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
03	0	0	0	0		0	0	0	0	0	RES_VCA	0	0	0	0	0
16	VCA D15	VCA D14	VCA D13	VCA D12	VCA D11	VCA D10	VCA D9	VCA D8	VCA D7	VCA D6	VCA D5	VCA D4	VCA D3	VCA D2	1(1) D1	1(1) D0
17	VCA D31	VCA D30	VCA D29	VCA D28	VCA D27	VCA D26	VCA D25	VCA D24	VCA D23	VCA D22	VCA D21	VCA D20	VCA D19	VCA D18	VCA D17	VCA D16
18									VCA D39	VCA D38	VCA D37	VCA D36	VCA D35	VCA D34	VCA D33	VCA D32

(1) Bits D0 and D1 of register 16 are forced to '1'.

- VCA_SCLK and VCA_SDATA become active only when one of the registers 16, 17 or 18 (address in hex) of the AFE5805 are written into.
- The contents of all three registers (total 40 bits) are written on VCA_SDATA even if only one of the above registers is written into. This condition is only valid if the content of the register has changed because of the most recent write. Writing contents that are the same as existing contents does not trigger activity on VCA_SDATA.
- For example, if register 17 is written into after a RESET is applied, then the contents of register 17 as well as the default values of the bits in registers 16 and 18 are written into VCA_SDATA.
- If register 16 is then written to, then the new contents of register 16, the previously written contents of register 17, and the default contents of register 18 are written into VCA_SDATA. Note that regardless of what is written into D0 and D1 of register 16, the respective outputs on VCA_SDATA are always ‘1’.
- Alternatively, all three registers (16, 17 and 18) can also be written within one write cycle of the ADC serial interface. In that case, there would be 48 consecutive SCLK edges within the same $\overline{CS}$ active window.
- VCA_SCLK is generated using an oscillator (running at approximately 6MHz) inside the AFE5805, but the oscillator is gated so that it is active only during the write operation of the 40 VCA bits.

VCA Reset

- VCA_$\overline{CS}$ should be permanently connected to the RST-input.
- When VCA_$\overline{CS}$ goes high (either because of an active low pulse on ADC_$\overline{RESET}$ for more than 10ns or as a result or setting bit RES_VCA), the following functions are performed inside the AFE5805:
  - Bits D0 and D1 of register 16 are forced to ‘1’
  - All other bits in registers 16, 17 and 18 are RESET to the respective default values (‘0’ for all bits except D5 of register 16 which is set to a default of ‘1’).
  - No activity on signals VCA_SCLK and VCA_SDATA.
- If bit RES_VCA has been set to ‘1’, then the state machine is in the RESET state until RES_VCA is set to ‘0’.

PRODUCT PREVIEW

VCA Register Map

BYTE 1	BYTE 2		BYTE 3		BYTE 4		BYTE 5	
D0:D7	D8:D11	D12:D15	D16:D19	D20:D23	D24:D27	D28:D31	D32:D35	D36:D39
Control	CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8

Byte 1—Control Byte Register Map

BIT NUMBER	BIT NAME	DESCRIPTION
D0 (LSB)	1	Start bit; this bit is permanently set high = 1
D1	WR	Write bit; this bit is permanently set high =1
D2	PWR	1= Power-down mode enabled.
D3	BW	Low-pass filter bandwidth setting (see Table 1)
D4	CL	Clamp level setting (see Table 1)
D5	Mode	1 = TGC Mode, 0 = CW Doppler Mode
D6	PG0	LSB of PGA Gain Control (see Table 2)
D7 (MSB)	PG1	MSB of PGA Gain Control

Byte 2—First Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D8 (LSB)	DB1:1	Channel 1, LSB of Matrix Control
D9	DB1:2	Channel 1, Matrix Control
D10	DB1:3	Channel 1, Matrix Control
D11	DB1:4	Channel 1, MSB of Matrix Control
D12	DB2:1	Channel 2, LSB of Matrix Control
D13	DB2:2	Channel 2, Matrix Control
D14	DB2:3	Channel 2, Matrix Control
D15 (MSB)	DB2:4	Channel 2, MSB of Matrix Control

Byte 3—Second Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D16 (LSB)	DB3:1	Channel 3, LSB of Matrix Control
D17	DB3:2	Channel 3, Matrix Control
D18	DB3:3	Channel 3, Matrix Control
D19	DB3:4	Channel 3, MSB of Matrix Control
D20	DB4:1	Channel 4, LSB of Matrix Control
D21	DB4:2	Channel 4, Matrix Control
D22	DB4:3	Channel 4, Matrix Control
D23 (MSB)	DB4:4	Channel 4, MSB of Matrix Control

Byte 4—Third Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D24 (LSB)	DB5:1	Channel 5, LSB of Matrix Control
D25	DB5:2	Channel 5, Matrix Control
D26	DB5:3	Channel 5, Matrix Control
D27	DB5:4	Channel 5, MSB of Matrix Control
D28	DB6:1	Channel 6, LSB of Matrix Control
D29	DB6:2	Channel 6, Matrix Control
D30	DB6:3	Channel 6, Matrix Control
D31 (MSB)	DB6:4	Channel 6, MSB of Matrix Control

Byte 5—Fourth Data Byte

BIT NUMBER	BIT NAME	DESCRIPTION
D32 (LSB)	DB7:1	Channel 7, LSB of Matrix Control
D33	DB7:2	Channel 7, Matrix Control
D34	DB7:3	Channel 7, Matrix Control
D35	DB7:4	Channel 7, MSB of Matrix Control
D36	DB8:1	Channel 8, LSB of Matrix Control
D37	DB8:2	Channel 8, Matrix Control
D38	DB8:3	Channel 8, Matrix Control
D39 (MSB)	DB8:4	Channel 8, MSB of Matrix Control

Clamp Level and LPF Bandwidth Setting

		FUNCTION
BW	D3 = 0	Bandwidth set to 15MHz
BW	D3 = 1	Bandwidth set to 10MHz
CL	D4 = 0	Clamps the output signal at 2dB below the full-scale of $2V_{PP}$ ($1.6V_{PP}$)
CL	D4 = 1	Clamp transparent (disabled)

PGA Gain Setting

PG1 (D7)	PG0 (D6)	FUNCTION
0	0	Sets PGA gain to 20dB
0	1	Sets PGA gain to 25dB
1	0	Sets PGA gain to 27dB
1	1	Sets PGA gain to 30dB

CW Switch Matrix Control for Each Channel

DBn:4 (MSB)	DBn:3	DBn:2	DBn:1 (LSB)	LNA INPUT CHANNEL n DIRECTED TO
0	0	0	0	Output CW0
0	0	0	1	Output CW1
0	0	1	0	Output CW2
0	0	1	1	Output CW3
0	1	0	0	Output CW4
0	1	0	1	Output CW5
0	1	1	0	Output CW6
0	1	1	1	Output CW7
1	0	0	0	Output CW8
1	0	0	1	Output CW9
1	0	1	0	Connected to AVDD1
1	0	1	1	Connected to AVDD1
1	1	0	0	Connected to AVDD1
1	1	0	1	Connected to AVDD1
1	1	1	0	Connected to AVDD1
1	1	1	1	Connected to AVDD1

POWER-DOWN MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
0F									X	X	X	X	X	X	X	X	PDN_CH<8:1>
								X									PDN_PARTIAL
						0	X										PDN_COMPLETE
						X	0										PDN_PIN_CFG

Each of the eight channels can be individually powered down. PDN_CH<N> controls the power-down mode for the ADC channel <N>.

In addition to channel-specific power-down, the AFE5805 also has two global power-down modes: partial power-down mode and complete power-down mode. Partial power-down mode partially powers down the chip; recovery from this mode is much quicker, provided that the clock has been running for at least 50µs before exiting this mode. Complete power-down mode, on the other hand, completely powers down the chip, and involves a much longer recovery time.

In addition to programming the device for either of these two power-down modes (through either the PDN_PARTIAL or PDN_COMPLETE bits, respectively), the PD pin itself can be configured as either a partial power-down pin or a complete power-down pin control. For example, if PDN_PIN_CFG = 0 (default), when the PD pin is high, the device enters complete power-down mode. However, if PDN_PIN_CFG = 1, when the PD pin is high, the device enters partial power-down mode.

LVDS DRIVE PROGRAMMABILITY

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
11														X	X	X	ILVDS_LCLK<2:0>
										X	X	X					ILVDS_FRAME<2:0>
						X	X	X									ILVDS_DAT<2:0>

The LVDS drive strength of the bit clock ($LCLK_P$ or $LCLK_N$) and the frame clock ($ADCLK_P$ or $ADCLK_N$) can be individually programmed. The LVDS drive strengths of all the data outputs OUT_P and OUT_N can also be programmed to the same value.

All three drive strengths (bit clock, frame clock, and data) are programmed using sets of three bits. Table 3 shows an example of how the drive strength of the bit clock is programmed (the method is similar for the frame clock and data drive strengths).

Table 3. Bit Clock Drive Strength(1)

ILVDS_LCLK<2>	ILVDS_LCLK<1>	ILVDS_LCLK<0>	LVDS DRIVE STRENGTH FOR $LCLK_P$ AND $LCLK_N$
0	0	0	3.5mA (default)
0	0	1	2.5mA
0	1	0	1.5mA
0	1	1	0.5mA
1	0	0	7.5mA
1	0	1	6.5mA
1	1	0	5.5mA
1	1	1	4.5mA

(1) Current settings lower than 1.5mA are not recommended.

PRODUCT PREVIEW

LVDS INTERNAL TERMINATION PROGRAMMING

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
12		X															EN_LVDS_TERM
		1												X	X	X	TERM_LCLK<2:0>
		1								X	X	X					TERM_FRAME<2:0>
		1				X	X	X									TERM_DAT<2:0>

The LVDS buffers have high-impedance current sources that drive the outputs. When driving traces with characteristic impedances that are not perfectly matched with the termination impedance on the receiver side, there may be reflections back to the LVDS output pins of the AFE5805 that cause degraded signal integrity. By enabling an internal termination (between the positive and negative outputs) for the LVDS buffers, the signal integrity can be significantly improved in such scenarios. To set the internal termination mode, the EN_LVDS_TERM bit should be set to '1'. Once this bit is set, the internal termination values for the bit clock, frame clock, and data buffers can be independently programmed using sets of three bits. Table 4 shows an example of how the internal termination of the LVDS buffer driving the bit clock is programmed (the method is similar for the frame clock and data drive strengths). These termination values are only typical values and can vary by several percentages across temperature and from device to device.

Table 4. Bit Clock Internal Termination

TERM_LCLK<2>	TERM_LCLK<1>	TERM_LCLK<0>	INTERNAL TERMINATION BETWEEN $LCLK_P$ AND $LCLK_N$ IN Ω
0	0	0	None
0	0	1	260
0	1	0	150
0	1	1	94
1	0	0	125
1	0	1	80
1	1	0	66
1	1	1	55

LOW-FREQUENCY NOISE SUPPRESSION MODE

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
14													X	X	X	X	LFNS_CH<1:4>
									X	X	X	X					LFNS_CH<8:5>

The low-frequency noise suppression mode is especially useful in applications where good noise performance is desired in the frequency band of 0MHz to 1MHz (around dc). Setting this mode shifts the low-frequency noise of the AFE5805 to approximately $f_S/2$, thereby moving the noise floor around dc to a much lower value. LFNS_CH<8:1> enables this mode individually for each channel.

PRODUCT PREVIEW

ANALOG INPUT INVERT

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
24													X	X	X	X	INVERT_CH<1:4>
									X	X	X	X					INVERT_CH<8:5>

Normally, the IN_P pin represents the positive analog input pin, and IN_N represents the complementary negative input. Setting the bits marked INVERT_CH<8:1> (individual control for each channel) causes the inputs to be swapped. IN_N now represents the positive input, and IN_P the negative input.

LVDS TEST PATTERNS

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
25										X	0	0					EN_RAMP
										0	X	0					DUALCUSTOM_PAT
										0	0	X					SINGLE_CUSTOM_PAT
															X	X	BITS_CUSTOM1<11:10>
													X	X			BITS_CUSTOM2<11:10>
26	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM1<9:0>
27	X	X	X	X	X	X	X	X	X	X							BITS_CUSTOM2<9:0>
45															0	X	PAT_DESKEW
															X	0	PAT_SYNC

The AFE5805 can output a variety of test patterns on the LVDS outputs. These test patterns replace the normal ADC data output. Setting EN_RAMP to '1' causes all the channels to output a repeating full-scale ramp pattern. The ramp increments from zero code to full-scale code in steps of 1LSB every clock cycle. After hitting the full-scale code, it returns back to zero code and ramps again.

The device can also be programmed to output a constant code by setting SINGLE_CUSTOM_PAT to '1', and programming the desired code in BITS_CUSTOM1<11:0>. In this mode, BITS_CUSTOM<11:0> take the place of the 12-bit ADC data at the output, and are controlled by LSB-first and MSB-first modes in the same way as normal ADC data are.

The device may also be made to toggle between two consecutive codes by programming DUAL_CUSTOM_PAT to '1'. The two codes are represented by the contents of BITS_CUSTOM1<11:0> and BITS_CUSTOM2<11:0>.

In addition to custom patterns, the device may also be made to output two preset patterns:

1. **Deskew patten:** Set using PAT_DESKEW, this mode replaces the 12-bit ADC output D<11:0> with the 010101010101 word.
2. **Sync pattern:** Set using PAT_SYNC, the normal ADC word is replaced by a fixed 111111000000 word.

Note that only one of the above patterns should be active at any given instant.

PROGRAMMABLE GAIN

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
2A													X	X	X	X	GAIN_CH4<3:0>
									X	X	X	X					GAIN_CH3<3:0>
					X	X	X	X									GAIN_CH2<3:0>
	X	X	X	X													GAIN_CH1<3:0>
2B	X	X	X	X													GAIN_CH5<3:0>
					X	X	X	X									GAIN_CH6<3:0>
									X	X	X	X					GAIN_CH7<3:0>
													X	X	X	X	GAIN_CH8<3:0>

The AFE5805, through its registers, allows for a digital gain to be programmed for each channel. This programmable gain can be set to achieve the full-scale output code even with a lower analog input swing. The programmable gain not only fills the output code range of the ADC, but also enhances the SNR of the device by using quantization information from some extra internal bits. The programmable gain for each channel can be individually set using a set of four bits, indicated as GAIN_CHN<3:0> for Channel N. The gain setting is coded in binary from 0dB to 12dB, as shown in Table 5.

Table 5. Gain Setting for Channel 1

GAIN_CH1<3>	GAIN_CH1<2>	GAIN_CH1<1>	GAIN_CH1<0>	CHANNEL 1 GAIN SETTING
0	0	0	0	0dB
0	0	0	1	1dB
0	0	1	0	2dB
0	0	1	1	3dB
0	1	0	0	4dB
0	1	0	1	5dB
0	1	1	0	6dB
0	1	1	1	7dB
1	0	0	0	8dB
1	0	0	1	9dB
1	0	1	0	10dB
1	0	1	1	11dB
1	1	0	0	12dB
1	1	0	1	Do not use
1	1	1	0	Do not use
1	1	1	1	Do not use

PRODUCT PREVIEW

CLOCK, REFERENCE, AND DATA OUTPUT MODES

ADDRESS IN HEX	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
42	1															X	DIFF_CLK
	1													X			EN_DCC
	1												X				EXT_REF_VCM
	1									X	X						PHASE_DDR<1:0>
46	1						1							X			BTC_MODE
	1						1						X				MSB_FIRST
	1						1					X					EN_SDR
	1		1				1					1					FALL_SDR

INPUT CLOCK

The AFE5805 is configured by default to operate with a single-ended input clock; CLK_P is driven by a CMOS clock and CLK_M is tied to '0'. However, by programming DIFF_CLK to '1', the device can be made to work with a differential input clock on CLK_P and CLK_M. Operating with a low-jitter differential clock generally provides better SNR performance, especially at input frequencies greater than 30MHz.

In cases where the duty cycle of the input clock falls outside the 45% to 55% range, it is recommended to enable an internal duty cycle correction circuit. Enable this circuit by setting the EN_DCC bit to '1'.

EXTERNAL REFERENCE

The AFE5805 can be made to operate in external reference mode by pulling the INT/$\overline{EXT}$ pin to '0'. In this mode, the REF_T and REF_B pins should be driven with voltage levels of 2.5V and 0.5V, respectively, and must have enough drive strength to drive the switched capacitance loading of the reference voltages by each ADC. The advantage of using the external reference mode is that multiple AFE5805 units can be made to operate with the same external reference, thereby improving parameters such as gain matching across devices. However, in applications that do not have an available high drive, differential external reference, the AFE5805 can still be driven with a single external reference voltage on the V_{CM} pin. When EXT_REF_VCM is set as '1' (and the INT/$\overline{EXT}$ pin is set to '0'), the V_{CM} pin is configured as an input pin, and the voltages on REF_T and REF_B are generated as shown in Equation 1 and Equation 2.

$$VREF_T = 1.5V + \frac{V_{CM}}{1.5V} \quad (1)$$

$$VREF_B = 1.5V - \frac{V_{CM}}{1.5V} \quad (2)$$

PRODUCT PREVIEW

BIT CLOCK PROGRAMMABILITY

The output interface of the AFE5805 is normally a DDR interface, with the LCLK rising edge and falling edge transitions in the middle of alternate data windows. Figure 2 shows this default phase.

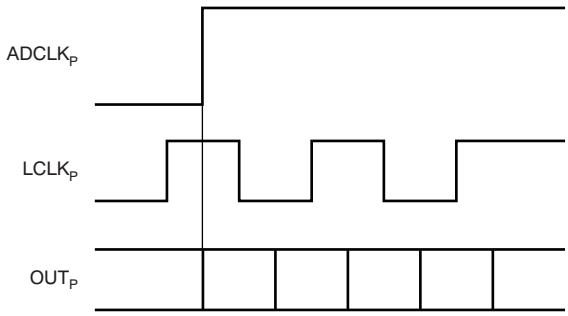


Figure 2. LCLK Default Phase

The phase of LCLK can be programmed relative to the output frame clock and data using bits PHASE_DDR<1:0>. Figure 3 shows the LCLK phase modes.

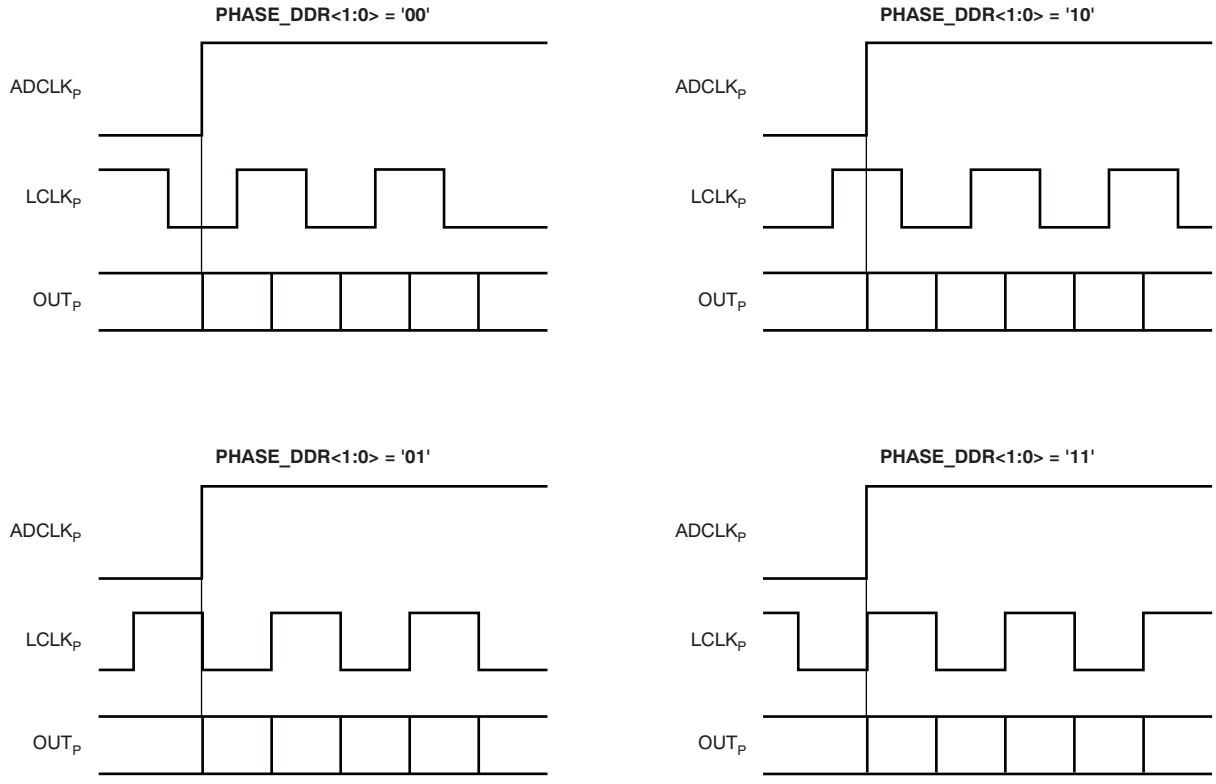


Figure 3. LCKL Phase Programmability Modes

PRODUCT PREVIEW

In addition to programming the phase of LCLK in the DDR mode, the device can also be made to operate in SDR mode by setting the EN_SDR bit to '1'. In this mode, the bit clock (LCLK) is output at 12 times the input clock, or twice the rate as in DDR mode. Depending on the state of FALL_SDR, LCLK may be output in either of the two manners shown in Figure 4. As Figure 4 illustrates, only the LCLK rising (or falling) edge is used to capture the output data in SDR mode.

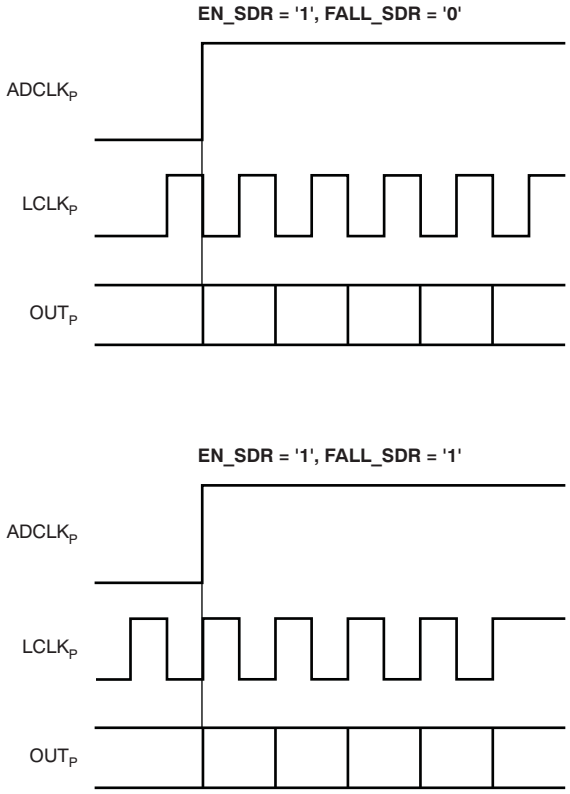


Figure 4. SDR Interface Modes

The SDR mode does not work well beyond 40MSPS because the LCLK frequency becomes very high.

DATA OUTPUT FORMAT MODES

The ADC output, by default, is in straight offset binary mode. Programming the BTC_MODE bit to '1' inverts the MSB, and the output becomes binary two's complement mode.

Also by default, the first bit of the frame (following the rising edge of ADCLK$_P$) is the LSB of the ADC output. Programming the MSB_FIRST mode inverts the bit order in the word, and the MSB is output as the first bit following the ADCLK$_P$ rising edge.

TYPICAL CHARACTERISTICS

AVDD_5V = 5.0V, AVDD1 = VDD2 = DVDD = 3.3V, LVDD = 1.8V, single-ended input into LNA, ac-coupled with 1.0µF, V_{CNTL} = 1.0V, f_{IN} 5MHz, Clock = 40MSPS, 50% duty cycle, –1dBFS input magnitude, internal reference mode, I_{SET} = 56kΩ, LVDS buffer setting = 3.5mA, at ambient temperature T_A = +25°C, unless otherwise noted.

GAIN SWEEP vs PG SETTING

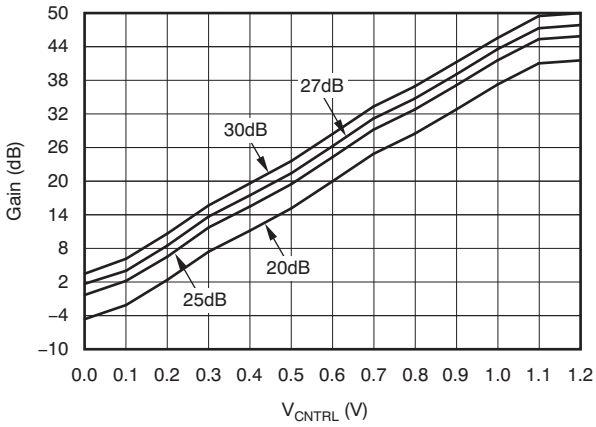


Figure 5.

10MHz LOW-PASS FILTER RESPONSE

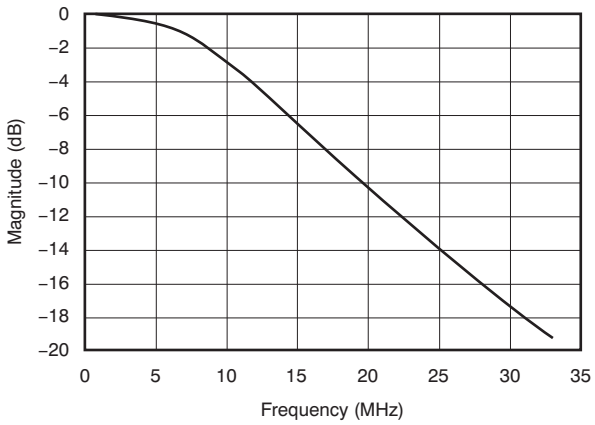


Figure 6.

15MHz LOW-PASS FILTER RESPONSE

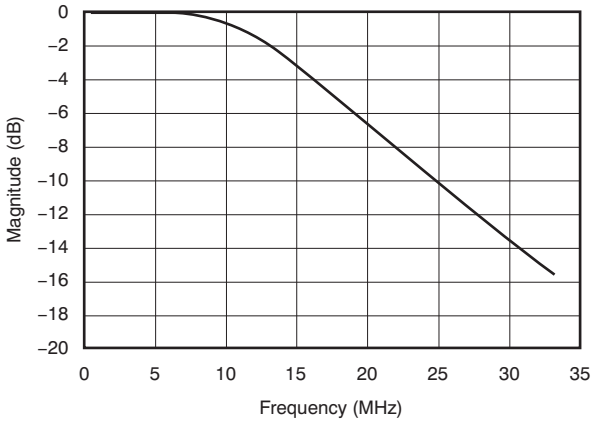


Figure 7.

CROSSTALK BETWEEN CH 8 AND CH N AT 2MHz

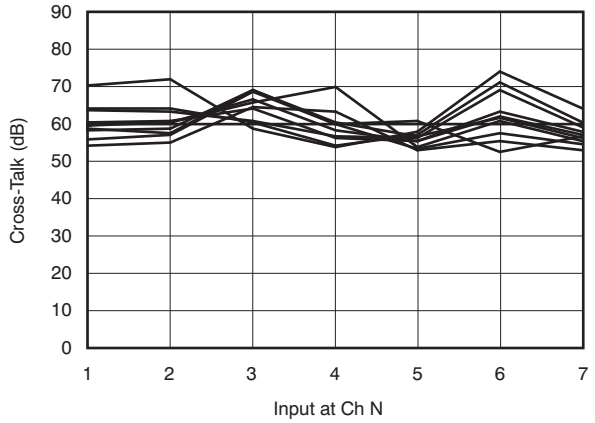


Figure 8.

PRODUCT PREVIEW

APPLICATION INFORMATION

CLOCK INPUT

The eight channels on the device operate from a single ADCLK input. To ensure that the aperture delay and jitter are the same for all channels, the AFE5805 uses a clock tree network to generate individual sampling clocks to each channel. The clock paths for all the channels are matched from the source point to the sampling circuit. This architecture ensures that the performance and timing for all channels are identical. The use of the clock tree for matching introduces an aperture delay that is defined as the delay between the rising edge of ADCLK and the actual instant of sampling. The aperture delays for all the channels are matched to the best possible extent. A mismatch of ±20ps (±3σ) could exist between the aperture instants of the eight ADCs within the same chip. However, the aperture delays of ADCs across two different chips can be several hundred picoseconds apart.

The AFE5805 can operate either in CMOS single-ended clock mode (default is DIFF_CLK = 0) or differential clock mode (SINE, LVPECL, or LVDS). In the single-ended clock mode, CLK_M must be forced to $0V_{DC}$, and the single-ended CMOS applied on the CLK_P pin. Figure 9 shows this operation.

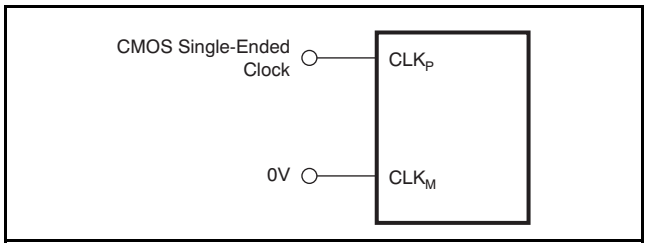


Figure 9. Single-Ended Clock Driving Circuit (DIFF_CLK = 0)

When configured for the differential clock mode (register bit DIFF_CLK = 1) the ADS528x clock inputs can be driven differentially (SINE, LVPECL, or LVDS) with little or no difference in performance between them, or with a single-ended (LVCMOS). The common-mode voltage of the clock inputs is set to V_{CM} using internal 5kΩ resistors, as shown in Figure 10. This method allows using transformer-coupled drive circuits for a sine wave clock or ac-coupling for LVPECL and LVDS clock sources, as shown in Figure 11 and Figure 12. When operating in the differential clock mode, the single-ended CMOS clock can be ac-coupled to the CLK_P input, with CLK_M connected to ground with a 0.1µF capacitor, as Figure 12 shows.

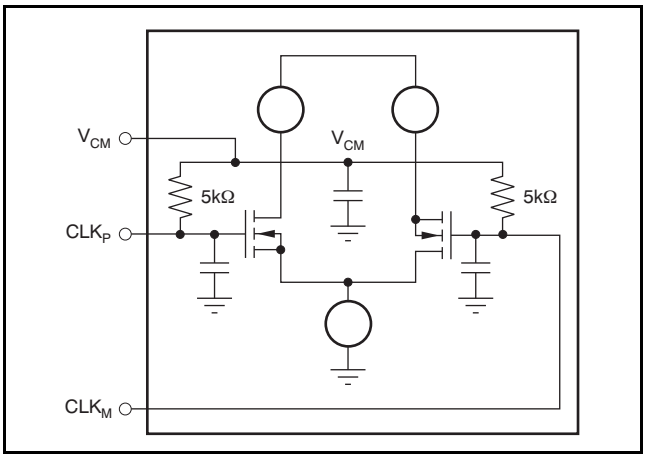


Figure 10. Internal Clock Buffer

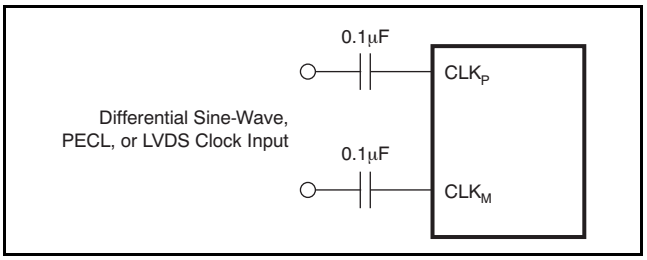


Figure 11. Differential Clock Driving Circuit (DIFF_CLK = 1)

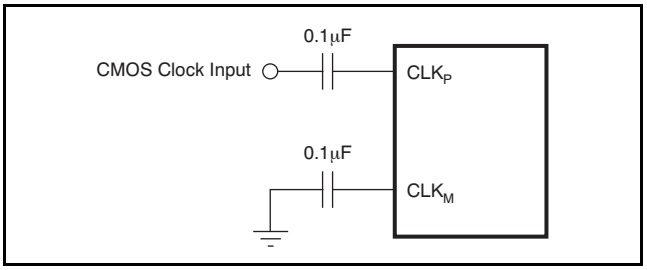


Figure 12. Single-Ended Clock Driving Circuit When DIFF_CLK = 1

For best performance, the clock inputs must be driven differentially, reducing susceptibility to common-mode noise. For high input frequency sampling, it is recommended to use a clock source with very low jitter. Bandpass filtering of the clock source can help reduce the effect of jitter. If the duty cycle deviates from 50% by more than 2% or 3%, it is recommended to enable the DCC through register bit EN_DCC.

PRODUCT PREVIEW

REFERENCE CIRCUIT

The digital beam-forming algorithm in an ultrasound system relies on gain matching across all receiver channels. A typical system would have about 12 octal ADCs on the board. In such a case, it is critical to ensure that the gain is matched, essentially requiring the reference voltages seen by all the ADCs to be the same. Matching references within the eight channels of a chip is done by using a single internal reference voltage buffer. Trimming the reference voltages on each chip during production ensures that the reference voltages are well-matched across different chips.

All bias currents required for the internal operation of the device are set using an external resistor to ground at the I_{SET} pin. Using a 56kΩ resistor on I_{SET} generates an internal reference current of 20μA. This current is mirrored internally to generate the bias current for the internal blocks. Using a larger external resistor at I_{SET} reduces the reference bias current and thereby scales down the device operating power. However, it is recommended that the external resistor be within 10% of the specified value of 56kΩ so that the internal bias margins for the various blocks are proper.

Buffering the internal bandgap voltage also generates the common-mode voltage V_{CM}, which is set to the midlevel of REF_T and REF_B, and is accessible on a pin (pin 65 in TQFP-80 package, pin 53 in QFN-64 package). It is meant as a reference voltage to derive the input common-mode if the input is directly coupled. It can also be used to derive the reference common-mode voltage in the external reference mode. Figure 13 shows the suggested decoupling for the reference pins.

The device also supports the use of external reference voltages. There are two methods to force the references externally. The first method involves pulling INT/$\overline{EXT}$ low and forcing externally REF_T and REFB to 2.5V and 0.5V nominally, respectively. In this mode, the internal reference buffer goes to a 3-state output. The external reference driving circuit should be designed to provide the required switching current for the eight ADCs inside the chip. It should be noted that in this mode, V_{CM} and I_{SET} continue to be generated from the internal bandgap voltage, as in the internal reference mode. It is therefore important to ensure that the common-mode voltage of the externally-forced reference voltages matches to within 50mV of V_{CM}.

The second method of forcing the reference voltages externally can be accessed by pulling INT/$\overline{EXT}$ low, and programming the serial interface to drive the external reference mode through the V_{CM} pin (register bit called EXT_REF_VCM). In this mode, V_{CM} becomes configured as an input pin that can be driven from external circuitry. The internal reference buffers driving REF_T and REF_B are active in this mode. Forcing 1.5V on the V_{CM} pin in the mode results in REF_T and REF_B coming to 2.5V and 0.5V, respectively. In general, the voltages on REF_T and REF_B in this mode are given by Equation 3 and Equation 4:

$$VREF_T = 1.5V + \frac{V_{CM}}{1.5V} \quad (3)$$

$$VREF_B = 1.5V - \frac{V_{CM}}{1.5V} \quad (4)$$

The state of the reference voltage internal buffers during various combinations of the PD, INT/$\overline{EXT}$, and EXT_REF_VCM register bits is described in Table 6.

PRODUCT PREVIEW

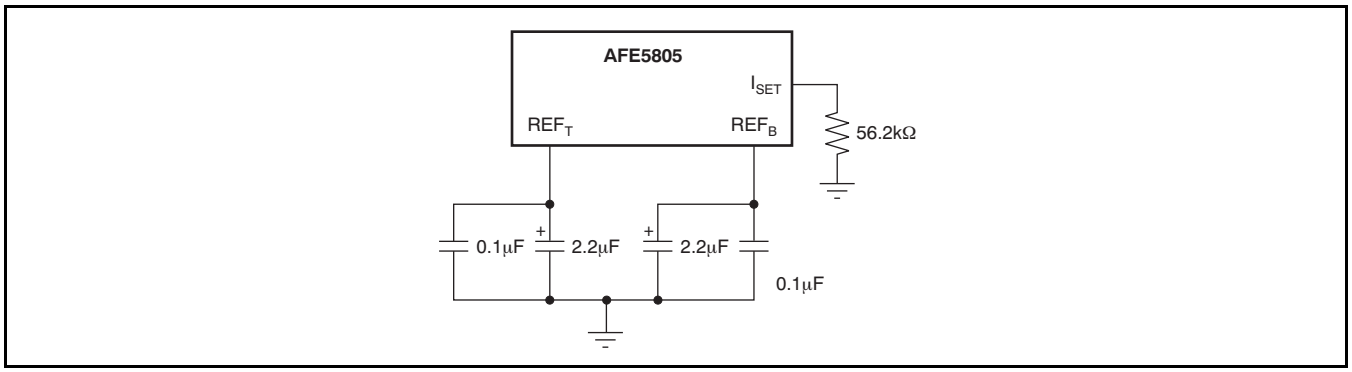


Figure 13. Suggested Decoupling on the Reference Pins

Table 6. State of Reference Voltages for Various Combinations of PD and INT/$\overline{EXT}$

REGISTER BIT	INTERNAL BUFFER STATE							
PD	0	0	1	1	0	0	1	1
INT/$\overline{EXT}$	0	1	0	1	0	1	0	1
EXT_REF_VCM	0	0	0	0	1	1	1	1
REF_T buffer	3-state	2.5V	3-state	2.5V(1)	1.5V + V_{CM}/1.5V	Do not use	2.5V(1)	Do not use
REF_B buffer	3-state	0.5V	3-state	0.5V(1)	1.5V – V_{CM}/1.5V	Do not use	0.5V(1)	Do not use
V_{CM} pin	1.5V	1.5V	1.5V	1.5V	Force	Do not use	Force	Do not use

(1) Weakly forced with reduced strength.

NOISE COUPLING ISSUES

High-speed mixed signals are sensitive to various types of noise coupling. One primary source of noise is the switching noise from the serializer and the output buffers. Maximum care is taken to isolate these noise sources from the sensitive analog blocks. As a starting point, the analog and digital domains of the device are clearly demarcated. AVDD and AVSS are used to denote the supplies for the analog sections, while LVDD and LVSS are used to denote the digital supplies. Care is taken to ensure that there is minimal interaction between the supply sets within the device. The extent of noise coupled and transmitted from the digital to the analog sections depends on:

1. The effective inductances of each of the supply and ground sets.
2. The isolation between the digital and analog supply and ground sets.

Smaller effective inductance of the supply and ground pins leads to better noise suppression. For this reason, multiple pins are used to drive each supply and ground. It is also critical to ensure that the impedances of the supply and ground lines on the board are kept to the minimum possible values. Use of ground planes in the printed circuit board (PCB) as well as large decoupling capacitors between the supply and ground lines are necessary to obtain the best possible SNR performance from the device.

It is recommended that the isolation be maintained onboard by using separate supplies to drive AVDD and LVDD, as well as separate ground planes for AVSS and LVSS. The use of LVDS buffers reduces the injected noise considerably, compared to CMOS buffers. The current in the LVDS buffer is independent of the direction of switching. Also, the low output swing as well as the differential nature of the LVDS buffer results in low-noise coupling.

PACKAGE OPTION ADDENDUM

19-May-2008

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
AFE5805ZCFR	PREVIEW	BGA	ZCF	135		TBD	Call TI	Call TI
AFE5805ZCFT	PREVIEW	BGA	ZCF	135		TBD	Call TI	Call TI
PAFE5805ZCF	PREVIEW	BGA	ZCF	135		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Clocks and Timers	www.ti.com/clocks	Digital Control	www.ti.com/digitalcontrol
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
RF/IF and ZigBee® Solutions	www.ti.com/lprf	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265