



AF4410N

N-Channel Enhancement Mode Power MOSFET

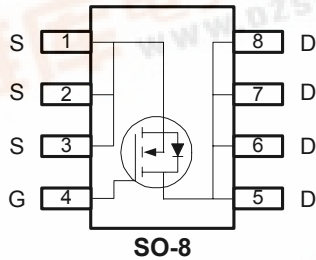
■ Features

- Simple Drive Requirement
- Low On-resistance
- Fast Switching

■ Product Summary

BV _{DSS} (V)	R _{DS(ON)} (mΩ)	I _D (A)
30	13.5	10

■ Pin Assignments



■ General Description

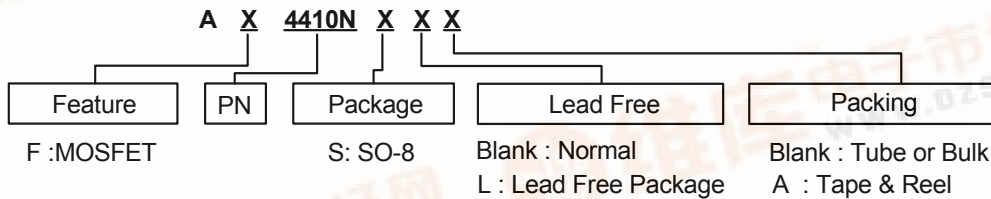
The advanced power MOSFET provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SO-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

■ Pin Descriptions

Pin Name	Description
S	Source
G	Gate
D	Drain

■ Ordering information





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■ Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	30	V
V_{GS}	Gate-Source Voltage	± 25	V
I_D	Continuous Drain Current (Note 1)	$T_A=25^\circ\text{C}$	10
		$T_A=70^\circ\text{C}$	8
I_{DM}	Pulsed Drain Current (Note 2)	50	A
P_D	Total Power Dissipation	$T_A=25^\circ\text{C}$	2.5
	Linear Derating Factor		0.02
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

■ Thermal Data

Symbol	Parameter	Maximum	Units
Rthj-amb	Thermal Resistance Junction-ambient (Note 1) Max.	50	$^\circ\text{C}/\text{W}$

■ Electrical Characteristics at $T_J=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0\text{V}, I_D=250\mu\text{A}$	30	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.037	-	$\text{V}/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance (Note 3)	$V_{GS}=10\text{V}, I_D=10\text{A}$	-	-	13.5	m Ω
		$V_{GS}=4.5\text{V}, I_D=5\text{A}$	-	-	22	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1	-	3	V
g_{fs}	Forward Transconductance	$V_{DS}=15\text{V}, I_D=10\text{A}$	-	20	-	S
I_{DSS}	Drain-Source Leakage Current ($T_J=25^\circ\text{C}$)	$V_{DS}=30\text{V}, V_{GS}=0\text{V}$	-	-	1	uA
	Drain-Source Leakage Current ($T_J=70^\circ\text{C}$)	$V_{DS}=24\text{V}, V_{GS}=0\text{V}$	-	-	25	
I_{GSS}	Gate-Source Leakage	$V_{GS}=\pm 25\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge (Note 3)	$I_D=10\text{A},$ $V_{DS}=15\text{V},$ $V_{GS}=5\text{V}$	-	13.5	-	nC
Q_{gs}	Gate-Source Charge		-	4	-	
Q_{gd}	Gate-Drain ("Miller") Charge		-	7	-	
$t_{d(on)}$	Turn-On Delay Time (Note 3)	$V_{DS}=25\text{V},$ $I_D=1\text{A},$ $R_G=3.3\Omega, V_{GS}=5\text{V}$ $R_D=25\Omega$	-	14	-	ns
t_r	Rise Time		-	16	-	
$t_{d(off)}$	Turn-Off Delay Time		-	21	-	
t_f	Fall-Time		-	15	-	
C_{iss}	Input Capacitance	$V_{GS}=0\text{V},$	-	1160	-	pF
C_{oss}	Output Capacitance	$V_{DS}=15\text{V},$	-	240	-	
C_{rss}	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	165	-	

■ Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward On Voltage (Note 3)	$I_S=2.1\text{A}, V_{GS}=0\text{V}$	-	-	1.2	V
t_{rr}	Reverse Recovery Time	$I_S=5\text{A}, V_{GS}=0\text{V},$	-	17.1	-	ns
Q_{rr}	Reverse Recovery Charge	$di/dt=100\text{A}/\mu\text{s}$	-	12	-	nC

Note 1: Surface mounted on 1 in² copper pad of FR4 board, 125 $^\circ\text{C}/\text{W}$ when mounted on Min. copper pad.

Note 2: Pulse width limited by Max. junction temperature.

Note 3: Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.

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■ Typical Performance Characteristics

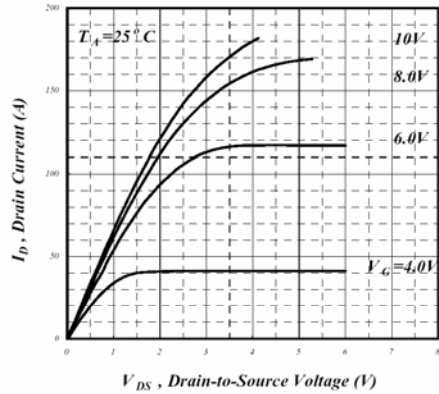


Fig 1. Typical Output Characteristics

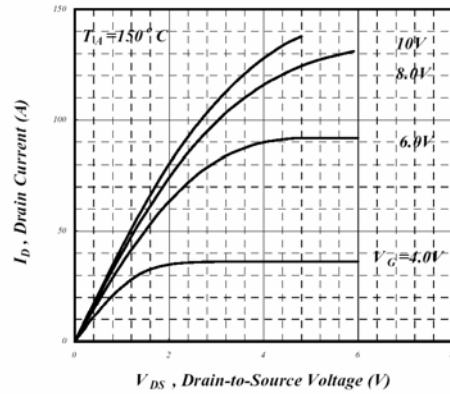


Fig 2. Typical Output Characteristics

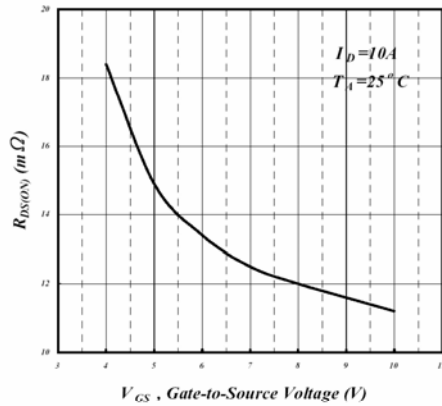


Fig 3. On-Resistance v.s. Gate Voltage

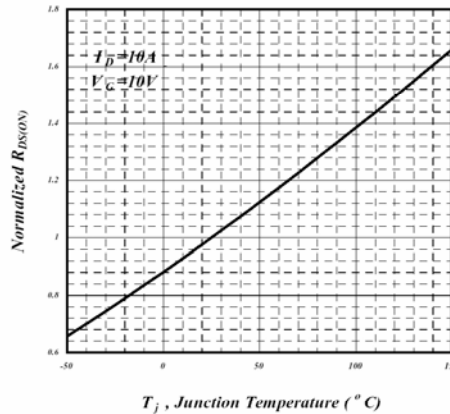


Fig 4. Normalized On-Resistance v.s. Junction Temperature

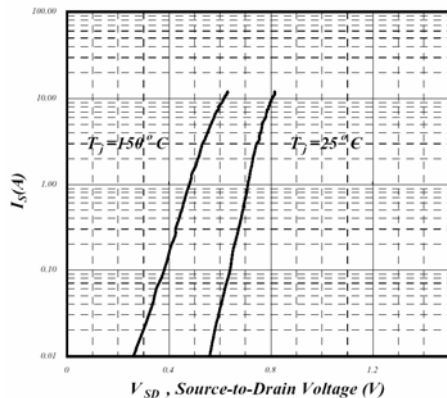


Fig 5. Forward Characteristic of Reverse Diode

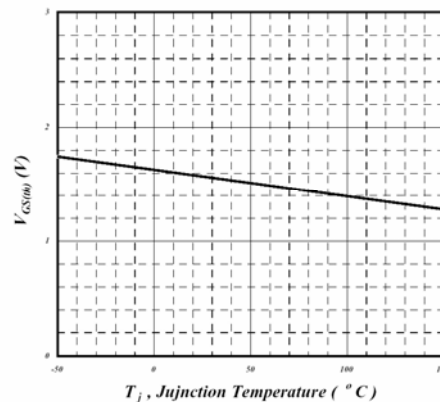


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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■ Typical Performance Characteristics (Continued)

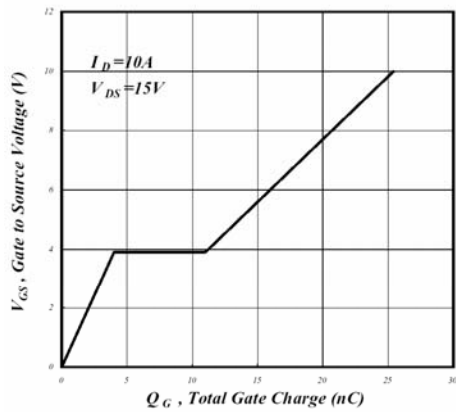


Fig 7. Gate Charge Characteristics

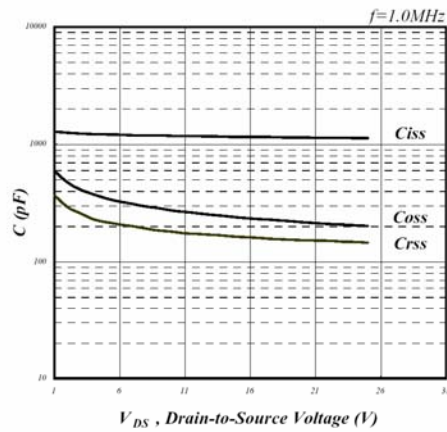


Fig 8. Typical Capacitance Characteristics

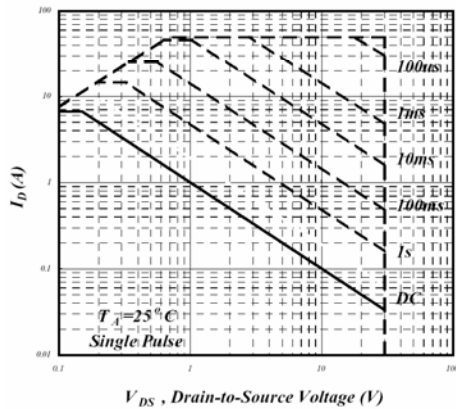


Fig 9. Maximum Safe Operating Area

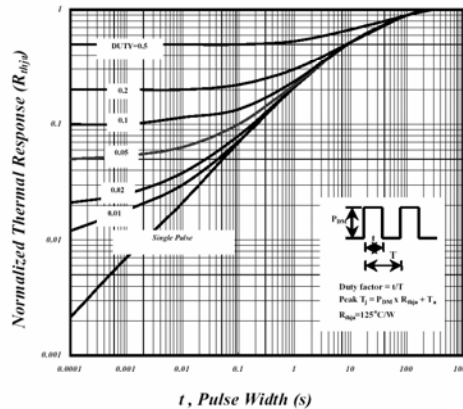


Fig 10. Effective Transient Thermal Impedance

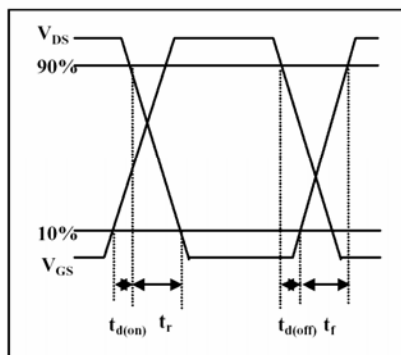


Fig 11. Switching Time Circuit

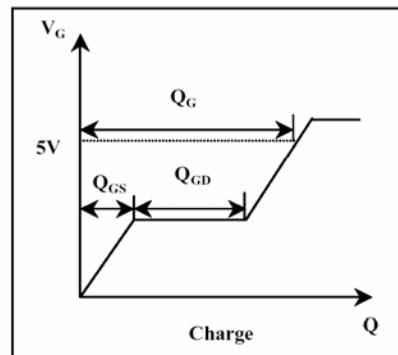
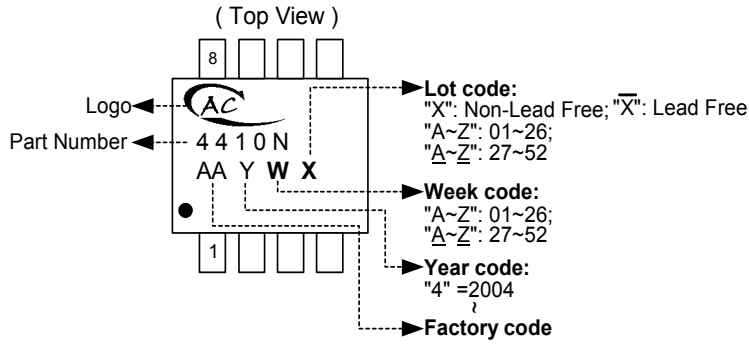


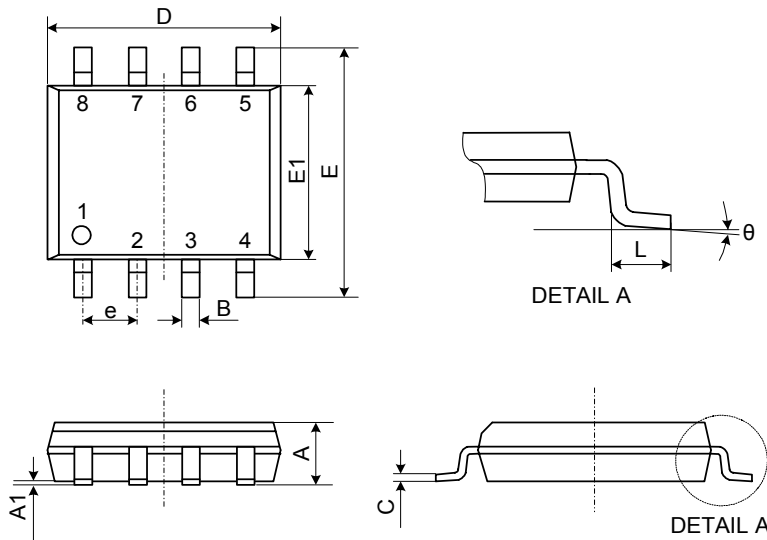
Fig 12. Gate Charge Circuit

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■ Marking Information SO-8



■ Package Information Package Type: SO-8



1. All Dimensions Are in Millimeters.
2. Dimension Does Not Include Mold Protrusions.

Symbol	Dimensions In Millimeters		
	Min.	Nom.	Max.
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
B	0.33	0.41	0.51
C	0.19	0.22	0.25
D	4.80	4.90	5.00
E	5.80	6.15	6.50
E1	3.80	3.90	4.00
L	0.38	0.71	1.27
θ	0°	4°	8°
e	1.27 TYP.		



易亨電子股份有限公司
Anachip Corporation

聯絡訊息



臺灣易亨電子大陸代理商：

景凌達(香港)有限公司

GOLDLIGHT(HONGKONG) CO.,LTD

深圳市景凌達電子有限公司

SHENZHEN GOLDLIGHT ELECTRONICS CO.,LTD

Govin(龍曉飛)

TEL:0755-28132705(EXT:8688) 61331851(EXT:8688) 83263976

FAX:0755-83263978 28132705(EXT:88)

Mobile:13802560427

MSN:govin168@hotmail.com

Http://www.anachip.net

Http://www.anachipCN.com

Http://www.anachip.com.tw

E-mail:govin@goldlight88.com

E-mail:govin@anachip.net

ADD:深圳市福田区振華路桑達電子區華明大廈318室