## 捷多邦,专业PCB**SN54AHQT27G\$SN74AHCT273** OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

SCLS375E - JUNE 1997 - REVISED APRIL 2002

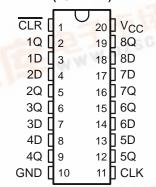
- Inputs Are TTL-Voltage Compatible
- Contain Eight Flip-Flops With Single-Rail Outputs
- **Direct Clear Input**
- **Individual Data Input to Each Flip-Flop**
- Applications Include:
  - Buffer/Storage Registers
  - Shift Registers
  - Pattern Generators
- Latch-Up Performance Exceeds 250 mA Per **JESD 17**
- **ESD Protection Exceeds JESD 22** 
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

#### description

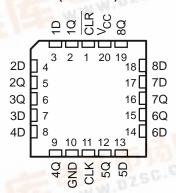
These devices are positive-edge-triggered D-type flip-flops with a direct clear (CLR) input.

Information at the data (D) inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock (CLK) pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When CLK is at either the high or low level, the D input has no effect at the output.

SN54AHCT273...JORWPACKAGE SN74AHCT273...DB, DGV, DW, N, NS, OR PW PACKAGE (TOP VIEW)



SN54AHCT273 . . . FK PACKAGE (TOP VIEW)



#### ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
Harry Mr.	PDIP – N	Tube	SN74AHCT273N	SN74AHCT273N
	SOIC - DW	Tube	SN74AHCT273DW	AHCT273
	J SOIC - DW	Tape and reel	SN74AHCT273DWR	AHC12/3
–40°C to 85°C	SOP – NS	Tape and reel	SN74AHCT273NSR	AHCT273
	SSOP – DB	Tape and reel	SN74AHCT273DBR	HB273
	TSSOP - PW	Tape and reel	SN74AHCT273PWR	HB273
	TVSOP - DGV	Tape and reel	SN74AHCT273DGVR	HB273
	CDIP – J	Tube	SNJ54AHCT273J	SNJ54AHCT273J
-55°C to 125°C	CFP – W	Tube	SNJ54AHCT273W	SNJ54AHCT273W
	LCCC - FK	Tube	SNJ54AHCT273FK	SNJ54AHCT273FK

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of

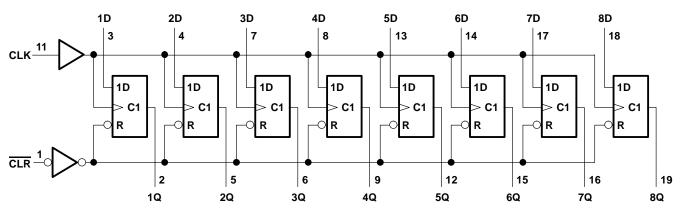


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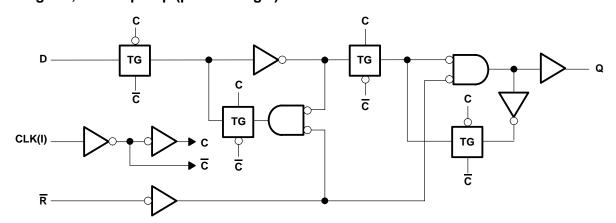
## FUNCTION TABLE (each flip-flop)

	INPUTS		OUTPUT
CLR	CLK	D	Q
L	Х	Х	L
Н	$\uparrow$	Н	Н
Н	$\uparrow$	L	L
Н	L	Χ	$Q_0$

## logic diagram (positive logic)



## logic diagram, each flip-flop (positive logic)





## SN54AHCT273, SN74AHCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V <sub>CC</sub>		
Input voltage range, V <sub>I</sub> (see Note 1)		
Output voltage range, V <sub>O</sub> (see Note 1)		
Input clamp current, $I_{IK}$ ( $V_I < 0$ )		–20 mA
Output clamp current, I <sub>OK</sub> (V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CO</sub>	c)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )		±25 mA
Continuous current through V <sub>CC</sub> or GND		
Package thermal impedance, θ <sub>JA</sub> (see Note 2)	: DB package	70°C/W
•••	DGV package	92°C/W
	DW package	58°C/W
	N package	69°C/W
	NS package	60°C/W
	PW package	83°C/W
Storage temperature range, T <sub>stq</sub>		–65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		SN54AH	SN54AHCT273		CT273	UNIT
		MIN	MAX	MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
VIH	High-level input voltage	2	2	2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
٧ <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
٧o	Output voltage	0	VCC	0	VCC	V
loh	High-level output current	27/	-8		-8	mA
loL	Low-level output current	7 <sub>0</sub> ,	8		8	mA
Δt/Δν	Input transition rise or fall time	Q	20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	85	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



## SN54AHCT273, SN74AHCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR

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## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	Vaa	T,	չ = 25°C	;	SN54AH	CT273	SN74AH	CT273	UNIT
PARAMETER	TEST CONDITIONS	vcc	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V	I <sub>OH</sub> = -50 μA	4.5 V	4.4	4.5		4.4		4.4		V
VOH	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8	, A	3.8		V
V	I <sub>OL</sub> = 50 μA	45.77			0.1		0.1		0.1	.,
VOL	I <sub>OL</sub> = 8 mA	4.5 V			0.36	ć	0.44		0.44	V
lį	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1	4:	±1*		±1	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			4	372	40		40	μΑ
ΔICC <sup>†</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5 V			1.35	OYO	1.5		1.5	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		2.5	10				10	pF

<sup>\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested at  $V_{CC} = 0 \text{ V}$ .

# timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

			T <sub>A</sub> = 1	T <sub>A</sub> = 25°C		T <sub>A</sub> = 25°C SN54AHCT273		SN74AH	UNIT	
			MIN	MAX	MIN	MAX	MIN	MAX	UNIT	
t <sub>w</sub> Pulse duration		CLR low	5		6		6		no	
t <sub>W</sub>	Puise duration	CLK high or low	5		6.5	(C)	6.5		ns	
	Code in time o	Data before CLK↑	5		5		5		20	
t <sub>su</sub>	Setup time	CLR before CLK↑	2.5		2.5		2.5		ns	
t <sub>h</sub>	Hold time, data after CLK↑		0		0		0		ns	

# switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V $\pm$ 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM	то	LOAD	T	<sub>A</sub> = 25°C	;	SN54AI	HCT273	SN74AH	CT273	UNIT
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
4			C <sub>L</sub> = 15 pF	75**	120**		65**		65		MHz
f <sub>max</sub>			C <sub>L</sub> = 50 pF	50	75		45	3	45		IVITIZ
<sup>t</sup> PHL	CLR	Q	C <sub>L</sub> = 15 pF		7.5**	10**	1**	11.6**	1	11.6	ns
<sup>t</sup> PLH	CLK		C 15 pE		5.5**	7.5**	1**	8.8**	1	8.8	ns
t <sub>PHL</sub>	CLK	Q	C <sub>L</sub> = 15 pF		5.8**	8.2**	1**	10**	1	10	115
<sup>t</sup> PHL	CLR	Q	C <sub>L</sub> = 50 pF		8.5	11	77	12.6	1	12.6	ns
<sup>t</sup> PLH	CLK		C: - 50 pF		6.5	8.5	Q <sup>2</sup> 1	9.8	1	9.8	no
<sup>t</sup> PHL	CLK	Q	C <sub>L</sub> = 50 pF		6.8	9.2	2 1	11	1	11	ns
<sup>t</sup> sk(o)		·	C <sub>L</sub> = 50 pF			1***				1	ns

<sup>\*\*</sup> On products compliant to MIL-PRF-38535, this parameter is not production tested.



<sup>†</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or VCC.

<sup>\*\*\*</sup> On products compliant to MIL-PRF-38535, this parameter does not apply.

# SN54AHCT273, SN74AHCT273 OCTAL D-TYPE FLIP-FLOPS WITH CLEAR SCLS375E – JUNE 1997 – REVISED APRIL 2002

## noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

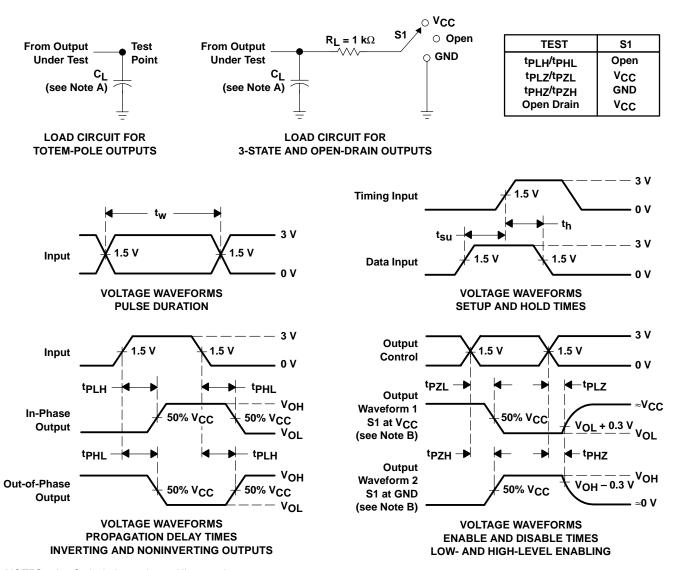
	PARAMETER	SN7	UNIT		
	PARAMETER				UNIT
V <sub>OL(P)</sub>	Quiet output, maximum dynamic V <sub>OL</sub>		0.76		V
V <sub>OL(V)</sub>	Quiet output, minimum dynamic V <sub>OL</sub>		-0.48		V
V <sub>OH(V)</sub>	Quiet output, minimum dynamic V <sub>OH</sub>	4.4			V
VIH(D)	High-level dynamic input voltage	2			V
V <sub>IL(D)</sub>	Low-level dynamic input voltage			0.8	V

NOTE 4: Characteristics are for surface-mount packages only.

## operating characteristics, $T_A = 25^{\circ}C$

	PARAMETER	TEST CO	ONDITIONS	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	No load,	f = 1 MHz	27	pF

#### PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  1 MHz,  $Z_Q = 50 \Omega$ ,  $t_f \leq 3$  ns.  $t_f \leq 3$  ns.
- $\label{eq:defD} \textbf{D.} \quad \text{The outputs are measured one at a time with one input transition per measurement.}$

Figure 1. Load Circuit and Voltage Waveforms





TEXAS INSTRUMENTS www.ti.com

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#### **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	e Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
SN74AHCT273DBR	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273DBRE4	ACTIVE	SSOP	DB	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273DGVR	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273DGVRE4	ACTIVE	TVSOP	DGV	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273DWE4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273DWRE4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT273NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHCT273NSR	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273NSRE4	ACTIVE	SO	NS	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273PWR	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273PWRE4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHCT273PWRG4	ACTIVE	TSSOP	PW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



## PACKAGE OPTION ADDENDUM

18-Jul-2006

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## N (R-PDIP-T\*\*)

## PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



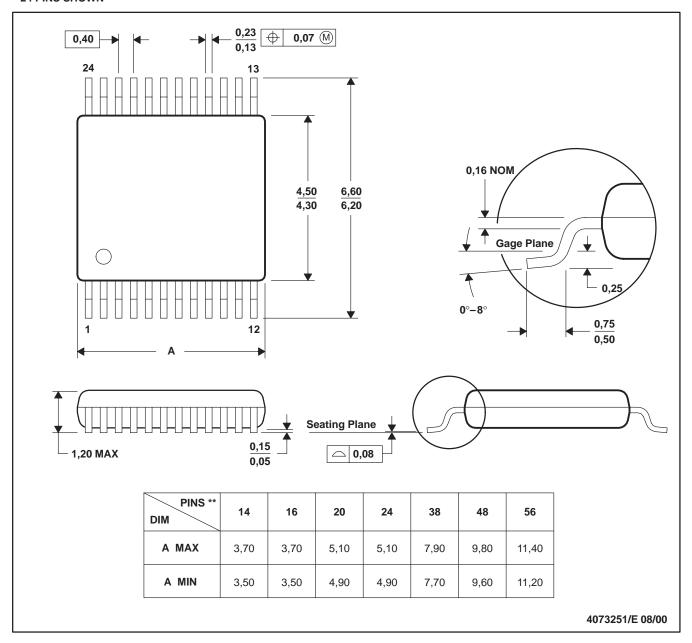
NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.

## DGV (R-PDSO-G\*\*)

#### **24 PINS SHOWN**

### **PLASTIC SMALL-OUTLINE**



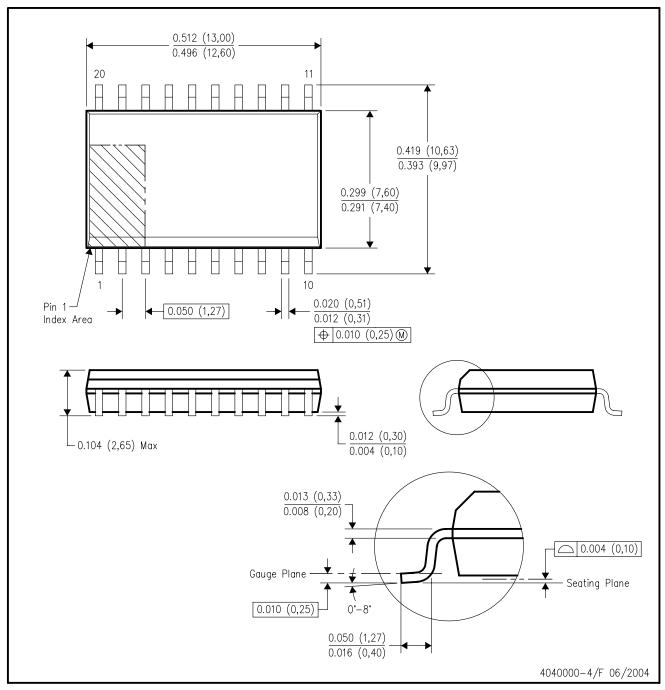
NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins MO-153 14/16/20/56 Pins – MO-194



## DW (R-PDSO-G20)

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-013 variation AC.

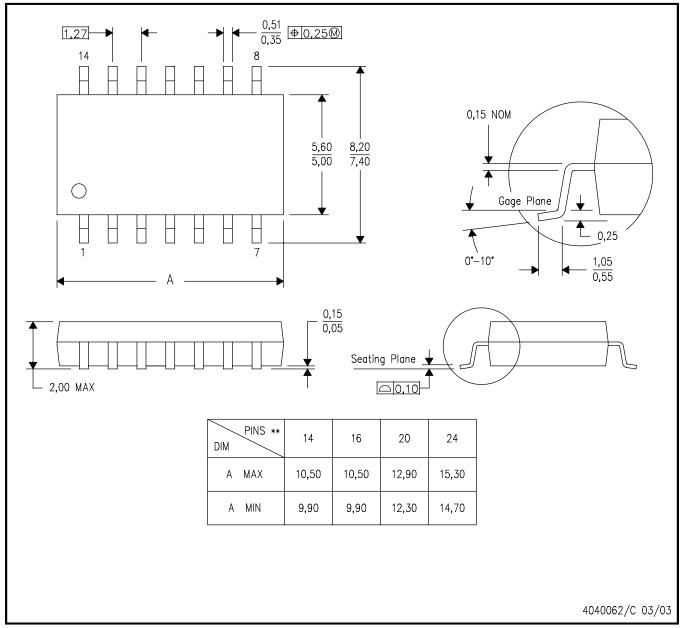


## **MECHANICAL DATA**

## NS (R-PDSO-G\*\*)

### 14-PINS SHOWN

## PLASTIC SMALL-OUTLINE PACKAGE



NOTES:

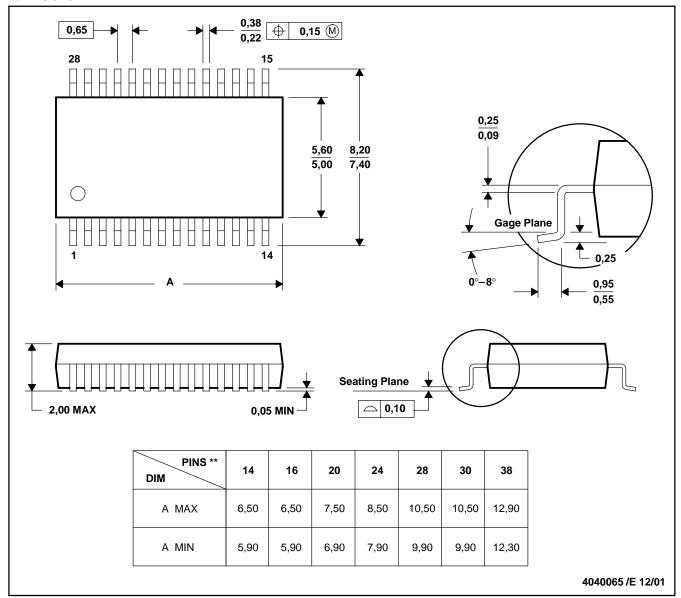
- . All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



## DB (R-PDSO-G\*\*)

#### **PLASTIC SMALL-OUTLINE**

#### **28 PINS SHOWN**



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150



## PW (R-PDSO-G\*\*)

#### 14 PINS SHOWN

#### PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-153

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