AK4560A
16bit CODEC with ALC and MIC/HP/SPK-Amps

GENERAL DESCRIPTION

AK4560A is a 16bit stereo CODEC with a built-in Microphone-Amp, Headphone-Amp and Speaker-Amp. Input circuits include Microphone/LINE inputs selector, power supply for microphone, Pre-Amp, HPF-Amp, EQ-Amp and ALC (Auto Level Control) circuit, and output circuits include LINEOUT buffer, Analog Volume, Headphone-Amp and Speaker-Amp, therefore the AK4560A suits a portable application with a built-in LCD and etc. As Multi-Power-Supply-System can be set a suitable power supply voltage in each block, the AK4560A is compatible with high performance and low power dissipation. The package is a 64pin LQFP, therefore, a new system can be a smaller board area than a current system is composed of 2 or 3 chips.

FEATURE

1. Resolution: 16bits
2. Recording Function:
   - 3-Input Selector (Internal MIC, External MIC, LINE)
   - Pre-Amp/EQ-Amp
   - HPF-Amp for wind-noise
   - Digital ALC (Auto Level Control) circuit
   - FADEIN / FADEOUT
   - Digital HPF for offset cancellation (fc=3.7Hz@fs=48kHz)
3. Playback Function
   - Digital De-emphasis Filter (tc = 50/15us, fs = 32kHz, 44.1kHz and 48kHz)
   - LINEOUT Buffer: +2dBV
   - Analog Volume
     - 0dB ~ -50dB, Mute
   - Headphone-Amp
     - Output Level: -3.4dBV, THD+N = 1%
   - Speaker-Amp with a built-in Digital ALC circuit
     - BTL Output
     - Output Power: 80mW @ 8Ω
   - BEEP and Shutter Signal Inputs
4. Analog Through Mode
5. Power Management
6. ADC Characteristics (LIN → ALC1 → ADMIX → ADC)
   - S/(N+D): 80dB, DR=S/N: 86dB
7. DAC Characteristics (DAC → LINEOUT)
   - S/(N+D): 82dB, DR=S/N: 88dB
8. Master Clock: 256fs/384fs
9. Sampling Rate: 8kHz ~ 50kHz
10. Audio Data Interface Format: MSB-First, 2's compliment (AK4518/AK4550 Compatible)
    - ADC: 16bit MSB justified, DAC: 16bit LSB justified
11. Ta = -20 ~ 85°C
12. Power Supply
    - CODEC, Analog Volume: 2.6 ~ 3.3V (typ. 2.8V)
    - LINEOUT, Headphone-Amp: 3.8 ~ 5.5V (typ. 4.5V)
    - MIC-Amp: 2.6 ~ 5.5V (typ. 3.9V)
    - Speaker-Amp: 3.8 ~ 4.3V (typ. 4.0V)
13. Power Supply Current
    - All Circuits Power-up: 32.5mA
14. Package: 64pin LQFP, 0.5mm Pitch

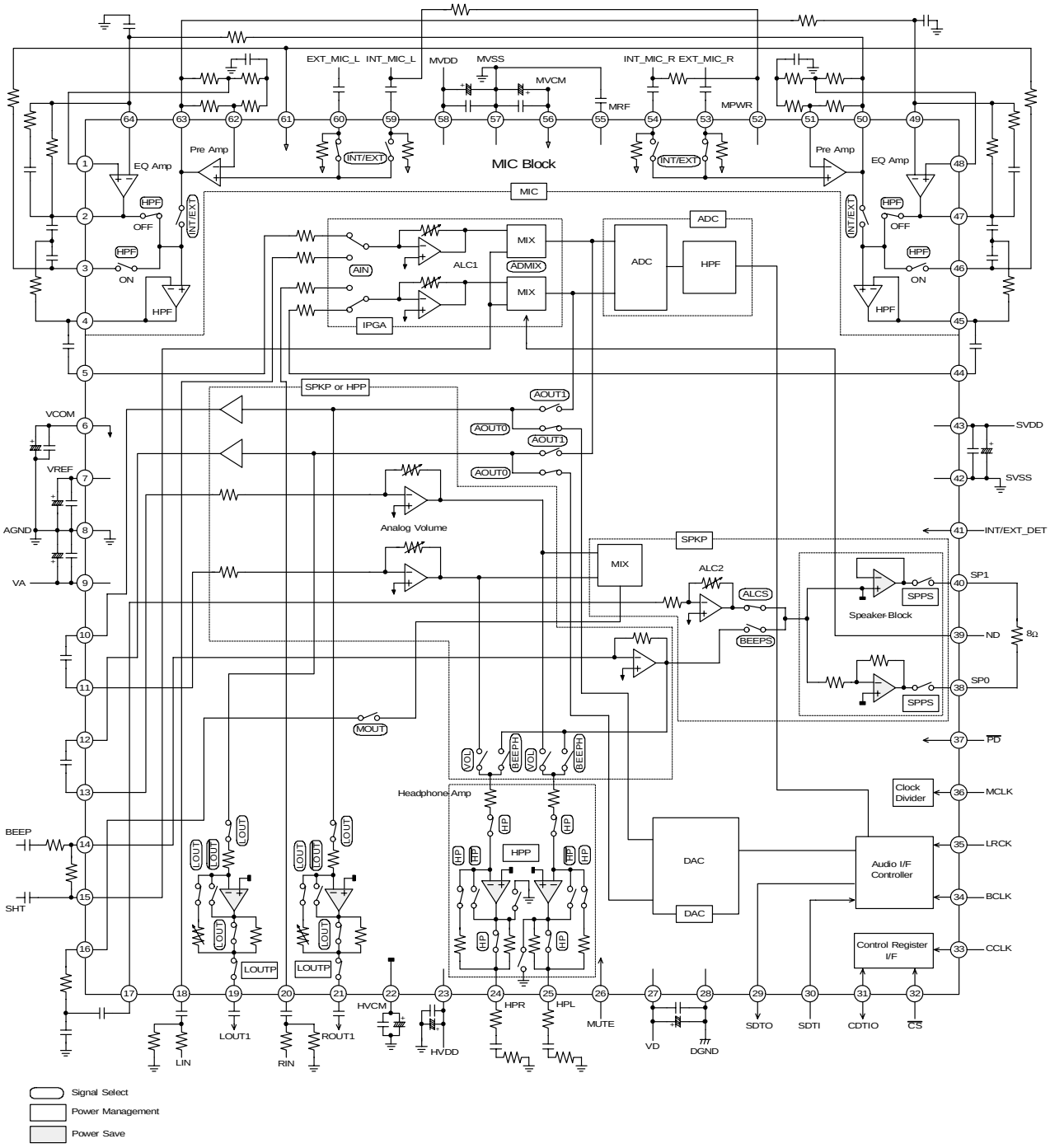
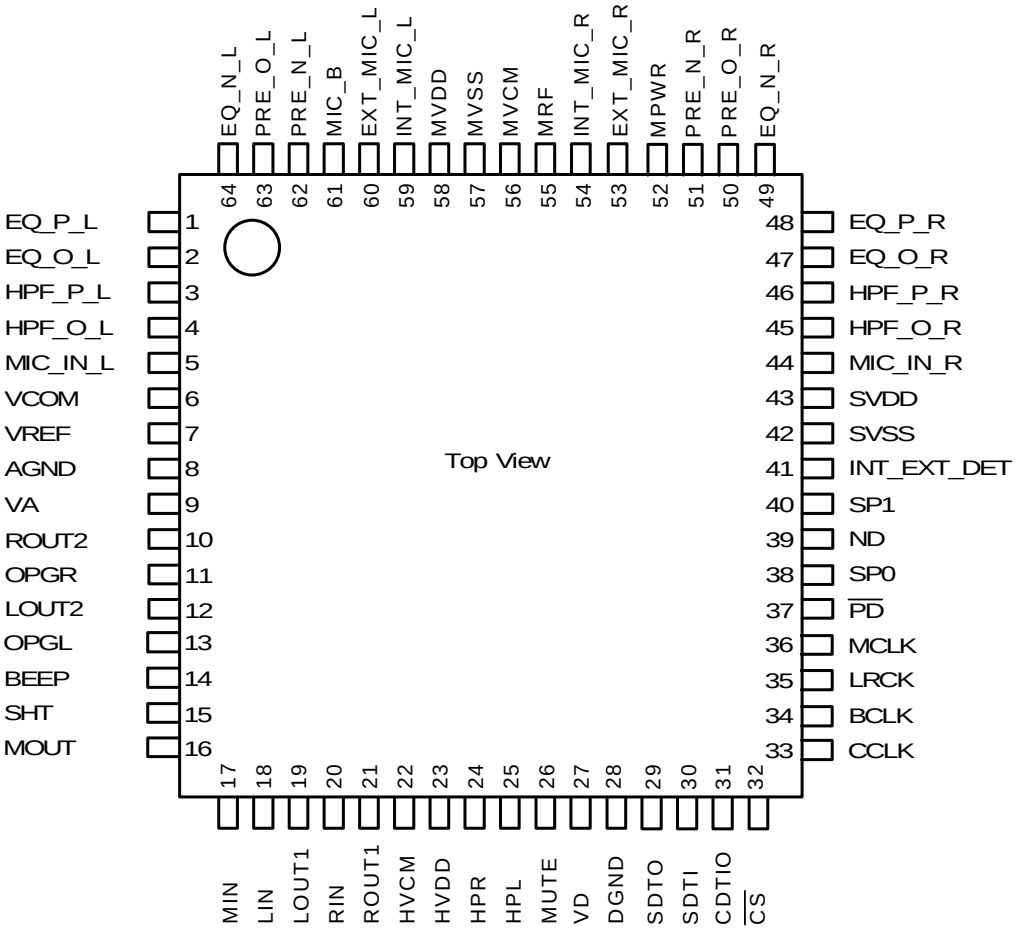


Figure 1. AK4560A Block Diagram

■ Ordering Guide

AK4560AVQ	-20 ~ +85 °C	64pin LQFP (0.5mm pitch)
AKD4560A	Evaluation Board	

■ Pin layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
Power Supply			
6	VCOM	O	Common Voltage Output Pin, 0.5 x VA
7	VREF	O	ADC, DAC Reference Level, 0.5 x VA
8	AGND	-	Analog Ground Pin
9	VA	-	Analog Power Supply Pin, +2.8V
22	HVCM	O	LINEOUT & HP-Amp Common Voltage Output Pin, 0.5 x HVDD
23	HVDD	-	LINEOUT & HP-Amp Power Supply Pin, +4.5V
27	VD	-	Digital Power Supply Pin, +2.8V
28	DGND	-	Digital Ground Pin
42	SVSS	-	Speaker Amp Ground Pin
43	SVDD	-	Speaker Amp Power Supply Pin, +4.0V
52	MPWR	O	MIC Power Supply Pin, 2.5V@MVDD=3.9V, Idd=3mA(max)
55	MRF	O	MIC Power Supply Ripple Filter Pin
56	MVCM	O	MIC Block Common Voltage Output Pin, 0.5 X MVDD
57	MVSS	-	MIC Block Ground Pin
58	MVDD	-	MIC Block Power Supply Pin
Operation Clock			
29	SDTO	O	Audio Serial Data Output Pin
30	SDTI	I	Audio Serial Data Input Pin
34	BCLK	I	Audio Serial Data Clock Pin
35	LRCK	I	Input/Output Channel Clock Pin
36	MCLK	I	Master Clock Input Pin
MIC Block			
1	EQ_P_L	I	Lch EQ-Amp Positive Input Pin
2	EQ_O_L	O	Lch EQ-Amp Output Pin
3	HPF_P_L	I	Lch HPF-Amp Positive Input Pin
4	HPF_O_L	O	Lch HPF Output Pin
45	HPF_O_R	O	Rch HPF Output Pin
46	HPF_P_R	I	Rch HPF-Amp Positive Input Pin
47	EQ_O_R	O	Rch EQ-Amp Output Pin
48	EQ_P_R	I	Rch EQ-Amp Positive Input Pin
49	EQ_N_R	I	Rch EQ-Amp Negative Input Pin
50	PRE_O_R	0	Rch Pre-Amp Output Pin
51	PRE_N_R	I	Rch Pre-Amp Negative Input Pin
53	EXT_MIC_R	I	External MIC Rch Input Pin
54	INT_MIC_R	I	Internal MIC Rch Input Pin
59	INT_MIC_L	I	Internal MIC Lch Input Pin
60	EXT_MIC_L	I	External MIC Lch Input Pin
61	MIC_B	I	MIC-Amp Bias Pin
62	PRE_N_L	I	Lch Pre-Amp Negative Input Pin
63	PRE_O_L	0	Lch Pre-Amp Output Pin
64	EQ_N_L	I	Lch EQ-Amp Negative Input Pin

Note: All input pins should not be left floating.

Control Data Interface			
31	CDTIO	I/O	Control Data Input/Output Pin
32	$\overline{\text{CS}}$	I	Chip Select Pin
33	CCLK	I	Control Clock Input Pin
ALC1 Block			
5	MIC_IN_L	I	Lch MIC Input Pin
18	LIN	I	Lch Line Input Pin
20	RIN	I	Rch Line Input Pin
44	MIC_IN_R	I	Rch MIC Input Pin
DAC			
10	ROUT2	O	Rch #2 Line Output Pin, -5.5dBV@VA=2.8V
12	LOUT2	O	Lch #2 Line Output Pin, -5.5dBV@VA=2.8V
19	LOUT1	O	Lch #1 Line Output Pin, +2dBV@VA=2.8V, VOL=+7.5dB
21	ROUT1	O	Rch #1 Line Output Pin, +2dBV@VA=2.8V, VOL=+7.5dB
Analog Volume			
11	OPGR	I	Rch Analog Volume Input Pin
13	OPGL	I	Lch Analog Volume Input Pin
Headphone Amp			
24	HPR	O	Rch Headphone-Amp Output Pin
25	HPL	O	Lch Headphone-Amp Output Pin
Speaker Amp Block			
16	MOUT	O	Analog Mixing Output Pin
17	MIN	I	ALC2 Input Pin
38	SP0	O	Speaker Amp positive Output Pin
40	SP1	O	Speaker Amp negative Output Pin
Other Functions			
14	BEEP	I	Beep Signal Input Pin
15	SHT	I	Shutter Signal Input Pin
26	MUTE	I	Mute Pin, “L”: Normal Operation, “H”: Mute
37	$\overline{\text{PD}}$	I	Power Down & Reset Pin, “L”: Power-down & Reset, “H”: Normal operation
39	ND	I	Noise Decrease Pin, “L”: Disable, “H”: Enable
41	INT_EXT_DET	I	Internal /External MIC Detect Pin, “L”: Internal MIC, “H”: External MIC

Note: All input pins should not be left floating.

ABSOLUTE MAXIMUM RATING

(AGND, DGND, MVSS, SVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog 1 (VA pin)	VA	-0.3	6.0	V
	Analog 2 (HVDD pin)	HVDD	-0.3	6.0	V
	MIC (MVDD pin)	MIC	-0.3	6.0	V
	Digital (VD pin)	VD	-0.3	6.0	V
	Speaker (SVDD pin)	SVDD	-0.3	6.0	V
	| DGND – AGND | (Note 2)	ΔGND1	-	0.3	V
	| MVSS – AGND | (Note 2)	ΔGND2	-	0.3	V
	| SVSS – AGND | (Note 2)	ΔGND3	-	0.3	V
Input Current (Any pines except supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA1	-0.3	VA+0.3	V
(Note 4)		VINA2	-0.3	MIC+0.3	V
Digital Input Voltage (Note 5)		VIND1	-0.3	VD+0.3	V
(Note 6)		VIND2	-0.3	HVDD+0.3	V
(Note 7)		VIND3	-0.3	SVDD+0.3	V
Ambient Temperature		Ta	-20	85	°C
Storage Temperature		Tstg	-65	150	°C
Maximum Power Dissipation (Note 8)		Pd	-	650	mW

Note 1. All voltage with respect to ground.
Note 2. DGND and AGND, MVSS and AGND, SVSS and AGND are the same voltage.
Note 3. Analog input pins except EXT_MIC_L, EXT_MIC_R, INT_MIC_L, INT_MIC_R, PRE_N_L, PRE_N_R, EQ_N_L, EQ_N_R, EQ_P_L, EQ_P_R, HPF_P_L, HPF_P_R and MIC_B pins.
Note 4. EXT_MIC_L, EXT_MIC_R, INT_MIC_L, INT_MIC_R, PRE_N_L, PRE_N_R, EQ_N_L, EQ_N_R, EQ_P_L, EQ_P_R, HPF_P_L, HPF_P_R and MIC_B pins
Note 5. Except INT_EXT_DET, ND and MUTE pins
Note 6. MUTE pin
Note 7. INT_EXT_DET and ND pins
Note 8. Wiring density is 50% over.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AGND, DGND, MVSS, SVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog 1 (VA pin)	VA	2.6	2.8	3.3	V
	Analog 2 (HVDD pin)	HVDD	3.8	4.5	5.5	V
	MIC (MIC pin)	MIC	2.6	3.9	5.5	V
	Digital (VD pin)	VD	2.6	2.8	3.3	V
	Speaker (SVDD pin)	SVDD	3.8	4.0	4.3	V

Note 1. All voltage with respect to ground.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; VA=VD=2.8V, MVDD=3.9V, SVDD=4.0V, HVDD=4.5V; AGND=DGND=MVSS=SVSS=0V; fs=48kHz; Input Frequency = 1kHz; Measurement width = 20Hz ~ 20kHz; unless otherwise specified)

Parameter	min	typ	max	Units
Pre-Amp Characteristics:				
Input Resistance (Note 9)	70	100	130	kΩ
Maximum Output Voltage (Note 10)			-1	dBV
Gain	+18	+26	+30	dB
Load Resistance	1			kΩ
Load Capacitance (Note 11)			20	pF
EQ-Amp Characteristics: (Gain:0dB)				
Maximum Output Voltage (Note 11)			-1	dBV
Load Resistance	1			kΩ
Load Capacitance (Note 11)			20	pF
HPF-Amp Characteristics: (Gain: 0dB)				
Maximum Output Voltage (Note 10)			-1	dBV
Load Resistance	3			kΩ
Load Capacitance (Note 11)			20	pF
MIC Block Characteristics: Measured via HPF_O_L/HPF_O_R (Note 12)				
S/(N+D) (-10dBV Output)	60	77		dB
Output Noise Voltage (No signal input, Rg = 1kΩ)				
BW = 20Hz ~ 20kHz, A-Weighted) (Note 13)		-93	-89	dBV
BW = 400Hz ~ 30kHz (Note 14)		-92	-88	dBV
Interchannel Isolation	70	90		dB
MIC Power Supply Characteristics:				
Output Voltage (No Load) (Note 15)	2.2	2.5	2.8	V
Output Current			3	mA

Note 9. INT_MIC_L, INT_MIC_R, EXT_MIC_L and EXT_MIC_R pins

Note 10. Maximum output voltage is typically (MVDD-1.3) V.

Note 11. When output pin drives some capacitive load, some resistor should be added in series between output pin and capacitive load.

Note 12. These values are measured via the following path. EQ-Amp and HPF-Amp are a unity gain buffer.
Pre-Amp (Gain: +26dB → EQ-Amp (Gain: 0dB, Not add signal of other channel) → HPF-Amp (Gain: 0dB)

Note 13. In case of the following path, output noise voltage is suitable value for -59.4dB (typ) and -55.4dBV (min).
MIC Block (Gain: +26dB, Input from INT_MIC_L/INT_MIC_R pins) → IPGA (Gain: +26dB) + ADC → DAC+LINEOUT (Gain: +7.5dB, Measured via LOUT1/ROUT1 pins)

Note 14. In the following path, if analog input signal is –70dBV (Then analog output level is –10.5dBV at LINEOUT), output noise voltage except the fundamental wave is suitable value for 58.4dBV(typ.) and –54.4dBV(min.). Because it is not possible that each block of IPGA, ADC, DAC and LINEOUT output a distortion when the small signal level is input.
MIC Block (Gain: +26dB, Input from INT_MIC_L/INT_MIC_R pins) → IPGA (Gain: +26dB) + ADC → DAC+LINEOUT (Gain: +7.5dB, Measured via LOUT1/ROUT1 pins)

Note 15. Output voltage is typically (MVDD - 1.4) V.

Parameter			min	typ	max	Units
ALC1 Characteristics (IPGA):						
Maximum Input Voltage (Note 16)					-0.5	dBV
Input Resistance:						
MIC(MIC_IN_L and MIC_IN_R pins) (Note 17)			5.6	9	13	kΩ
LINE(LIN and RIN pins) (Note 18)			117	184	260	kΩ
Step Size	MIC	LINE				
	+26dB ~ -10dB	+0dB ~ -36dB	0.1	0.5		dB
	-10dB ~ -18dB	-36dB ~ -44dB	0.1	1		dB
	-18dB ~ -30dB	-44dB ~ -56dB	0.1	2		dB
	-30dB ~ -42dB	-56dB ~ -68dB	-	2		dB
	-42dB ~ -54dB	-68dB ~ -80dB	-	4		dB
ADC Analog Input Characteristics: ALC1 = OFF						
Resolution					16	Bits
Input Voltage (Note 19) (Note 20)			-6.3	-5.5	-4.7	dBV
(Note 21)			-32.3	-31.5	-30.7	dBV
S/(N+D) (-2.0dBFS Output) (Note 20)			74	80		dB
(Note 21)			68	74		dB
DR (-60dBFS Output, A-Weighted) (Note 20)			80	86		dB
(Note 21)			73	79		dB
S/N (A-Weighted) (Note 20)			80	86		dB
(Note 21)			73	79		dB
Interchannel Isolation (Note 20)			80	100		dB
(Note 21)			80	100		dB
Interchannel Gain Mismatch (Note 20)					0.5	dB
(Note 21)					0.5	dB
DAC Analog Output Characteristics: Measured via OUT1/ROUT1. VOL=+7.5dB						
Resolution					16	Bits
S/(N+D) (0dBFS Input)			76	82		dB
DR (-60dBFS Input, A-Weighted)			82	88		dB
S/N (A-Weighted)			82	88		dB
Output Voltage (Note 19)			+1.2	+2	+2.8	dBV
Interchannel Isolation			80	100		dB
Interchannel Gain Mismatch					0.5	dB
Load Resistance			10			kΩ
Load Capacitance (Note 22)					20	pF

Note 16. When ALC1 is enabled, maximum input voltage becomes typically (VA – 0.13V) Vpp.
E.g. 2.67Vpp = -0.5dBV @ VA = 2.8V

Note 17. Input impedance of MIC changes from 8kΩ to 10kΩ by setting GAIN value, typically.

Note 18. Input impedance of LINE changes from 168kΩ to 200kΩ by setting GAIN value, typically.

Note 19. Input/Output voltage are proportional to VA voltage. 0.54 x VA.

Note 20. Input from LIN/RIN pins. AIN = "1". IPGA = 0dB.

Note 21. Input from MIC_IN_L and MIC_IN_R pins. AIN = "0". IPGA = +26dB.

Note 22. When output pin drives some capacitive load, some resistor should be added in series between output pin and capacitive load.

Parameter	min	typ	max	Units
Analog Volume Characteristics (OPGA):				
Input Resistance (OPGL and OPGR pins) (Note 23)	44	110	205	kΩ
Step Size: +0dB ~ -16dB	0.1	1		dB
-16dB ~ -38dB	0.1	2		dB
-38dB ~ -50dB	0.1	4		dB
Headphone-Amp Characteristics: R_L = 220Ω (Note 24)				
Output Voltage (FS-12dB = -17.5dBV Input) (Note 19)	-6.5	-5.7	-4.9	dBV
S/(N+D) (-3.4dBV Output)	40	53		dB
Output Noise Voltage (OPGA=MUTE, A-Weighted)		-80	-74	dBV
Interchannel Isolation	80	100		dB
Interchannel Gain Mismatch			0.5	dB
Load Resistance	220			Ω
Load Capacitance (Note 22)			20	pF
Speaker-Amp Characteristics: R_L= 8Ω, BTL, Input from MIN pin, ALC2=OFF				
Output Voltage	-4	-2	0	dBV
S/(N+D) (80mW Output)	40	55		dB
S/N (A-Weighted)	81	87		dB
Load Resistance	8			Ω
Load Capacitance (Note 22)			10	pF
Shutter Input: (SHT pin)				
Maximum Input Voltage (Note 19)			-5.5	dBV
Input Resistance	29	42	55	kΩ
BEEP Input: (BEEP pin)				
Maximum Input Voltage (Note 19)			-7.5	dBV
Feed-back Resistance	14	20	26	kΩ
Monaural Input: (MIN pin)				
Maximum Input Voltage (Note 19)			-5.5	dBV
Input Resistance (Note 25)	14	23	33	kΩ
Monaural Output: (MOUT pin) (Note 26)				
Output Voltage (Note 19)	-6.3	-5.5	-4.7	dBV
Load Resistance	10			kΩ
Load Capacitance (Note 22)			20	pF

Note 23. Input impedance of OPGA changes from 63kΩ to 158kΩ by setting GAIN value, typically.
Note 24. Input OPGL/OPGR pins. These values are measured via the following path.
Analog volume (OPGA=0dB) → Monaural Output (MOUT pin)
Note 25. Input impedance of MIN pin changes from 21kΩ to 25kΩ by setting ALC2 GAIN value, typically.
Note 26. OPGL/OPGR pins are input to –5.5dBV. These values are measured via the following path.
Analog volume (OPGA=0dB) → Monaural Output (MOUT pin)

Parameter	min	typ	max	Units
Power Supplies Current				
Power Up ($\overline{PD}$ = "H")				
All Circuit Power Up: (MIC=IPGA=ADC=DAC=VCOM=HPP=SPKP=LOUTP= "1")				
VA+VD		19.0	28.5	mA
MVDD (Note 27)		6.5	9.8	mA
HVDD:HP-Amp Normal Operation (LOUT=HP= "1", No Output)		3.5	5.3	mA
SVDD:SPK-Amp Normal Operation (SPPS= "1", No Output)		3.5	5.3	mA
ALC1+ADMIX+ADC: (IPGA=ADC=VCOM= "1") (Note 28)				
VA+VD		10.0	15.0	mA
DAC+LINEOUT: (DAC=LOUTP=VCOM= "1") (Note 29)				
VA+VD		8.0	12.0	mA
HVDD: LINEOUT Normal Operation (LOUT= "1", No Output)		1.5	2.3	mA
Power Down ($\overline{PD}$ = "L")				
VA+VD+HVDD+MVDD+SVDD (Note 30)			200	uA

Note 27. MPWR pin supplies 0mA.

Note 28. As VCOM = "1", HVDD of power supply current is 0.5mA (typ.) and power supply current of MVDD is 0.5mA (typ.).

Note 29. As VCOM= "1", power supply current is 0.5mA (typ.).

Note 30. In case of power-down, all digital input pins including clock (MCLK, BCLK and LRCK) pins are held "VD" or "DGND". $\overline{PD}$ pin is held "DGND".

FILTER CHARACTERISTICS

(Ta=25°C; VA=VD=2.6 ~ 3.3V; fs=48kHz; De-emphasis = OFF)

Parameter		Symbol	min	typ	max	Units
ADC Digital Filter (LPF):						
Passband (Note 31)	±0.1dB	PB	0		18.9	kHz
	-1.0dB		-	21.8	-	kHz
	-3.0dB		-	23.0	-	kHz
Stopband (Note 31)		SB	29.4			kHz
Passband Ripple		PR			±0.1	dB
Stopband Attenuation		SA	65			dB
Group Delay (Note 32)		GD	-	17.0	-	1/fs
Group Delay Distortion		ΔGD		0		us
ADC Digital Filter (HPF):						
Frequency Response (Note 31)	-3.0dB	FR	-	3.7	-	Hz
	-0.56dB		-	10	-	Hz
	-0.15dB		-	20	-	Hz
DAC Digital Filter:						
Passband (Note 31)	±0.1dB	PB	0		21.7	kHz
	-6.0dB		-	24.0	-	kHz
Stopband (Note 31)		SB	26.2			kHz
Passband Ripple		PR			±0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay (Note 32)		GD	-	14.8	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response	0 ~ 20.0kHz	FR		±0.5		dB

Note 31. The passband and stopband frequencies scale with fs (system sampling rate).
For example, ADC is PB=0.454*fs (@-1.0dB), DAC is PB=0.454*fs (@-0.1dB).

Note 32. The calculating delay time which occured by digital filtering, This time is from the input of analog signal to setting the 16 bit data of both channels on input register to the output register of ADC. And this time include group delay of HPF. For DAC, this time is from setting the 16 bit data of both channels on input register to the output of analog signal.

DC CHARACTERISTICS

(Ta=25°C; VA=VD=2.6 ~ 3.3V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	1.5	-	-	V
Low-Level Input Voltage	VIL	-	-	0.6	V
High-Level Output Voltage Iout=-200uA	VOH	VD-0.2	-	-	V
Low-Level Output Voltage Iout=200uA	VOL	-	-	0.2	V
Input Leakage Current	Iin	-	-	±10	uA

SWITCHING CHARACTERISTICS

(Ta=25°C; VA=VD=2.6 ~ 3.3V; C_L=20pF)

Parameter	Symbol	min	typ	max	Units
Control Clock Frequency					
Master Clock(MCLK) 256fs: Frequency	fCLK	2.048	12.288	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
384fs: Frequency	fCLK	3.072	18.432	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
Channel Select Clock (LRCK): Frequency	fs	8	48	50	kHz
Duty	Duty	45	50	55	%
Audio Interface Timing					
BCLK Period	tBLK	312.5			ns
BCLK Pulse Width Low	tBLKL	130			ns
Pulse Width High	tBLKH	130			ns
LRCK Edge to BCLK "↑" (Note 33)	tLRB	50			ns
BCLK "↑" to LRCK Edge (Note 33)	tBLR	50			ns
LRCK to SDTO(MSB) Delay Time	tLRM			80	ns
BCLK "↓" to SDTO Delay Time	tBSD			80	ns
SDTI Latch Hold Time	tSDH	50			ns
SDTI Latch Set up Time	tSDS	50			ns
Control Interface Timing					
CCLK Period	tCCK	200			ns
CCLK Pulse Width Low	tCCKL	80			ns
Pulse Width High	tCCKH	80			ns
CDTIO Latch Set Up Time	tCDS	50			ns
CDTIO Latch Hold Time	tCDH	50			ns
CSN "H" Time	tCSW	150			ns
CSN "↓" to CCLK "↑"	tCSS	50			ns
CCLK "↑" to CSN "↑"	tCSH	50			ns
CDTIO Output Delay Time	tDCD			70	ns
CSN "↑" to CDTO(Hi-Z) Time (Note 34)	tCCZ			70	ns
Reset Timing					
$\overline{PD}$ Pulse Width	tPDW	150			ns
$\overline{PD}$ "↑" to SDTO Delay Time	tPDV		8224		1/fs

Note 33. BCLK rising edge must not occur at the same time as LRCK edge.

Note 34. R_L=1kΩ/10% Change. (Pull-up operates for VD)

■ Timing Diagram

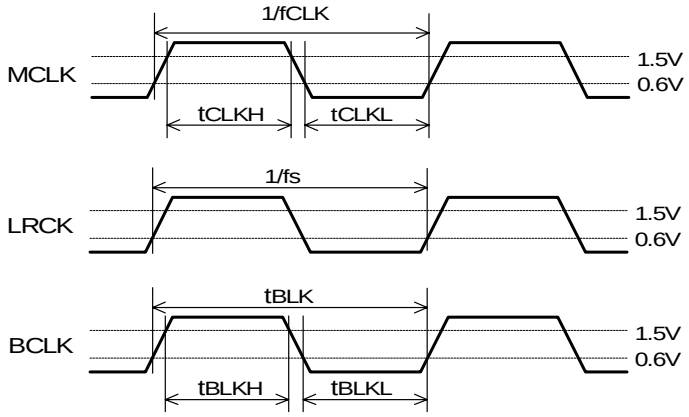


Figure 2. Clock Timing

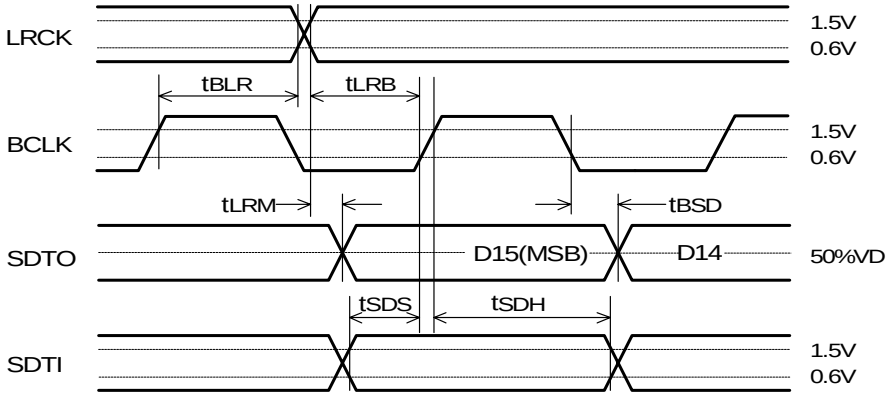


Figure 3. Audio Data Input/Output Timing

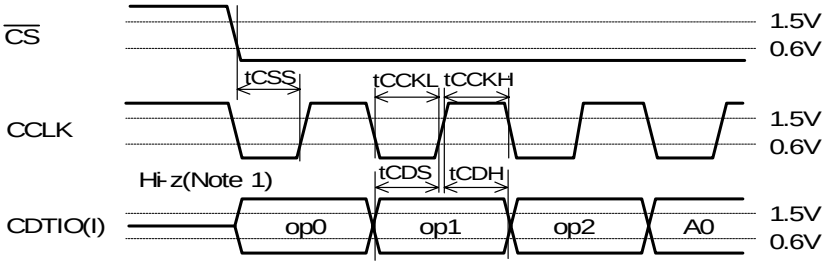


Figure 4. WRITE/READ Command Input Timing

Note:1. CDTIO pin should not be left floating except READ output timing as CDTIO pin is input pin then.

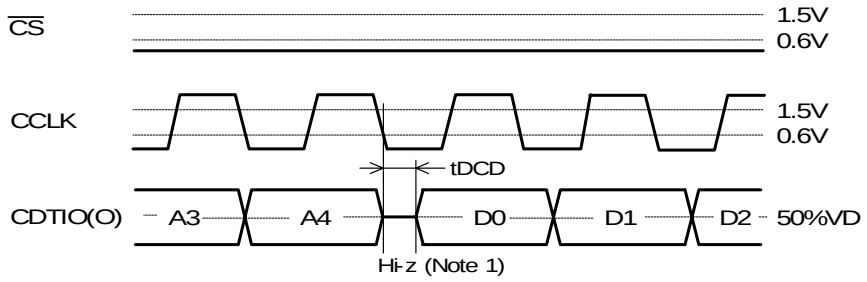


Figure 5. READ Data Input/Output Timing

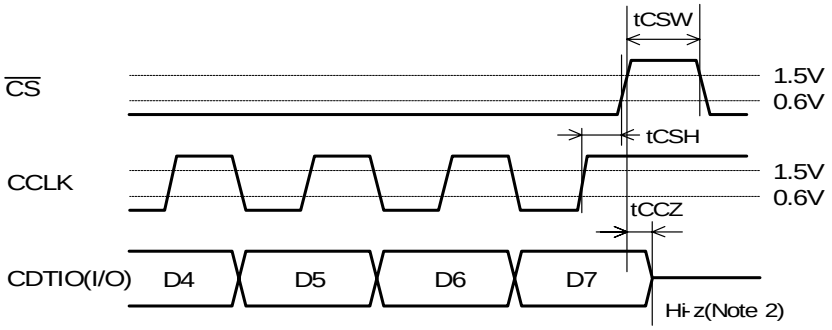


Figure 6. WRITE/READ Data Input/Output Timing

Notes:1. CDTIO pin should not be left floating except READ output timing as CDTIO pin is input pin then.
2. R_L = 1kΩ/10% Change. (Pull-up operates for VD.)

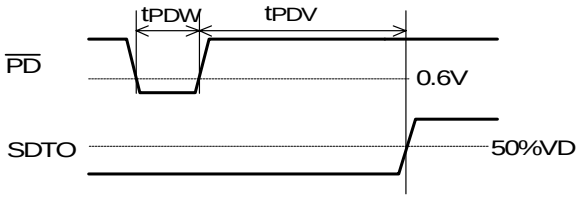


Figure 7. Reset Timing

OPERATION OVERVIEW

■ System Clock

The clock which are required to operate are MCLK (256fs/384fs), LRCK (fs), BCLK (32fs~). The master clock (MCLK) should be synchronized with LRCK but the phase is free of care.
The MCLK can be input 256fs or 384fs. When 384fs is input, the internal master clock is divided into 2/3 automatically.
* fs is sampling frequency.

When the synchronization is out of phase by changing the clock frequencies during normal operation, the AK4560A may occur click noise. In case of DAC, click noise is avoided by setting the inputs to "0".

All external clocks (MCLK, BCLK and LRCK) should always be present. If these clocks are not provided, the AK4560A may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4560A should be in the power-down mode. (Refer to the "Power Management Mode".)

■ System Reset

AK4560A should be reset once by bringing $\overline{\text{PD}}$ pin "L" upon power-up. After the system reset operation, the all internal AK4560A registers become initial value.

Initializing cycle is 8224/fs=171.3ms@fs=48kHz. During initializing cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". Output data of ADC settles data equivalent for analog input signal after initializing cycle. This cycle is not for DAC.

As a normal initializing cycle may not be executed, nothing writes at address 02H during initializing cycle.

■ Digital High Pass Filter

The ADC has HPF for the DC offset cancel. The cut-off frequency of HPF is 3.7Hz (@fs=48kHz) and it is -0.15dB at 22Hz. It also scales with the sampling frequency (fs).

■ Audio Interface Format

Data is shifted in/out the SDTI/SDTO pins using BCLK and LRCK inputs. The serial data is MSB-first, 2's compliment format, ADC is MSB justified and DAC is LSB justified.

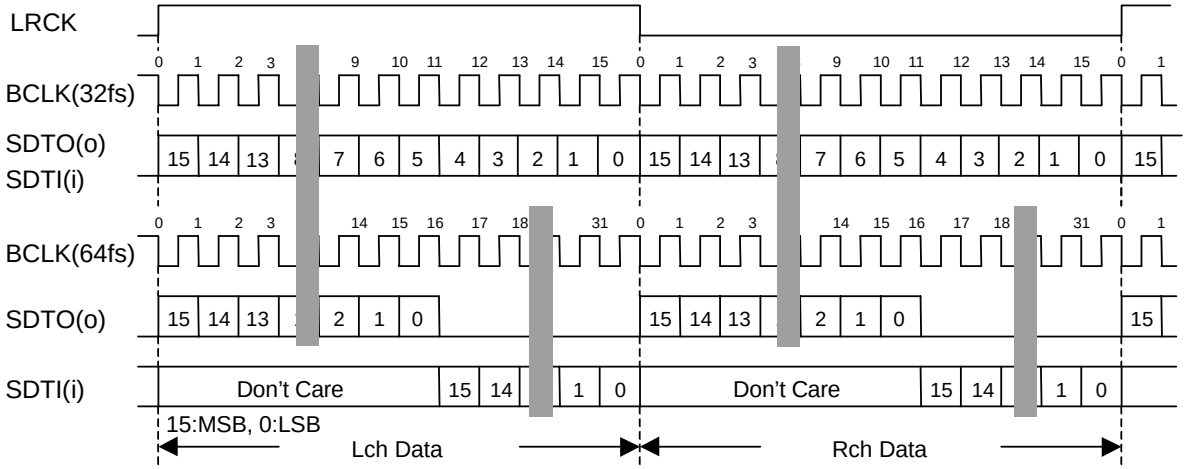


Figure 8. Audio Data Timing

■ Control Register Timing

The data on the 3-wire serial interface consists of op-code (3bit), address (LSB-first, 5bit) and control data (LSB-first, 8bit). The Transmitting data is output to each bit by "↓" of CCLK, the receiving data is latched by "↑" of CCLK. Writing data becomes effective by "↑" of $\overline{CS}$. Reading data becomes Hi-z (floating) by "↑" of $\overline{CS}$. $\overline{CS}$ should be held to "H" at no access.

CCLK always need 16 edges of "↑" during $\overline{CS}$. Reading/Writing of the address except 00H~09H are inhibited.
Reading/Writing of the control registers by except op1-0 = "11" are invalid.
In case of reading data, nothing is written to D0~D7 data.

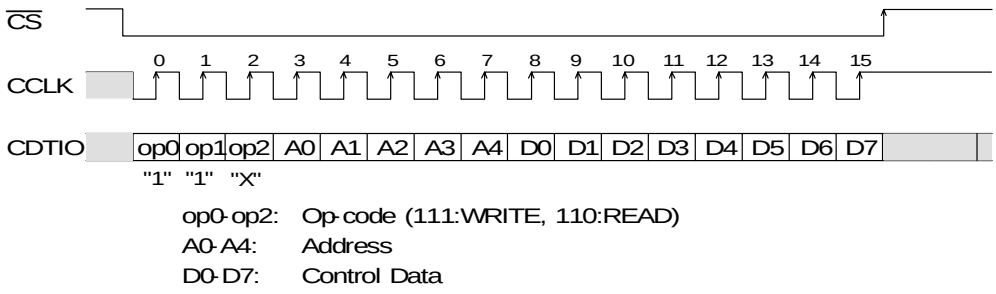


Figure 9. Control Data Timing

■ Register Map

The following registers are reset at $\overline{PD}$ pin = "L", then inhibits writing.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Signal Select 1	0	0	ADMIX	AOUT1	AOUT0	AIN	HPF	INT/EXT
01H	Signal Select 2	SPPS	ALCS	BEEPS	LOUT	MOUT	BEEPH	HP	VOL
02H	Power Management Control	LOUTP	SPKP	HPP	VCOM	DAC	ADC	IPGA	MIC
03H	Mode Control	0	0	VOL1	VOL0	MONO1	MONO0	DEM1	DEM0
04H	Timer Select	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
05H	ALC Mode Control 1	0	0	ZELM	LMAT1	LMAT0	FDATT	RATT	LMTH
06H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
07H	Operation Mode	0	0	STAT	ND	ALC2	FDIN	FDOUT	ALC1
08H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
09H	Output PGA Control	0	0	0	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0

Table 1. AK4560A Register Map

Signal Select 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Signal Select 1	0	0	ADMIX	AOUT1	AOUT0	AIN	HPF	INT/EXT
R/W		RD		R/W					
RESET		0	0	0	0	1	0	0	0

INT/EXT: Select Internal / External MIC (Refer to Figure 12 and Figure 13.)
- 0: Internal MIC (RESET)
- 1: External MIC

INT/EXT bit and INT_EXT_DET pin are ORed.
When this function is controlled by INT_EXT_DET pin, INT_EXT bit is fixed to "0". When this function is controlled by INT/EXT bit, INT_EXT_DET pin is fixed to "L".

HPF: Select HPF-Amplifier
- 0: Disable (RESET)
- 1: Enable

When HPF bit is "0", HPF-Amp becomes a unity gain buffer.
When External MIC (INT/EXT bit = "1" or INT_EXT_DEC pin = "H") is selected, HPF bit is ignored.

AIN: Select input signal of ALC1 and change gain table of IPGA.
- 0: MIC (RESET)
- 1: LINE

AOUT1-0: Select input signal of LINEOUT or Analog Volume (OPGA)

ON/OFF of DAC is selected by AOUT0 bit and ON/OFF of Analog Through Mode is selected by AOUT1.
- 00: Input signal is OFF. Common voltage is output.
- 01:DAC (RESET)
- 10: Analog Through Mode (Output signal of ALC1)
- 11: Output signal of DAC and Analog Through are mixed.

ADMIX: Output signal of ALC1 and input signal of SHT pin are mixed.
- 0: Disable (RESET)
- 1: Enable

Signal Select 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Signal Select 2	SPPS	ALCS	BEEPS	LOUT	MOUT	BEEPH	HP	VOL
R/W		R/W							
RESET		0	0	0	0	0	0	0	0

VOL: Select signal of analog volume (OPGA) to input to Headphone-Amp
0: OFF (RESET)
1: ON. Output signal of analog volume is input to Headphone-Amp.

HP: Select output signal of Headphone-Amp
0: OFF. Power-Save-Mode. Output HVCM voltage (RESET)
1: ON

BEEPH: Select BEEP signal to input to Headphone-Amp
0: OFF (RESET)
1: ON. Input BEEP signal to Headphone-Amp.

MOUT: Select monaural output (Mixing = (L+R)/2).
0: OFF. Output VCOM voltage. (RESET)
1: ON

LOUT: Select LINEOUT
0: OFF. Power-Save-Mode. Output HVCM voltage. (RESET)
1: ON

BEEPS: Select BEEP/Shutter signal to input to Speaker-Amp
0: OFF (RESET)
1: ON. BEEP or Shutter signal is input to Speaker-Amp.

ALCS: Select output signal of ALC2 to input to Speaker-Amp
0: OFF (RESET)
1: ON. Output signal of ALC2 is input to Speaker-Amp.

SPPS: Speaker-Amp Power-Save-Mode
0: Power-Save-Mode
SP0 pin becomes Hi-z and SP1 pin is output to SVDD/2 voltage. (RESET)
1: Normal operation

Power Management Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Power Management Control	LOUTP	SPKP	HPP	VCOM	DAC	ADC	IPGA	MIC
R/W		R/W							
RESET		1	1	1	1	1	1	1	1

MIC: MIC Block (Pre-Amp, EQ-Amp, HPF-Amp and MPWR) Power Control.
0: OFF. Output pins are Hi-z.
1: ON (RESET)

IPGA: IPGA (ALC1) Power Control
0: OFF
1: ON (RESET)

ADC: ADC Power Control
0: OFF. SDTO pin is output "L".
1: ON (RESET)
When ADC bit changes from "0" to "1", initializing cycle (8224/fs=171.3ms@fs=48kHz) starts. After initializing cycle, digital data of ADC is output.

DAC: DAC Power Control
0: OFF
1: ON (RESET)

VCOM: Common Voltage (VCOM, HVCM and MVCM) Power Control
0: OFF
1: ON (RESET)

HPP: Headphone-Amp Power Control (Including OPGA, BEEP and HP-Amp)
0: OFF. Output of Headphone-Amp becomes "L" (AGND).
1: ON (RESET)

SPKP: Speaker Block Power Control (Including OPGA, BEEP, MOUT, ALC2 and Speaker-Amp)
0: OFF. Output of Speaker-Amp is Hi-z.
1: ON (RESET)

LOUTP: Lineout Power Control
0: OFF. Output pin is Hi-z.
1: ON (RESET)

Analog volume (OPGA) are enabled when SPKP bit = "1" or HPP bit = "1".

These bits can be partially powered-down by ON/OFF ("1" / "0"). When $\overline{\text{PD}}$ pin goes "L", all the circuit in AK4560A can be powered-down regardless of these bits in the address.

When bit in this address goes all "0", all the circuits in AK4560A can be also powered-down. But contents of registers are kept.

When each block is operated, VCOM bit must go "1". VCOM bit can write "0" when all bits in this address can be "0".

Except the case of IPGA=ADC=DAC=SPKP=HPP= "0" or $\overline{\text{PD}}$ pin = "L", MCLK, BCLK and LRCK should not be stopped.

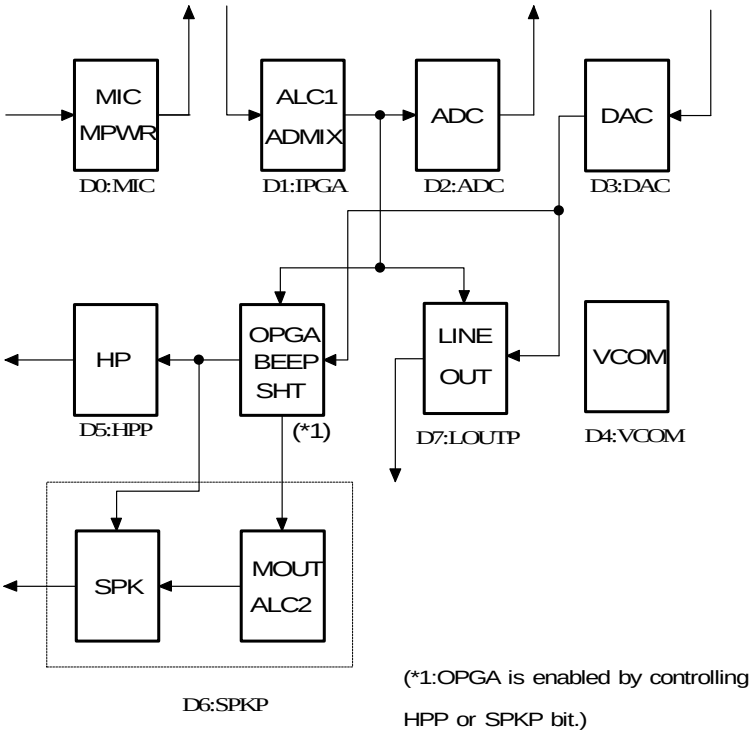


Figure 10. Power Management Control

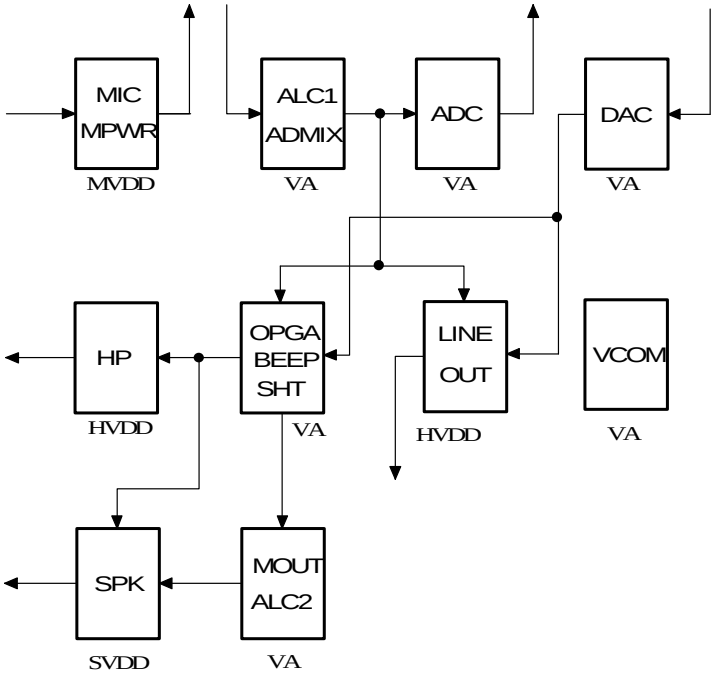


Figure 11. Analog Power Supply Source of Each Block

Mode Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control	0	0	VOL1	VOL0	MONO1	MONO0	DEM1	DEM0
R/W		RD		R/W					
RESET		0	0	1	0	0	0	0	1

DEM1-0: Select De-emphasis Frequency

The AK4560A includes the digital de-emphasis filter (tc = 50/15us) by IIR filter. The filter corresponds to three sampling frequencies (32kHz, 44.1kHz and 48kHz). The de-emphasis filter selected DEM0 and DEM1 registers are enabled for input audio data.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	RESET
1	0	48kHz	
1	1	32kHz	

Table 2. De-emphasis Frequencies

MONO1-0: Select digital data to input to DAC

MONO1	MONO0	LOUT	ROUT	
0	0	Lch	Rch	RESET
0	1	Lch	Lch	
1	0	Rch	Rch	
1	1	Rch	Lch	

Table 3. Select digital data to input to DAC

VOL1-0: LINEOUT Gain Setting

As signal level of LINEOUT is different by VA power supply voltage, a gain of LINEOUT is set by VOL1-0 bits.

VOL1	VOL0	Gain	VA Voltage	
1	0	+7.5dB	2.8V	RESET
1	1	+6.9dB	3.0V	

Table 4. LINEOUT volume setting

Timer Select

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Timer Select	FDTM1	FDTM0	ZTM1	ZTM0	WTM1	WTM0	LTM1	LTM0
R/W		R/W							
RESET		1	0	1	0	1	0	0	0

LTM1-0: ALC1 limiter operation period at zero crossing disable (ZELM = "1")

The IPGA value is changed immediately. When the IPGA value is changed continuously, the change is done by the period specified by LTM1-0 bits.

LTM1	LTM0	ALC1 Limiter Operation Period				
			48kHz	44.1kHz	32kHz	
0	0	0.5/fs	10us	11us	16us	RESET
0	1	1/fs	21us	23us	31us	
1	0	2/fs	42us	45us	63us	
1	1	4/fs	83us	91us	125us	

Table 5. ALC1 Limiter Operation Period at zero crossing disable (ZELM = "1")

WTM1-0: ALC1 Recovery Waiting Period

A period of recovery operation when any limiter operation does not occur during ALC1 operation.

Recovery operation is done at period set by WTM1-0 bits.

When the input signal level exceeds auto recovery waiting counter reset level set by LMTH bit, the auto recovery waiting counter is reset.

The waiting timer starts when the input signal level becomes below the auto recovery waiting counter reset level.

WTM1	WTM0	ALC1 Recovery Operation Waiting Period				
			48kHz	44.1kHz	32kHz	
0	0	512/fs	10.7ms	11.6ms	16.0ms	
0	1	1024/fs	21.3ms	23.2ms	32.0ms	
1	0	2048/fs	42.6ms	46.4ms	64.0ms	RESET
1	1	4096/fs	85.2ms	92.8ms	128.0ms	

Table 6. ALC1 Recovery Operation Waiting Period

ZTM1-0: Zero crossing timeout at writing operation by uP and ALC1 recovery operation

When IPGA of each L/R channels do zero crossing or timeout independently, the IPGA value is changed by uP WRITE operation or ALC1 recovery operation

ZTM1	ZTM0	Zero Crossing Timeout Period				
			48kHz	44.1kHz	32kHz	
0	0	513/fs	10.7ms	11.6ms	16.0ms	
0	1	1025/fs	21.4ms	23.2ms	32.0ms	
1	0	2049/fs	42.7ms	46.5ms	64.0ms	RESET
1	1	4097/fs	85.4ms	92.9ms	128.0ms	

Table 7. Zero Crossing Timeout

FDTM1-0: FADEIN/OUT Cycle Setting

The FADEIN/OUT operation is done by a period set by FDTM1-0 bits when FDIN or FDOUT bits are set to "1". When IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed.

FDTM1	FDTM0	FADEIN/OUT Period				
			48kHz	44.1kHz	32kHz	
0	0	512/fs	10.7ms	11.6ms	16.0ms	
0	1	1024/fs	21.3ms	23.2ms	32.0ms	
1	0	2048/fs	42.6ms	46.4ms	64.0ms	RESET
1	1	4096/fs	85.2ms	92.8ms	128.0ms	

Table 8. FADEIN/OUT Period

ALC Mode Control 1

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
05H	ALC Mode Control 1	0	0	ZELM	LMAT1	LMAT0	FDATT	RATT	LMTH
R/W		R/W							
RESET		0	0	0	0	0	0	0	0

LMTH: ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

The ALC1 limiter detection level and the ALC1 recovery counter reset level are of uneven quality about ±2dB.

LMTH	ALC1 Limiter Detection Level	ALC1 Recovery Waiting Counter Reset Level	
0	ADC Input ≥ -6.0dB	-6.0dB > ADC Input ≥ -8.0dB	RESET
1	ADC Input ≥ -4.0dB	-4.0dB >ADC Input ≥ -6.0dB	

Table 9. ALC1 Limiter Detection Level / Recovery Waiting Counter Reset Level

RATT: ALC1 Recovery GAIN Step

During the ALC1 Recovery operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, RATT = "1" is set, IPGA changes to 32H by the ALC1 recovery operation, the input signal level is gained by 1dB (=0.5dB x 2).
When the IPGA value exceeds the reference level (REF6-0), the IPGA value does not increase.

RATT	GAIN STEP	
0	1	RESET
1	2	

Table 10. ALC1 Recovery GAIN Step Setting

FDATT: FADEIN/OUT ATT Step

During the FADEIN/OUT operation, the number of steps changed from current IPGA value is set. For example, when the current IPGA value is 30H, FDATT = "1" is set, IPGA changes to 32H(at FADEIN operation) or 2EH (at FADEOUT operation) by the FADEIN/OUT operation, the input signal level is changed by 1dB (=0.5dB x 2).
When the IPGA value exceeds the reference level (REF6-0), the IPGA value does not increase.

FDATT	ATT STEP	
0	1	RESET
1	2	

Table 11. FADEIN/OUT ATT Step Setting

LMAT1-0: ALC1 Limiter ATT Step

During the ALC1 limiter operation, when either Lch or Rch exceeds the ALC1 limiter detection level set by LMTH, the number of steps attenuated from current IPGA value is set. For example, when the current IPGA value is 68H in the state of LMAT1-0 bit = "11", it becomes IPGA = 64H by the ALC1 limiter operation, the input signal level is attenuated by 2dB (=0.5dB x 4).
When the attenuation value exceeds IPGA = "00" (MUTE), it clips to "00".

LMAT1	LMAT0	ATT STEP	
0	0	1	RESET
0	1	2	
1	0	3	
1	1	4	

Table 12. ALC1 Limiter ATT Step Setting

ZELM: Enable zero crossing detection at ALC1 Limiter operation

0: Enable (RESET)
1: Disable

In case of ZELM = "0", IPGA of each L/R channel do zero crossing or timeout independently, the IPGA value is changed by ALC1 operation. Zero crossing timeout is the same as ALC1 recovery operation. In case of ZELM = "1", the IPGA value is changed immediately.

ALC Mode Control 2

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	ALC Mode Control 2	0	REF6	REF5	REF4	REF3	REF2	REF1	REF0
R/W		RD	R/W						
RESET		0	1	1	0	0	0	0	0

REF6-0: Set the Reference value at ALC1 Recovery Operation

During the ALC1 recovery operation, if the IPGA value exceeds the setting reference value by Gain operation, IPGA does not become the larger than the reference value.

For example, when REF=30H, RATT=2, IPGA=2FH and IPGA will become 2FH + 2step = 31H by the ALC1 recovery operation, but the IPGA value becomes 30H as REF value is 30H.

	DATA	GAIN(dB)		STEP	LEVEL
		MIC	LINE		
RESET	60H	+26.0	+0.0	0.5dB	73
	5FH	+25.5	-0.5		
	5EH	+25.0	-1.0		
	:	:	:		
	2CH	+0.0	-26.0		
	2BH	-0.5	-26.5		
	:	:	:		
	19H	-9.5	-35.5		
	18H	-10.0	-36.0		
	17H	-11.0	-37.0	1dB	8
	16H	-12.0	-38.0		
	:	:	:		
	11H	-17.0	-43.0		
	10H	-18.0	-44.0		
	0FH	-20.0	-46.0	2dB	12
	0EH	-22.0	-48.0		
	:	:	:		
	05H	-40.0	-66.0		
	04H	-42.0	-68.0		
	03H	-46.0	-72.0	4dB	3
	02H	-50.0	-76.0		
	01H	-54.0	-80.0		
	00H	MUTE	MUTE		1

Table 13. Setting Reference Value at ALC1 Recovery Operation

Operation Mode

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Operation Mode	0	0	STAT	ND	ALC2	FDIN	FDOUT	ALC1
R/W		RD			R/W				
RESET		0	0	0	0	1	0	0	0

ALC1: ALC1 Enable Flag
0: Disable (RESET)
1: Enable
FDOUT: FADEOUT Enable Flag
0: Disable (RESET)
1: Enable
FDIN: FADEIN Enable Flag
0: Disable (RESET)
1: Enable
* When FADEIN or FADEOUT operation is done, ALC1 bit should always be "1".

ALC2: ALC2 Enable Flag
0: Disable
1: Enable (RESET)
After initializing cycle (2048/fs=42.7ms@fs=48kHz), ALC2 is enabled. This initializing cycle starts when $\overline{PD}$ pin change "L" to "H" or SPKP bit change from "0" to "1".

ND: REF6-0 value of ALC1 is decreased to –3.5dB.
0: Keep REF6-0 value of ALC1 (RESET)
1: Decrease –3.5dB from REF6-0 value of ALC1
This bit and ND pin are ORed.
When this function is controlled by ND pin, ND bit is fixed to "0". When this function is controlled by ND bit, ND pin is fixed to "L".

STAT: Status Flag
0: In case of ALC1 (including FADEIN, FADEOUT and Noise Decreasing function) operation or initializing cycle. (RESET)
1: Manual Mode

STAT bit is "0" during initilizing operation after exiting power-down by $\overline{PD}$ pin. After the finish of the initilizing operation, STAT bit becomes "1".

During the ALC1 operation, STAT bit becomes "1" after the max "1" ATT/GAIN operation is completed by internal state.

Input PGA Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	Input PGA Control	0	IPGA6	IPGA5	IPGA4	IPGA3	IPGA2	IPGA1	IPGA0
R/W		RD	R/W						
RESET		0	0	1	0	1	1	0	0

IPGA6-0: Input Analog PGA; 97 levels

	DATA	GAIN(dB)		STEP	LEVEL
		MIC	LINE		
	60H	+26.0	+0.0	0.5dB	73
	5FH	+25.5	-0.5		
	5EH	+25.0	-1.0		
	:	:	:		
RESET	2CH	+0.0	-26.0		
	2BH	-0.5	-26.5		
	:	:	:		
	19H	-9.5	-35.5		
	18H	-10.0	-36.0		
	17H	-11.0	-37.0	1dB	8
	16H	-12.0	-38.0		
	:	:	:		
	11H	-17.0	-43.0		
	10H	-18.0	-44.0		
	0FH	-20.0	-46.0	2dB	12
	0EH	-22.0	-48.0		
	:	:	:		
	05H	-40.0	-66.0		
	04H	-42.0	-68.0		
	03H	-46.0	-72.0	4dB	3
	02H	-50.0	-76.0		
	01H	-54.0	-80.0		
	00H	MUTE	MUTE		1

Table 14. Input Gain Setting

Output PGA Control

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
09H	Output PGA Control	0	0	0	OPGA4	OPGA3	OPGA2	OPGA1	OPGA0
R/W		RD			R/W				
RESET		0	0	0	1	1	1	1	1

OPGA4-0: Output analog PGA; 32 Level; 0dB ~ -50dB, Mute.

These bits can change volume of Headphone-Amps and Speaker-Amp.
This volume includes zero crossing detection, and it does L/R channels independently. Zero crossing timeout is proportional to sampling rate, To = 512/fs.
10.7ms = 512/fs@fs=48kHz
16ms = 512/fs@fs=32kHz

	DATA	GAIN(dB)	STEP	LEVEL
RESET	1FH	+0	1dB	17
	1EH	-1		
	1DH	-2		
	:	:		
	10H	-15		
	0FH	-16		
	0EH	-18	2dB	11
	0DH	-20		
	:	:		
	05H	-36		
	04H	-38		
	03H	-42	4dB	3
	02H	-46		
	01H	-50		
	00H	Mute		1

Table 15. ATT value of Analog Volume

FUNCTION DETAIL

■ MIC BLOCK

MIC block includes 2-inputs selectors, Internal MIC or External MIC Mode can be selected by MIC bit. (Refer to Figure 12 and Figure 13)

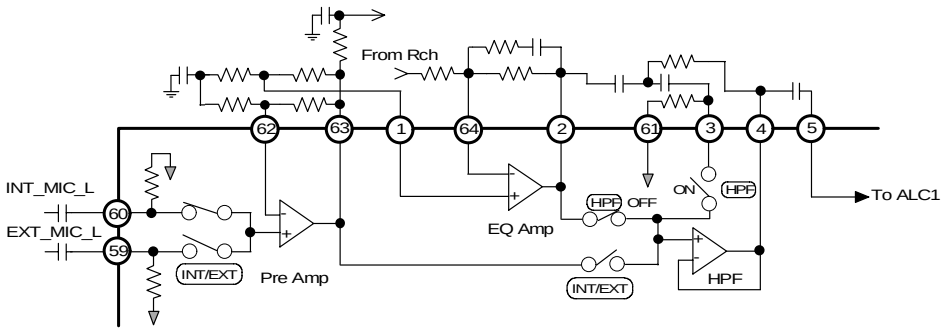


Figure 12. Internal path at selecting Internal MIC Mode (HPF OFF)

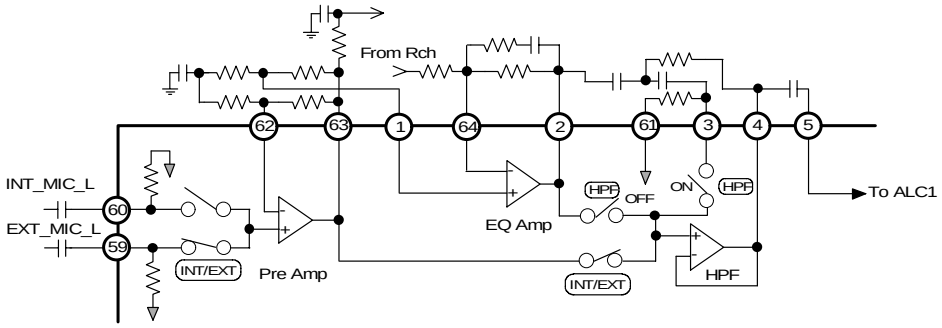


Figure 13. Internal path at selecting External MIC Mode (HPF OFF)

1. Pre- Amp

Pre-Amp is non-inverting amplifier and internally biased to MVCM voltage with 100kΩ (typ.). Gain value of Pre-Amp is adjusted by external resistor.

Gain (1+Rf/Ri) of Pre-Amp should use a range of +18~30dB.

An external capacitor needs to cancel DC gain. Cut-off frequency is decided by a external input resistor (Ri) and a capacitor (C).

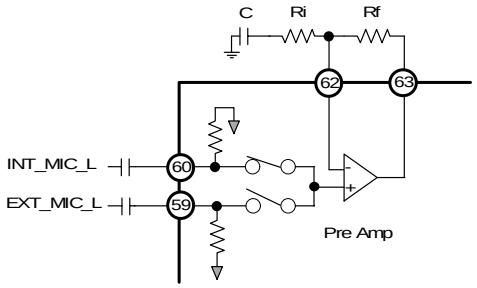


Figure 14. Pre-Amp

2. EQ-Amp

EQ-Amp is block to emphasize a stereo feeling at using Internal MIC Mode.
EQ-Amp can be emphasized by adding the output signal from pre-amplifier and the reverse channel differentially. When External MIC Mode is selected, EQ-Amp does not connect.

3. HPF-Amp

To cancel wind-noise, AK4560A has the HPF-Amp which is non-inverting amplifier, 2^{nd} order high pass filter and gain of 0dB. The HPF-Amp can be ON/OFF by controlling the internal registers. In case of OFF, HPF-Amp becomes a unity gain buffer. This HPF-Amp can use when Internal MIC Mode is selected. In case of External MIC Mode, the control of HPF-Amp is invalid and becomes a unity gain buffer.

4. Power Supply for MIC

Power Supply for microphone is supplied from MPWR pin. Output voltage is MVDD – 1.4V (typ) . For example, MPWR pin outputs 2.5V at MVDD = 3.9V. And MPWR pin can supply the current until 3mA.
When MIC bit is “0”, the power supply current can be stopped.

■ Shutter Signal Input

1. Recording

When ADMIX bit is "1", input signal from SHT pin is attenuated to –4.5dB internally and is mixed to output signal from ALC1 by a gain of 0dB. Input impedance of SHT pin is 42kΩ (typ.).
When ADMIX bit is "0", output signal of ALC1 is input to ADC by a gain of 0dB.

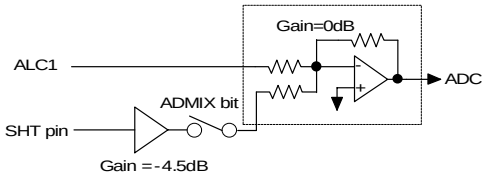


Figure 15. ADMIX Block Diagram

2. Playback

When BEEPS bit is "1", input signal from SHT pin can be input to Speaker-Amp. This signal level can be adjusted by an external resistor (R2). An internal resistor value (Rf) is 20k ± 30% Ω. For example, when R2 is 20kΩ, the final output level from Speaker-Amp becomes "$20\log_{10}$(20k/20k) dB + 5.6dB (Speaker-Amp) = +5.6dB". (Refer to Figure 16)

■ BEEP Input

When BEEPH bit is "1", input signal from BEEP pin can be input to Headphone-Amp. When BEEPS bit is "1", input signal from BEEP pin can be input to Speaker-Amp.
This signal level can be adjusted by an external resistor (R1). An internal resistor value (Rf) is 20k ± 30% Ω. For example, when R1 is 20kΩ, the final output level from Headphone-Amp becomes
"$20\log_{10}$(20k/20k) dB + 11.8dB (Headphone-Amp block) = +11.8dB". (Refer to Figure 16)

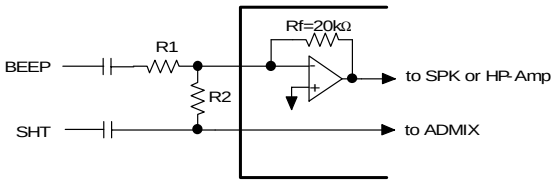


Figure 16. Block Diagram of BEEP and SHT pin

■ Analog Volume (OPGA)

The AK4560A includes the 0dB ~ -50dB & MUTE analog volume with zero crossing detection for headphone and speaker. Zero crossing is detected on L/R channels independently. Zero crossing timeout (To) is proportional to sampling rate. To=512/fs@fs=48kHz=10.7ms.

OPGA is not written during counting zero crossing timers. In case of writing control register continually, the change of OPGA should be written after zero crossing timeout and over. If OPGA is changed by writing to control register before zero crossing detection, OPGA value of L/R channels may not give a difference level.

Usually, to remove the offset of DAC, it needs a capacitor (Ca) between LOUT2/ROUT2 and OPGL/OPGR. The cut-off frequency is decided by capacity of Ca and input impedance (typ. 110kΩ) of OPGL/OPGR.

Power supply for analog volume enables when speaker or headphone of power management bits is "1". (SPKP bit = "1" or HPP bit = "1")

The initial value is 0dB at exiting power-down.

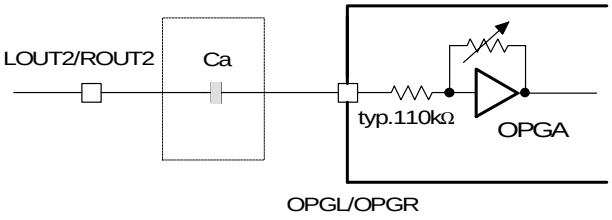


Figure 17. Connect LOUT2/ROUT2 with OPGL/OPGR

■ LINE input

In case of LINE input, input impedance of LIN/RIN is 184kΩ (typ.) and centered around the VCOM voltage. When input voltage is +2dBV, LIN/RIN pins should be input to –5.5dBV@VA=2.8V and less after dividing resistors externally. When LIN bit is "1", LINE input is selected. Then IPGA table of ALC1 is changed to LINE side.

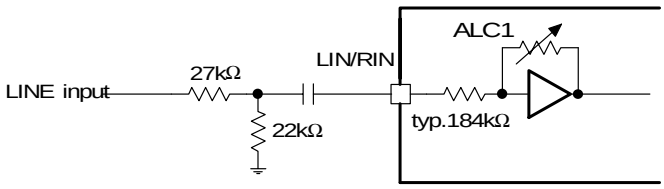


Figure 18. Example of LINEIN at VA=2.8V

■ MUTE pin Function

When MUTE pin is “H”, output signals of LINEOUT, Headphone and Speaker is muted by force, and these signals are output to common voltage. Then switches of AOUT1-0, VOL, BEEPH, ALCS and BEEPS become “OFF” by force. When MUTE pin is “L”, these output signals are normal operation.

■ Analog Through Mode

This mode can be input to playback circuits after adding ALC1 output signal and shutter signal. This mode can be controlled by AOUT1-0 bits.

■ Noise decreasing function

When ND pin is “H” or ND bit is “1”, the setting reference value of ALC1 (REF6-0 bits) is decreased to –3.5dB. Then this mode is doing at every 1step with zero crossing detection. The time constant is about 12sec@fs=32kHz and 8sec@fs=48kHz.

When ND pin (or ND bit) changes from “H” (or “1”) to “L” (or “0”), the current reference value operates toward the setting reference value of ALC1. Then this mode is doing at every 1step with zero crossing detection. The time constant is about 3sec@fs=32kHz and 3sec@fs=48kHz.

In case of doing the FADEIN/FADEOUT operation during noise decreasing operation, the FADEIN/FADEOUT operation starts from the current IPGA value.

■ LINEOUT

The signals of DAC or Analog Through Mode are gained to +7.5dB (@VA= 2.8V, Vol1-0 bit = "10", refer to Figure 22) internally, and its signal is output from LINEOUT. This gain can be changed by VOL1-0 bits.

Output level of LINEOUT is +2dBV and centered HVCM voltage. Load resistance is min. 10kΩ. (Refer to Figure 19)

Power supply voltage for LINEOUT is supplied from HVDD voltage. The supplied HVDD voltage does not change output level of LINEOUT. But if HVDD voltage is low, a distortion characteristic of LINEOUT is bad.

LOUT1 and ROUT1 outputs are muted by LOUT bit. Then LOUT1 and ROUT1 pins output HVCM voltage and enter Power-Save-Mode. (Refer to Figure 20). When LOUTP bit is "0", LOUT1 and ROUT1 pins become Power-Down-Mode and output signal is Hi-z. (Refer to Figure 21)

When $\overline{PD}$ pin changes from "L" to "H" after power-up, LOUT1 and ROUT1 pins become Power-Save-Mode. In Power-Save-Mode, LOUT1 and ROUT1 pins gradually become HVCM voltage via an internal resistor (R1: typ.200kΩ) from Hi-z to decrease a pop noise. And when Power OFF, the pop noise can be decreased by controlling via Power-Save-Mode.

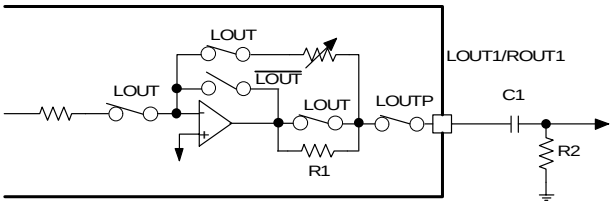


Figure 19. LINEOUT Normal Operation

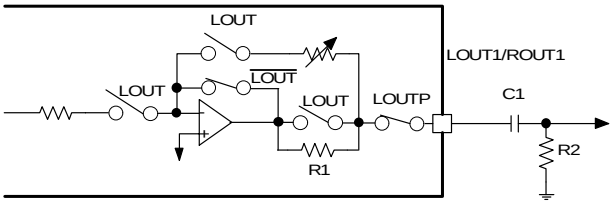


Figure 20. LINEOUT Power-Save-Mode

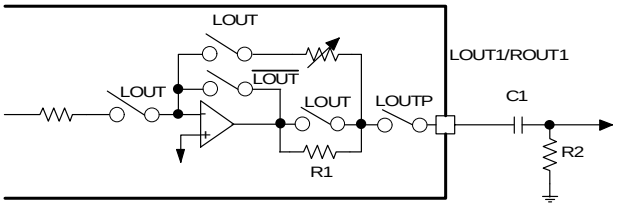


Figure 21. LINEOUT Power-Down-Mode

■ Headphone-Amps

Power supply voltage for Headphone-Amp is supplied from HVDD pin and centered around HVCM voltage. Load resistance of headphone output is min.220Ω. (Refer to Figure 23).

Output level of Headphone-Amp is gained to +11.8dB internally, and THD+N is 1% at –3.4dBV(1.9Vpp) output level. (Refer to Figure 22)

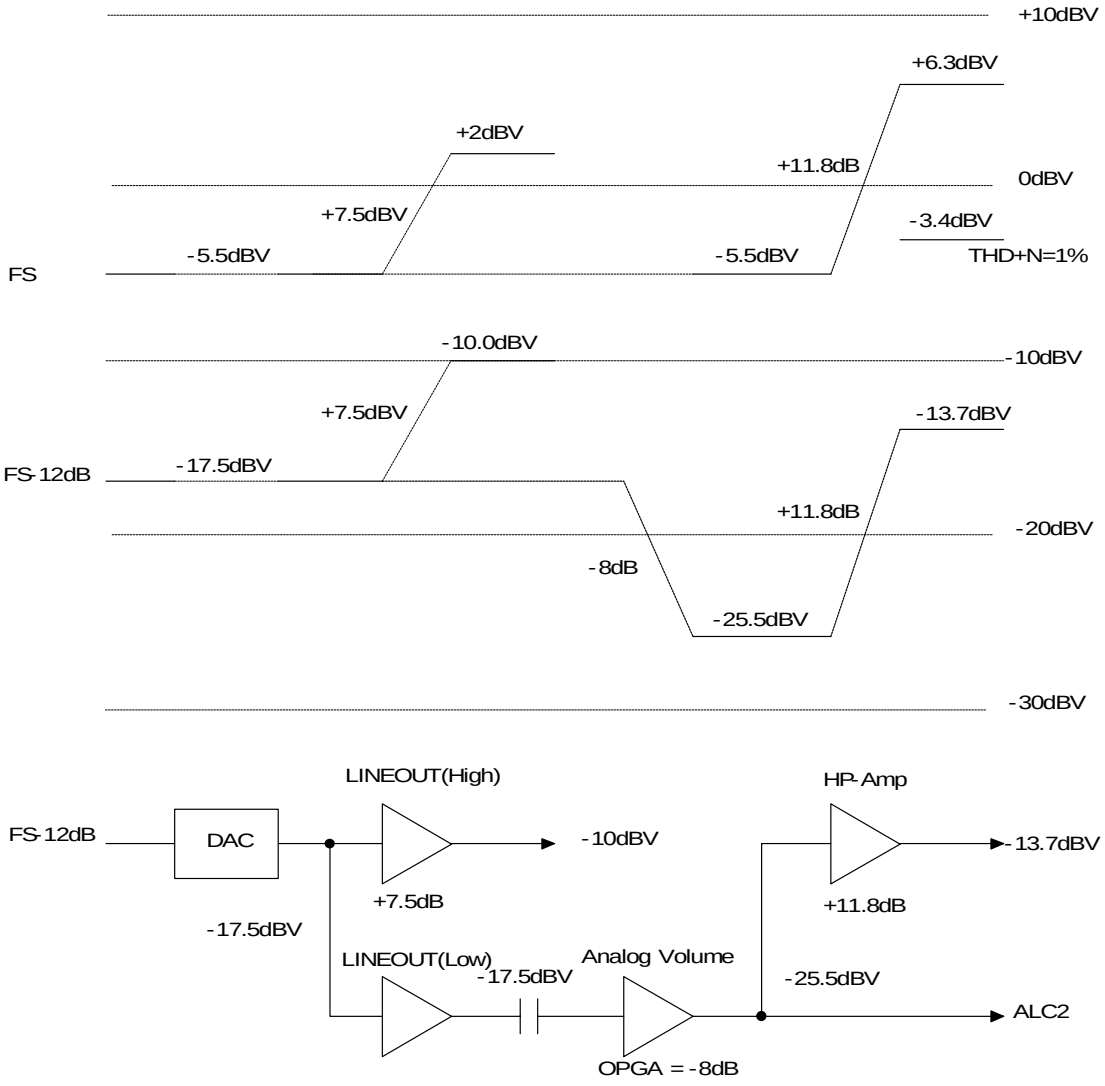


Figure 22. LINEOUT and Headphone-Amp Level Diagram (@VA=2.8V,OPGA=-8dB,VOL1-0=+7.5dB)

When HP bit is “0”, output signal is muted and enter the Power-Save-Mode. Then HPL and HPR pins output HVCM voltage. (Refer to Figure 24)

When HPP bit is “0”, Headphone-Amp is powered down perfectly. Then HPL and HPR pins go “L” (AGND). (Refer to Figure 25)

When $\overline{\text{PD}}$ pin changes from “L” to “H” after power-up, HPL and HPR pins become Power-Save-Mode. In Power-Save-Mode, output voltage of HPL and HPR pins gradually change from AGND to HVCM voltage by the time constants of an internal resistor (R2: typ.10kΩ) and an external capacitor (C1). (Refer to Figure 24)
In case of entering the normal operation mode after that, HP bit changes from “0” to “1”.

In the Power-Down-Mode ($\overline{\text{PD}}$ pin = “L” or HPP bit = “0”), output voltage of HPL and HPR pins gradually change from AGND to HVCM voltage by the time constants of an internal resistor (R2:typ.10kΩ) and an external capacitor (C1). (Refer to Figure 25)

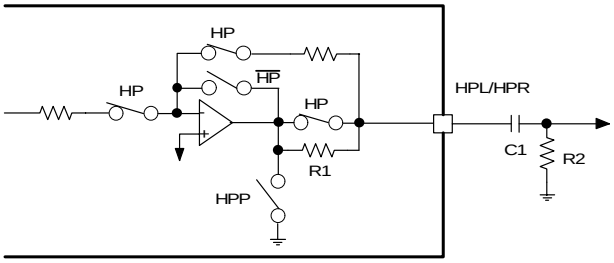


Figure 23. Headphone-Amps Normal Operation

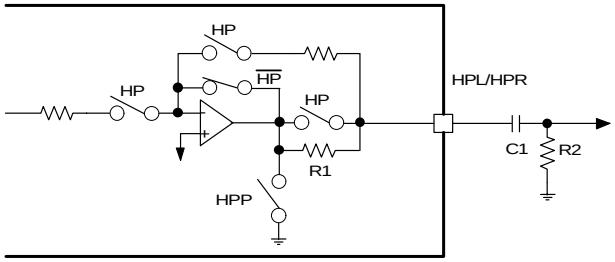


Figure 24. Headphone-Amps Power-Save-Mode

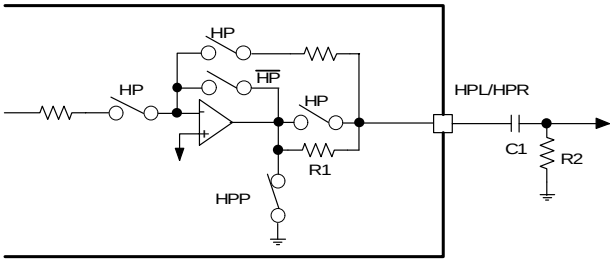


Figure 25. Headphone-Amps Power-Down-Mode

■ SPEAKER BLOCK

The output signal from analog volume is converted into a monaural signal, its signal is input to speaker-Amp via ALC2 circuit. This speaker-Amp is a monaural output by BTL, can be output to maximum 80mW at 8Ω. (Refer to Figure 26)

Speaker Blocks (MOUT, ALC2 and Speaker-Amp) can be powered ON/OFF by controlling SPKP bit.
When SPKP bit is "0", MOUT, SP0 and SP1 pins go Hi-z. (Refer to Figure 28)

When SPPS bit is "0", Speaker-Amp becomes Power-Save-Mode. (Refer to Figure 27)
Then SP0 pin goes Hi-z and SP1 pin is output to SVDD/2 via R1 (typ.100k Ω).

When $\overline{\text{PD}}$ pin changes from "L" to "H" after power-up, SP0 and SP1 pins become Power-Save-Mode. In Power-Save-Mode, SP0 and SP1 pins gradually become HVCM voltage via an internal resistor (R1: typ.200kΩ) from Hi-z to decrease a pop noise. And when Power OFF (SPKP = "0"), the pop noise can be decreased by controlling via Power-Save-Mode.

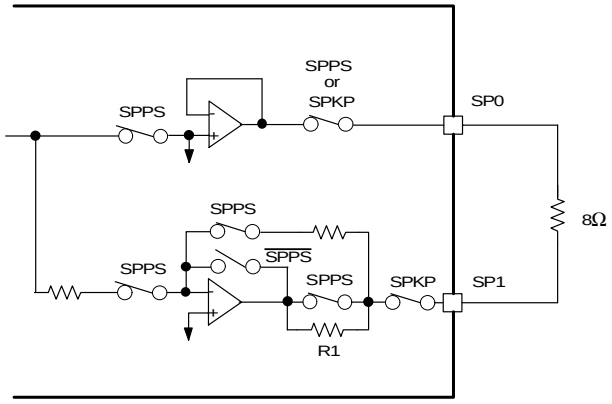


Figure 26. Speaker-Amp Normal Operation

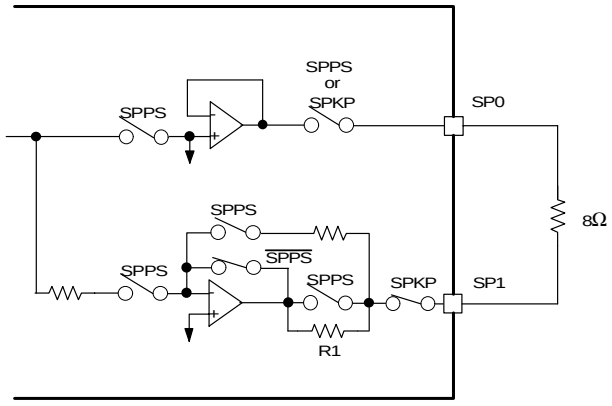


Figure 27. Speaker-Amp Power-Save-Mode

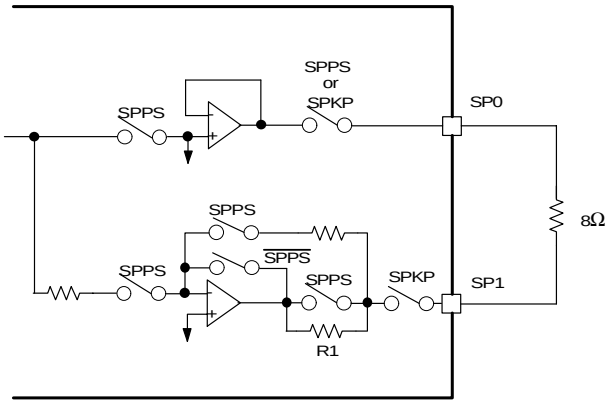


Figure 28. Speaker-Amp Power-Down-Mode

1. Monaural Output

Both L/R channels of output signal from analog volume (OPGA) are mixed at (L+R)/2. When MOUT bit is "0", these signals can be OFF. Then MOUT pin outputs VCOM voltage. Load impedance is 10kΩ (min.).
When SPKP bit is "0", MOUT pin becomes Power-Down-Mode and outputs Hi-z.

2. ALC2

Input resistance of ALC2 is 23kΩ (typ.) and centered around VCOM voltage, and input signal level is –5.5dBV. (Refer to Figure 29)

Limiter detection level is not related to power supply voltage, output level is limited by the ALC2 circuit when input signal exceeds –7.5dBV (=FS-2dB@VA=2.8V) and over.

When the continuous signal of –7.5dBV and over is input to the ALC2 circuit, the change period of ALC2 limiter operation is 2/fs=42us@fs=48kHz and the attenuation level is 0.5dB/step.
The ALC2 recovery operation is always detected by zero crossing operation and gains 1dB/step. The ALC2 recovery operation is done until input level of speaker-Amp goes to –9.5dBV(=FS-4dB@VA=2.8V). The ALC2 recovery operation period is fixed to 2048/fs=42.7mS@fs=48kHz.
In case of inputting signal between –7.5dBV and –9.5dBV, the ALC2 limiter or recovery operations are not done.

When $\overline{\text{PD}}$ pin changes from "L" to "H" or SPKP bit changes from "0" to "1", the initilizing cycle (2048/fs = 42.7ms @fs=48kHz) starts. ALC2 is disabled during initilizing cycle, ALC2 starts after finishing the initilizing cycle.

Parameter		ALC2 Limiter operation	ALC2 Recovery operation
Operation Start Level		-7.5dBV	-9.5dBV
Period	fs=48kHz	2/fs = 42us	2048/fs = 42.7ms
	fs=32kHz	2/fs = 63us	2048/fs = 64ms
Zero-crossing Detection		No	Yes(Timeout = 2048/fs)
ATT/GAIN		0.5dB step	1dB step

Table 16. Content of ALC2

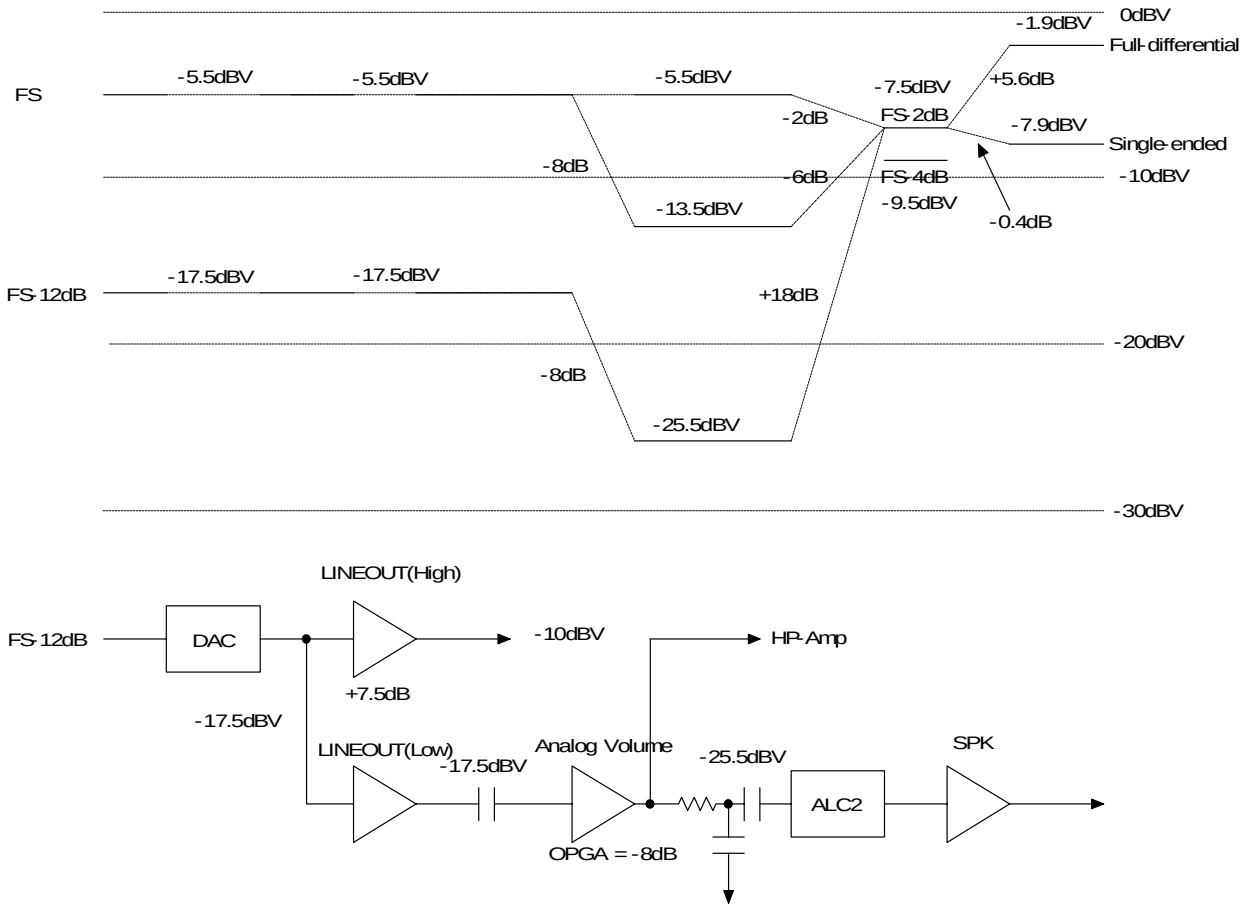


Figure 29. Speaker-Amp Output Level Diagram (VA=2.8V, OPGA = -8dB, VOL1-0=+7.5dB)

■ ALC1 Operation

1. ALC1 Limiter Operation

During the ALC1 limiter operation, when either Lch or Rch exceed ALC1 limiter detection level (LMTH), IPGA value is attenuated by ALC1 limiter ATT step (LMAT1-0) automatically. Then the IPGA value is changed commonly for L/R channels.

In case of ZELM = "1", timeout period is set by LTM1-0 bits. The operation for attenuation is done continuously until the input signal level becomes LMTH or less. After finishing the operation for attenuation, if ALC1 bit does not change into "0", the operation of attenuation repeats when the input signal level exceed LMTH. (Refer to Figure 30)

In case of ZELM = "0", timeout period is set by ZTM1-0 bits. The IPGA value is attenuated by zero crossing detection automatically. (Refer to Figure 31)

The ALC1 operation corresponds to the impulse noise in additional to the ALC operation of AK4516A. When the impulse noise is input, the ALC1 recovery operation becomes the faster period than a normal recovery operation.

[Explanation for ALC1 operation]

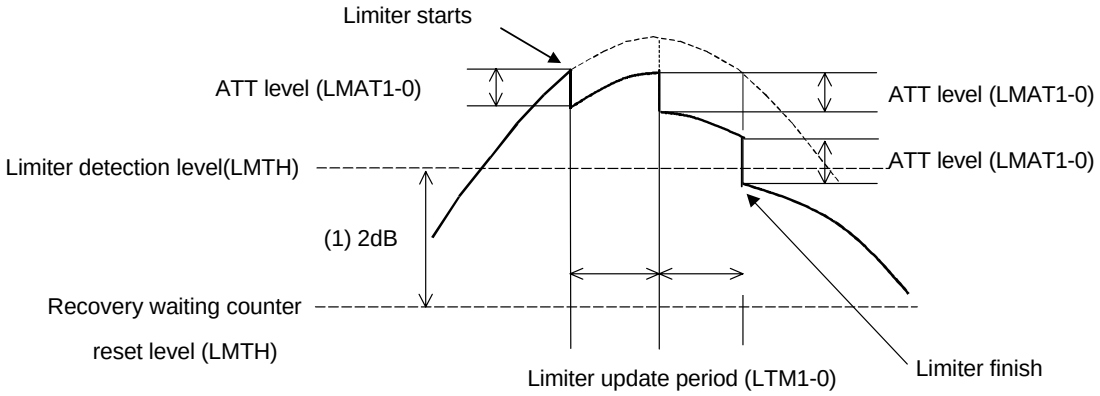


Figure 30. Disable ALC1 zero crossing detection (ZELM = "1")

(1). When the signal is input between 2dB, the AK4560A does not operate the ALC1 limiter and recovery.

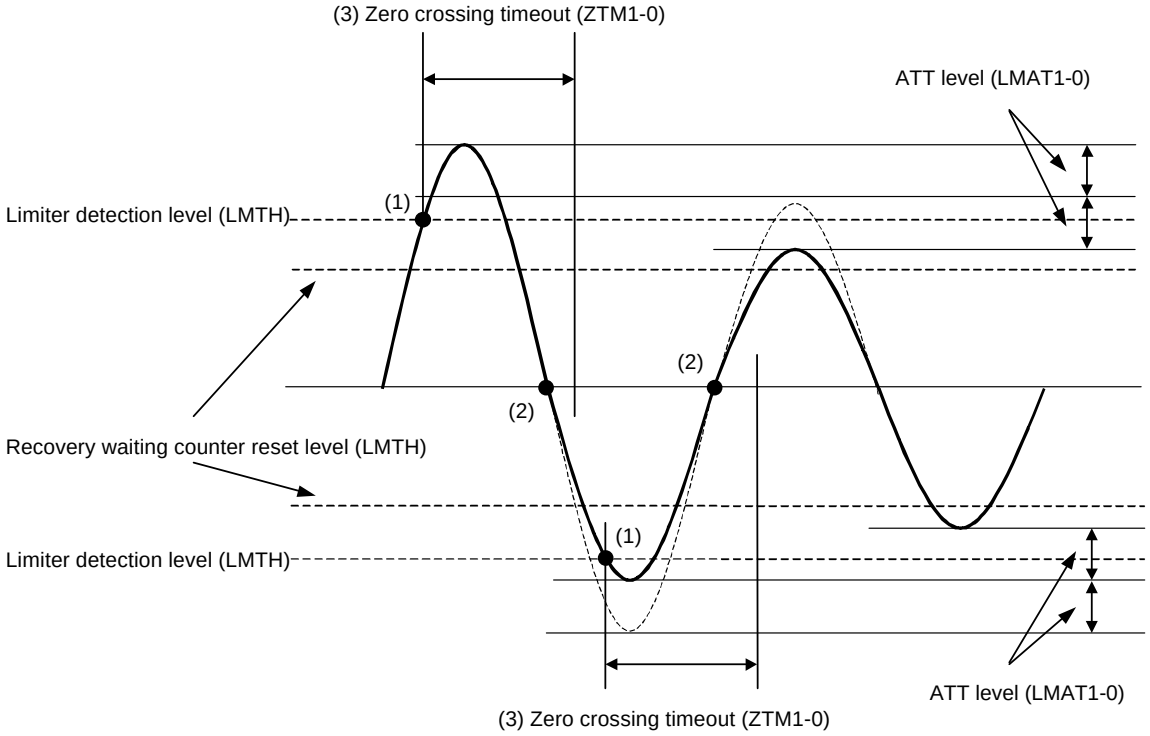


Figure 31. In case of continuing the limiter operation (ZELM = "0")

(1) When the input level exceeds the ALC1 limiter detection level, the ALC1 limiter operation starts. Zero crossing counter starts at the same time.
(2) Zero crossing detection. When the input signal is detected, the IPGA value is attenuated until the value set by LMAT1-0 and the ALC1 limiter operation is finished.
(3) Zero crossing timeout is set by ZTM1-0 bits. But the first zero crossing timeout cycle after starting the limiter operation may be the short cycle by the state of the last zero crossing counter. (For example, in case of doing the limiter operation during the recovery operation)

2. ALC1 Recovery Operation

The ALC1 recovery operation waits until a time of setting WTM1-0 bits after completing the ALC1 limiter. If the input signal does not exceed "LMTH – 2dB", the ALC1 recovery operation is done. The IPGA value increases automatically by this operation up to the set reference level (REF6-0 bits). Then the IPGA value is set for L/R commonly. The ALC1 recovery operation is done at a period set by WTM1-0 bits.

When L/R channels are detected by zero crossing operation during WTM1-0, the ALC1 recovery operation waits until WTM1-0 period and the next recovery operation is done.

During the ALC1 recovery operation, when either input signal level of Lch or Rch exceeds the ALC1 limiter detection level (LNTH), the ALC1 recovery operation changes into the ALC1 limiter operation immediately
In case of "(Recovery waiting counter reset level) ≤ Input Signal < Limiter detection level" during the ALC1 recovery operation, the waiting timer of ALC1 recovery operation is reset. Therefore, in case of "(Recovery waiting counter reset level) > Input Signal", the waiting timer of ALC1 recovery operation starts.

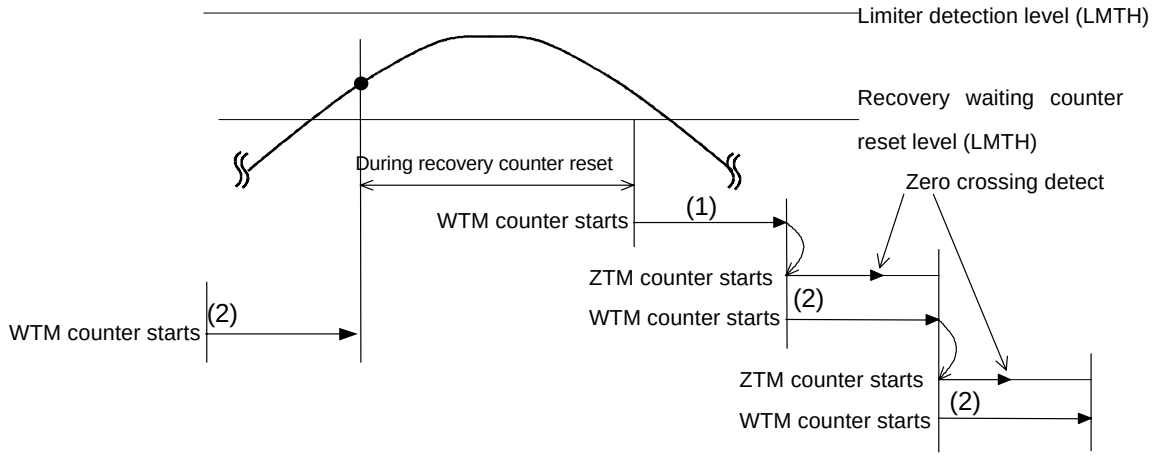


Figure 32. The transition from the limiter operation to the recovery operation

(1). When the input signal is below the ALC1 recovery waiting counter reset level, the ALC1 recovery operation waits the time set by WTM1-0 bits. If the input signal does not exceed the ALC1 limiter detection level or the ALC1 recovery waiting counter reset level, the ALC1 recovery operation is done only once.
(2). The IPGA value is changed by the zero crossing operation in ALC1 recovery operation, but the next counter of the ALC1 recovery waiting timer is also starting.

Other:

When a channel of one side enters the limiter operation during the waiting zero crossing, the present ALC1 recovery operation stops, according as the small value of IPGA (a channel of waiting zero crossing), the ALC1 limiter operation is done.
When both channels are waiting for the next ALC1 recovery operation, the ALC1 limiter operation is done from the IPGA value of a point in time.
During the ALC1 operation, the value of writing in IPGA6-0 bits is ignored.

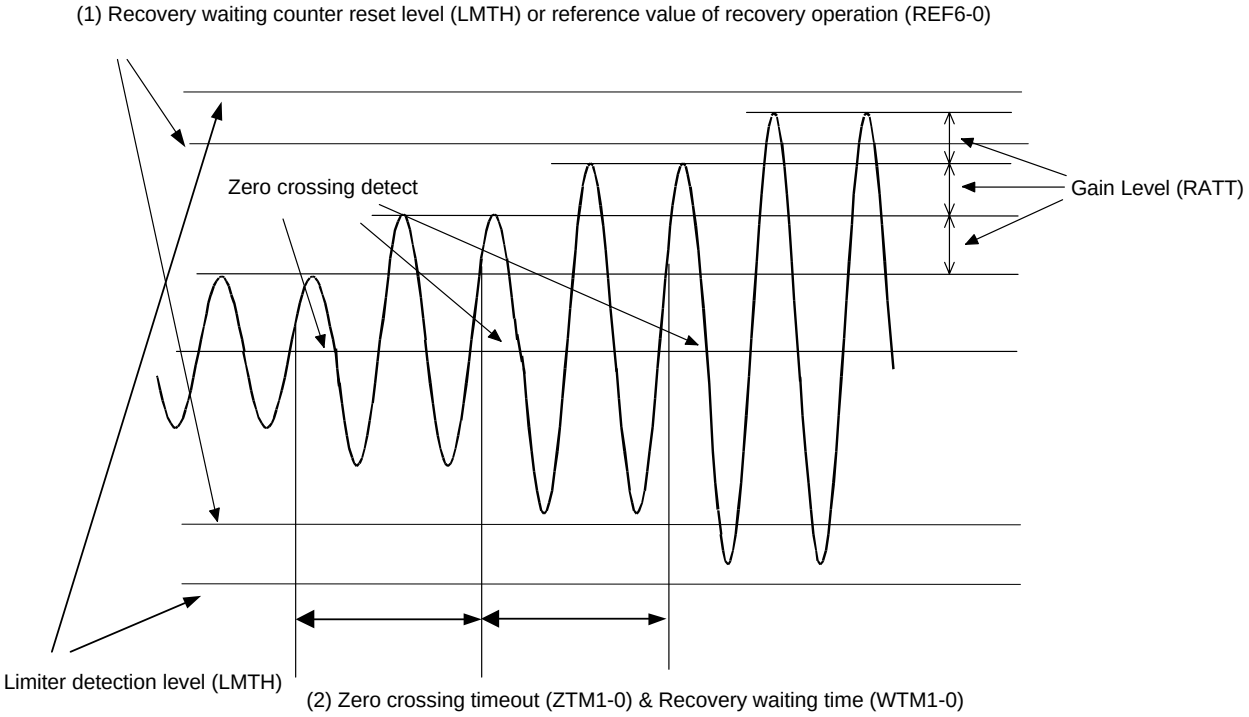


Figure 33. The continuous ALC1 Recovery Operation

(1). When the input signal exceeds the ALC1 recovery waiting counter reset level, the ALC1 recovery operation stops, the ALC1 recovery operation is repeated when input signal level is below "LMTH" again. When the IPGA value by repeating the ALC1 recovery operation reaches the reference level (REF6-0 bits), the ALC1 recovery operation stops also

(2). ZTM bit sets zero crossing timeout and WTM bit sets the ALC1 recovery operation period. When the ALC1 recovery waiting time (WTM1-0 bits) is shorter than zero crossing timeout period of ZTM1-0 bit, the ALC1 recovery is operated by the zero crossing timeout period of ZTM1-0 bit. Therefore, in this case the auto recovery operation period is not constant.

3. ALC1 Operation OFF (ALC1 bit = "0")

The zero crossing detection of IPGA is done to L/R channels independently. Zero crossing timeout is set by ZTM1-0 bits. When the control register is written from uP, the zero crossing counter for L/R channels commonly is reset and its counter starts. When the signal detects zero crossing or zero crossing timeout, the written value from uP becomes a valid for the first time. In case of writing to the control register continually, the control register should be written by an interval more than zero crossing timeout. If an appointed interval is written, there is possible to the different value the IPGA value of L/R channels

For example, when the present IPGA value is updated by zero crossing detection in a channel of one side and other channel is not updated, if the new data is written in IPGA, the updated channel is keeping the last IPGA value and other channel is updated to a new IPGA value by the last zero crossing counter. Therefore, zero crossing counter does not reset when the zero crossing detection is waiting.

During ALC1 operation, the following registers are inhibits.
• LTM1-0, LMTH, LMAT1-0, WTM1-0, ZTM1-0, RATT, REF6-0

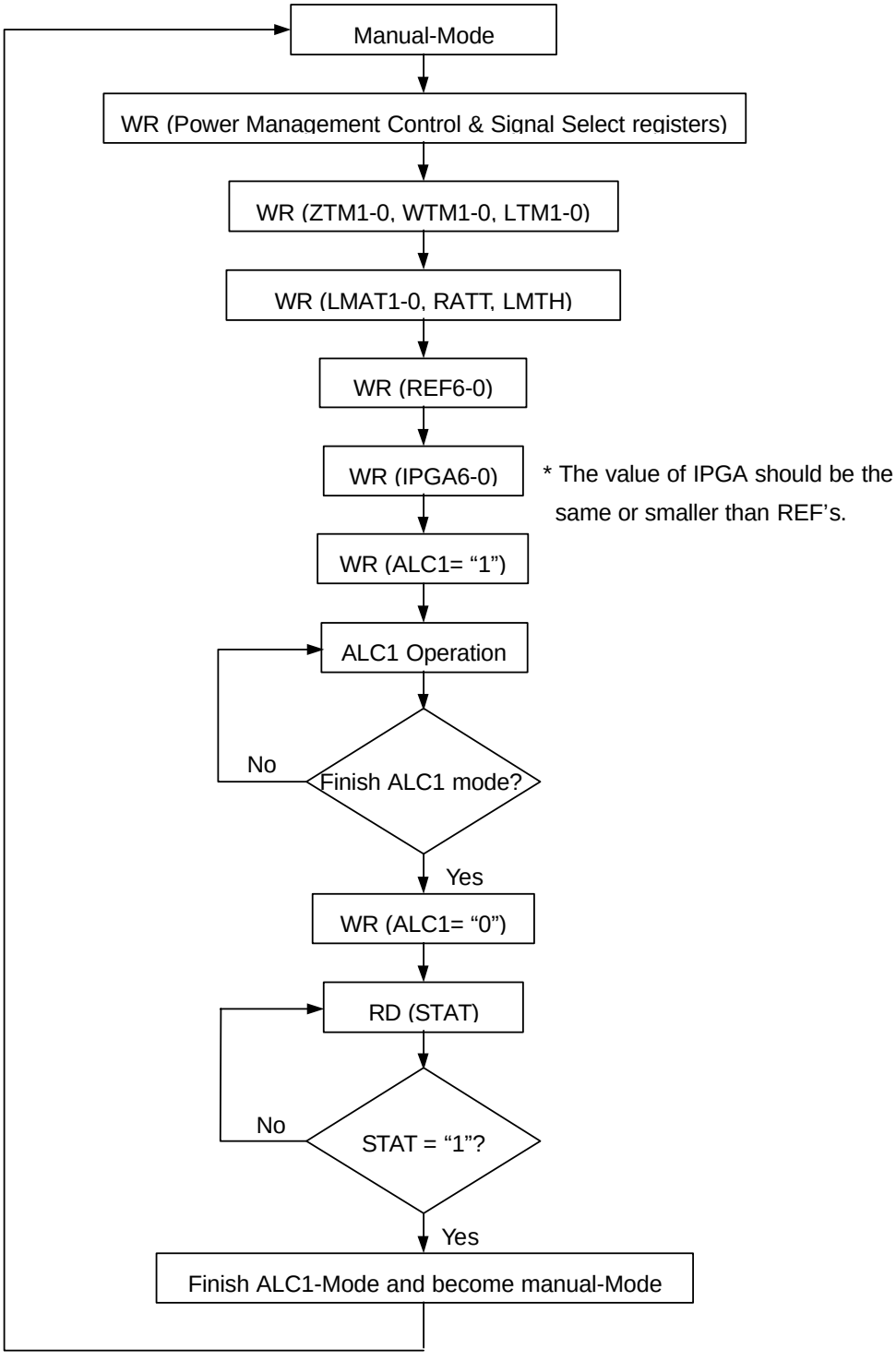


Figure 34. Registers set-up sequence at ALC1 operation

■ FADEIN Mode

In FADEIN Mode, the IPGA value is increased at the value set by FDATT when FDIN bit changes from "0" to "1". The update period can be set by FDTM1-0 bits. The FADEIN Mode is always detected by the zero crossing operation. This operation is kept over the REF value or until the limiter operation at once. If the limiter operation is done during FADAIN cycle, the FADEIN operation becomes the ALC operation.

NOTE: When FDIN and FDOUT bits are "1", FDOUT operation is enabled.

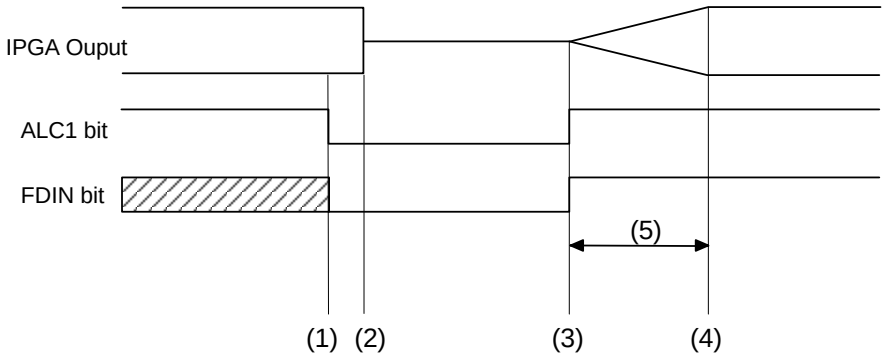


Figure 35. Example for controlling sequence in FADEIN operation

(1) WR (ALC1 = FDIN = "0"): The ALC1 operation is disabled. To start the FADEIN operation, FDIN bit is written in "0".
(2) WR (IPGA = "MUTE"): The IPGA output is muted.
(3) WR (ALC1 = FDIN = "1"): The FADEIN operation starts. The IPGA changes from the MUTE state to the FADEIN operation.
(4) The FADEIN operation is done until the limiter detection level (LMTH) or the reference level (REF6-0). After completing the FADEIN operation, the AK4560A becomes the ALC1 operation.
(5) FADEIN time can be set by FDTM1-0 and FDATT bits
E.g. FDTM1-0 = 1024/fs @ fs =48kHz = 21.3ms, FDATT = 1step
(96 x FDTM1-0) / FDATT = 96 x 21.3ms / 1 = 2.04s

■ **FADEOUT Mode**

In FADEOUT mode, the present IPGA value is decreased until the MUTE state when FDOUT bit changes from "0" to "1". This operation is always detected by the zero crossing operation.
If the large signal is input to the ALC1 circuit during the FADEOUT operation, the ALC1 limiter operation is done. However a total time of the FADEOUT operation is the same time, even if the limiter operation is done. The period of FADEOUT is set by FDTM1-0 bits, a number of step can be set by FDATT bit.
When FDOUT bit changes into "0" during the FADEOUT operation, the ALC1 operation start from the preset IPGA value.
When FDOUT and ALC1 bits change into "0" at the same time, the FDOUT operation stops and the IPGA becomes the value at that time.

NOTE: When FDIN and FDOUT bits are "1", FDOUT bit is enabled.

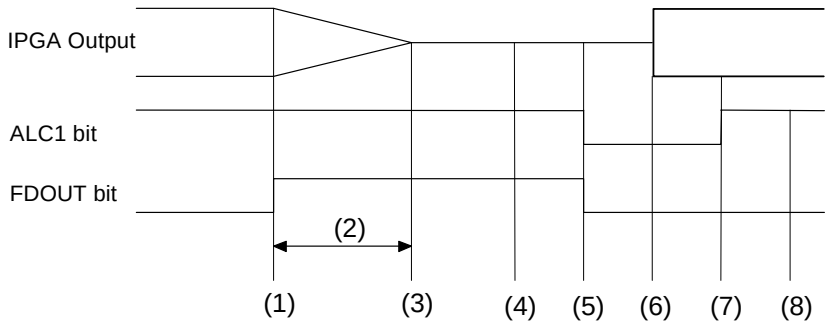
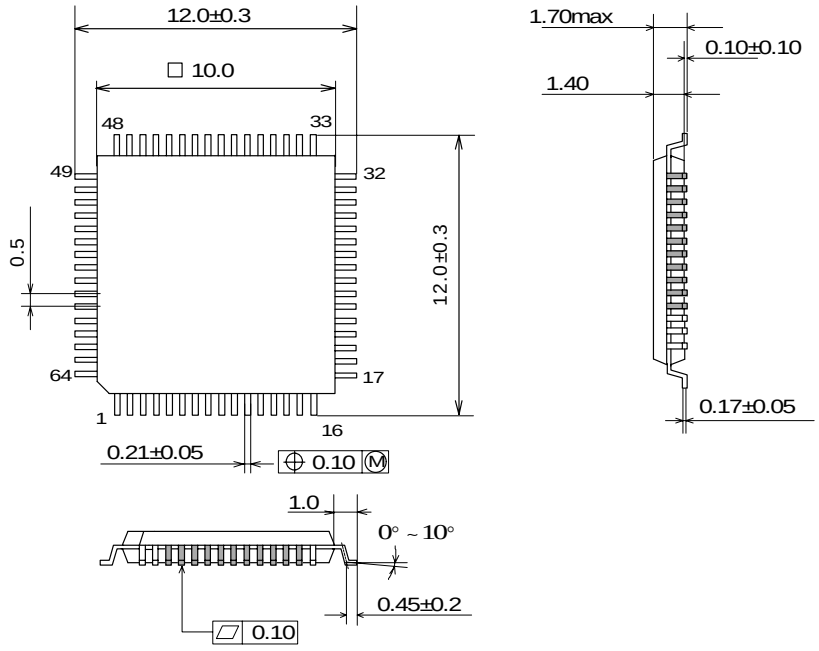


Figure 36. Example for controlling sequence in FADEOUT operation

(1) WR (FDOUT = "1"): The FADEOUT operation starts. Then ALC1 bit should be always "1".
(2) FADEOUT time can be set by FDTM1-0 and FDATT bits.
During the FADEIN operation, the zero crossing timeout period is ignored and becomes the same as the FADEIN period.
E.g. FDTM1-0 = 1024/fs @ fs =48kHz = 21.3ms, FDATT = 1step
(96 x FDTM1-0) / FDATT = 96 x 21.3ms / 1 = 2.04s
(3) The FADEOUT operation is completed. The IPGA value is the MUTE state. If FDOUT bit is keeping "1", the IPGA value is keeping the MUTE state.
(4) Analog and digital outputs mutes externally. Then the IPGA value is the MUTE state.
(5) WR (ALC1 = FDOUT = "0"): Exit the ALC1 and FADEOUT operations
(6) WR (IPGA): The IPGA value changes the initial value (exiting MUTE state).
(7) WR (ALC1 = "1", FDOUT = "0"): The ALC1 operation restarts. But the ALC1 bit should not write until completing zero crossing operation of IPGA.
(8) Release a mute function of analog and digital outputs externally.

PACKAGE

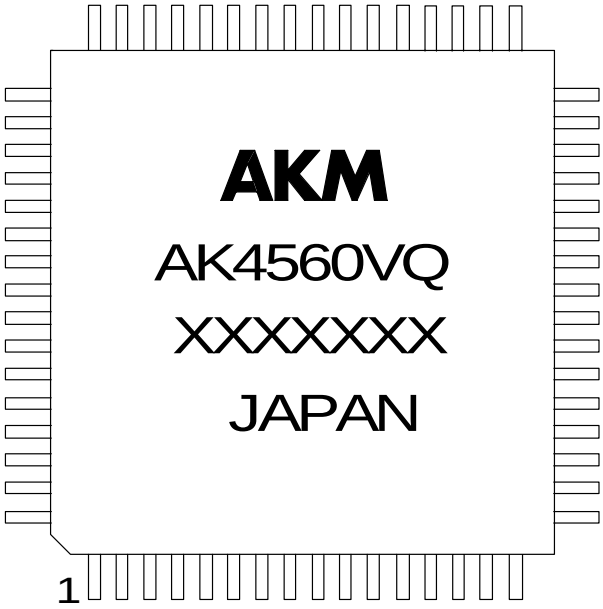
64pin LQFP(Unit:mm)



■ **Package & Lead frame material**

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder plate

MARKING



- Asashi kasei Logo
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- Date Code: XXXXXXX (7 digits)
  First 4 digits: weekly code, Remains 3 digits: code management in office
- Country of Origin: JAPAN